REVIEW

Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs

To cite this article: Ron Green et al 2016 Jpn. J. Appl. Phys. 55 04EA03

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1. Introduction

Instability of the threshold-voltage (V_T) in SiC MOSFETs, first reported in 2006, has become an important reliability issue in the past few years. As such, it has been studied by a number of different research groups in recent years. This work reports on three important aspects of the issue: (1) the V_T instability observed in commercial devices, (2) a summary of the basic mechanisms driving this instability, and (3) the need for an improved test method for evaluating these devices. Even under significant overstress conditions, no negative threshold-voltage shift was observed in the most-recent vintage commercial devices from one of the manufacturers during a -15 V, 175 °C negative-bias temperature stress lasting 120 h. © 2016 The Japan Society of Applied Physics

2. Background

There are two basic mechanisms that affect the V_T stability: oxide-trap activation and oxide-trap charging. The oxide traps themselves are defects related to an oxygen vacancy, resulting in a weak Si–Si bond. If this bond is broken, the defect becomes an active trap site, referred to in some of the literature as an E’ center. Once active, it may then engage in charge trapping. In fact, the E’ center is known to be a hole trap. Trapped positive charge in the gate oxide results in a negative shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerably during a bias-temperature stress at temperatures at and above 150 °C. This increase in V_T instability, whether determined by a unipolar gate-bias stress or a back-and-forth bipolar stress-and-measure sequence, is likely due to the activation of additional E’ centers in the oxide, causing a positive shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerably during a bias-temperature stress at temperatures at and above 150 °C. This increase in V_T instability, whether determined by a unipolar gate-bias stress or a back-and-forth bipolar stress-and-measure sequence, is likely due to the activation of additional E’ centers in the oxide, causing a positive shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerably during a bias-temperature stress at temperatures at and above 150 °C. This increase in V_T instability, whether determined by a unipolar gate-bias stress or a back-and-forth bipolar stress-and-measure sequence, is likely due to the activation of additional E’ centers in the oxide, causing a positive shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerably during a bias-temperature stress at temperatures at and above 150 °C. This increase in V_T instability, whether determined by a unipolar gate-bias stress or a back-and-forth bipolar stress-and-measure sequence, is likely due to the activation of additional E’ centers in the oxide, causing a positive shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerably during a bias-temperature stress at temperatures at and above 150 °C. This increase in V_T instability, whether determined by a unipolar gate-bias stress or a back-and-forth bipolar stress-and-measure sequence, is likely due to the activation of additional E’ centers in the oxide, causing a positive shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerable...
When activation is not present, the $V_T$ shift generally exhibits a linear-with-log-time response to a bias stress. This is because the oxide-trap charging occurs via a direct tunneling mechanism.\cite{27,28} In fact, a two-way tunneling model predicts a tunneling front that proceeds from the interface into the oxide at a rate of 1.5 to 2 A per decade of time.\cite{2} This implies that the oxide traps close to the interface can change charge state very, very quickly, and suggests that the time taken to measure the effect of a stress greatly affects what is observed. If there is too long a delay following the removal of the stress bias, or the bias applied during the measurement is present for an extended period of time, then the full effect of the bias stress will not be observed.\cite{2} This summary focuses on near-interfacial oxide traps as the main charge-trapping defect affecting the $V_T$ stability. However, interface traps may very well play an important supporting role if a two-step charging mechanism involves interface traps as a necessary intermediary.\cite{2} We have also observed evidence of interface trap build-up during bias-temperature stressing.\cite{2} Our overall conceptual framework has been based not only on testing commercially-available SiC power MOSFETs, but also MOS test structures and devices wherein details of the device design and processing are in some cases more readily accessible.\cite{27,28,33}

Processing also affects $V_T$ stability. Since some $V_T$ instability is observed in as-processed devices at room temperature prior to bias-temperature stressing, clearly some trap activation must occur during processing. Furthermore, it has been previously reported that the standard nitrogen-based post-oxidation anneal, used to suppress interface traps and improve channel mobility, also reduces $V_T$ instability.\cite{29,34} Other recent results indicate the benefits of a P-based anneal as well.\cite{13}

Present test methods employed by industry qualification standards (Automotive Electronics Council Q101\cite{20} — based on the JEDEC JESD-22 A108C test method\cite{21}) and military standards (MIL-STD-750\cite{22}) — test method 1042.3 for device burn-in and life-testing) allow long delay times such that devices that would have been deemed to have failed by shifting too much may instead be judged to be stable.\cite{23,24} Thus, improved test methods are needed.

3. Experimental procedure

The devices used in this BTI evaluation and comparison are representative of three different vintages of commercially-available 1200 V SiC MOSFETs from one leading manufacturer (“Vendor A”—including their most recent) and the most recent vintage from a second major manufacturer (“Vendor B”). Table I lists the vendor, date of purchase, maximum junction temperature, and gate-voltage specifications for each device under evaluation. First-generation Vendor A devices were purchased in April 2012 and second-generation devices in May and September of 2014. The Vendor B devices were all purchased in September 2014.

The BTI test system features computer control and monitoring of device temperature, stress bias, and other key measurement parameters. An Omega benchtop controller with dual 5-A solid-state relay outputs was used for control of an Ultramic® ceramic heater with temperature operation up to 400 °C, and a solenoid air valve for rapid device heating and cooling between 25 and 200 °C. Device cooling was achieved by forced-air-flow of compressed nitrogen over a pin-fin heat sink and device package assembly. Device heating was generally achieved in 1 to 2 min while device cooling took between 3 to 5 min to stabilize back at room temperature. The adopted test methodology, described in detail below, was implemented using conventional parametric testers equipped with source measurement units (SMU) that force and sense $V_D$ and $I_T$.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>$T_{j, \text{Max}}$</th>
<th>$V_{GS, \text{Max}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor A (April 2012)</td>
<td>135 °C</td>
<td>−5/+25 V</td>
</tr>
<tr>
<td>Vendor A (May 2014)</td>
<td>150 °C</td>
<td>−10/+25 V</td>
</tr>
<tr>
<td>Vendor A (August 2014)</td>
<td>150 °C</td>
<td>−10/+25 V</td>
</tr>
<tr>
<td>Vendor B (September 2014)</td>
<td>175 °C</td>
<td>−6/+22 V</td>
</tr>
</tbody>
</table>

Fig. 1. (Color online) Schematic diagram of the experimental test methods used to measure both the $V_T$ shift and $V_T$ hysteresis following a unipolar negative-bias temperature stress. The $V_T$ shift was characterized at high temperature by sweeping $V_{GS}$ in the appropriate direction (from −5 to +15 V) to measure $I_T$, and the $V_T$ hysteresis was characterized at room temperature using a three-cycle switched-bias stress sequence.

Fig. 2. (Color online) Schematic diagram of the experimental test methods used to measure both the $V_T$ shift and $V_T$ hysteresis following a unipolar positive-bias temperature stress.
not expose the device-under-test to an opposite-bias-polarity bias-temperature stress.

Each device was subject to a temperature stress of 175 °C with a gate-voltage stress of either +25 or −15 V (VGS set to 0 V) to investigate positive BTI (PBTI) and negative BTI (NBTI), respectively. In order to perform a fair comparison, the stress conditions had to be identical for all devices tested. 175 °C was chosen as the stress temperature since it was the highest temperature specified for any of the devices (see Table I). This also represents a temperature of interest for Army applications. Likewise, the positive-bias stress was set at +25 V, matching the greatest positive bias specified for any of the devices. The negative-bias stress was set at −15 V to accelerate NBTI in the most recent devices from both manufacturers, even though it exceeds the greatest bias specified for any of the devices tested. The maximum negative gate-voltage specification is set conservatively by the manufacturer to limit charging and reduce the effects of NBTI. Accelerating the negative stress bias demonstrates device robustness to charging effects that can cause parametric drift in VTH under NBTS conditions.

Although it is true that the VTH shift due to interfacial charge is dependent on gate-oxide thickness, as is the local electric field in the oxide, the specific thickness used is a device-design decision made by the manufacturer. The application engineer will simply want to know how stable VTH is for any particular application. On the other hand, qualification testing will require that a minimum acceptable level of reliability is demonstrated.

An unbiased ramp of room temperature to the stress temperature (in this case 175 °C) marked the beginning of the test sequence; and once the temperature had stabilized to within ±1 °C of the set point, an immediate sweep of VGS (positive direction for NBTS and negative direction for PBTI—see Figs. 1 and 2, respectively) and measurement of ID was performed, characterizing VTH before any high-temperature stressing had occurred. The accuracy of the sweep method in determining VTH is dependent on key measurement factors such as: 1) time delay between stress-bias removal and application of the measurement bias, 2) sweep speed, and 3) direction of the gate sweep. The delay in applying the measurement bias following removal of the stress bias results in a potential relaxation of the charge state of the oxide traps and subsequent underestimation of the change in VTH due to the stress bias. Therefore, the delay time associated with bias interruption should be minimized. We have optimized our test system and reduced this delay time to about 10 ms. The time required to complete a measurement sweep can also alter the charge state of the oxide traps previously established by the dc gate-bias stress and thereby affect VTH. Shorter measurement times (on the order of tens of μs) are preferred because this allows fewer traps to change charge state. However, such faster measurements require more expensive test equipment to better characterize VTH. Our standard parameter analyzer test system can make these measurements in about 2 s even when sweeping VGS over a 25 V range. Specification of the direction of the measurement sweep is extremely important when using a sweep method to characterize VTH since starting the measurement sweep near the stress bias and sweeping VGS towards VTH results in fewer changes in the charge state of near-interfacial oxide traps during the measurement. Therefore, a negative-bias temperature stress (NBTIS) is followed by a positive sweep of VGS and a positive-bias temperature stress (PBTS) is followed by a negative sweep of VGS.

One of the main advantages of SiC devices is their high-temperature capability. Therefore, it is of the utmost importance that high-temperature measurements be performed following the bias-temperature stress. These will always reveal the largest shifts in threshold voltage when significant trap activation has occurred. That is why in this present study we focused on immediate high-temperature measurements. However, it should be noted that when little or no trap activation occurs, larger shifts in VTH may be observed when performing immediate measurements at room temperature (without first making a high-temperature measurement) by rapidly cooling the device while maintaining stress bias. In our particular test sequence (see Figs. 1 and 2), we made an immediate high-temperature measurement to measure the VTH shift, rapidly cooled the device using the system described in detail above, and then performed the room-temperature back-and-forth stress-and-measure test sequence to measure the VTH hysteresis. The results of applying this test method to various commercially-available 1.2 kV SiC power MOSFETs are reported in the next section.

Figure 3 shows an example of the shift in the ID–VTH characteristics of a SiC MOSFET for a series of NBTS segments, using the test method described above and highlighted in Fig. 1. The log of the drain current is plotted for increasing stress times out to 120 h. As expected for a NBTS, a negative shift in the characteristic curves was observed for increasing cumulative stress times, which is consistent with the positive charging of near-interfacial oxide traps.

In characterizing the subthreshold VTH hysteresis, a threecycle stress-and-measure sequence was employed, with each individual cycle consisting of two stress (VGS = ±15 V) and two measurement segments, for a total of six bias and six measurement segments (see Figs. 1 and 2). As always, VGS was swept in a direction away from the stress bias. Performed after each bias-temperature-stress segment, this allowed us to characterize the VTH hysteresis as a function of cumulative unipolar bias-temperature-stress time.

Figure 4 plots the log of the drain current versus VGS for a given three-cycle alternating-bias test sequence performed at room temperature. A total of six curves are shown—three curves swept in the negative direction following a 100 s
positive gate stress ($V_{GS} = +15 \text{ V}$) and three curves swept in the positive direction following a negative gate stress ($V_{GS} = -15 \text{ V}$), also for 100 s. The $V_T$ hysteresis is determined from the difference in $V_{GS}$ in the subthreshold region between the positive and negative sweeps at a constant drain current ($I_D = 3 \times 10^{-3} \text{ A}$). We used the lowest current level consistently above the noise in order to get the largest active oxide-trap signal possible for such a short stress time. We performed these short 100 s stresses at room temperature so that the devices would not be exposed to opposite-polarity bias-temperature stresses, and so that the effect of the cumulative BTS time could be compared more readily to pre-stress values, whereby an increase in the width of the hysteresis in the $I_D$–$V_{GS}$ characteristics is an indication of increased numbers of active near-interfacial oxide traps present.

4. Results and discussion

4.1 $V_T$ shift due to unipolar bias-temperature stress

In this section, we present unipolar high-temperature gate-bias (HTGB) bias-temperature stress electrical test results for three vintages of commercial SiC MOSFETs from Vendor A, including their most recent MOSFETs, and the latest device offering from Vendor B (as of September 2014). All device testing and measurements were carried out at 175 °C using the BTTI test procedures described previously. The test results discussed below characterize the responses of SiC MOSFETs to unipolar gate-bias stress effects at high temperature.

Figure 5 shows the $V_T$ shift response of three different vintages of commercial SiC power MOSFETs from Vendor A when exposed to an overstress of $-15 \text{ V}$ at 175 °C. The shift in $V_T$ was determined by the difference of the initial $I_D$–$V_{GS}$ measurement and post-stress measurements made periodically while at temperature during the gate-bias stress. The data reveals a significant difference in the response of the latest (August 2014) devices and the two earlier commercial releases. The two earlier Vendor A vintages exhibited quite large negative $V_T$ shifts ranging from 3 to 7 V under these NBTS conditions, with trap activation becoming apparent at stress times greater than $10^3 \text{ s}$. In stark contrast, the most-recent-vintage Vendor A devices are very stable under NBTS. This dramatic improvement bodes well for the successful commercialization of these devices, which are only presently rated for $-10 \text{ V}$ at 150 °C (see Table I). The shift in $V_{T,\text{sub}}$ (calculated for $I_D = 3 \times 10^{-3} \text{ A}$) is shown, since the magnitude of the drain-leakage current is the most important consideration under negative bias since this is an OFF-voltage condition. (It should be noted that using the linear $V_T$ shift for the same devices and under the same test conditions resulted in similar results, although the shifts were somewhat smaller.) Significant increases in the subthreshold drain-leakage current during blocking will reduce the voltage hold-off capability of the device.

Figure 6 shows a comparison of recent-vintage Vendor A and Vendor B devices when exposed to an overstress of $-15 \text{ V}$ at 175 °C. The most-recent-vintage Vendor A results from Fig. 5 are replotted in Fig. 6, but on a finer scale. On this scale it can be seen that there is actually a slight positive shift that occurs during this NBTS. This may be due to a slight increase in interface traps, which are negatively charged in inversion for these n-channel MOSFETs. The Vendor B device shifts slightly more than 1 V for this mid-$10^3 \text{ s}$ (approximately 120 h) stress, which is much better than that of previous-vintage Vendor A devices. The negative shift is observed after the earliest measurement, and continues to drift negatively, rather than exhibiting a sharp knee in the curve as was observed for the older (May 2014) Vendor A devices in Fig. 5. Shifting of this magnitude is inconsequential for these specific conditions in that $V_T$ did not shift far enough negatively to significantly increase the subthreshold drain-leakage current because these devices have sufficient positive margin ($V_{T,\text{sub}} = 1.4 \text{ V}$) even at 175 °C. However, for longer stress times, based on the slightly super-linear negative shift of $V_T$ with log stress time, we would expect to observe an increase in subthreshold leakage current at some point. But it is also important to note that this was a significant overstress.
MOSFETs from Vendor A due to a +25 V, 175 °C PBTS. Results are very similar to Fig. 7. Figure 9 shows a comparison of recent-vintage Vendor A devices, which, although rated for +25 V, are only rated at 150 °C; and for the Vendor B devices, which, although rated at 175 °C, are only rated at +22 V (see Table I).

4.2 \( V_T \) hysteresis due to unipolar bias-temperature stress

This section describes the results of the back-and-forth room-temperature stress-and-measure sequences depicted on the right-hand sides of both Figs. 1 and 2, following either a unipolar negative or positive BTS step, respectively. This switched-polarity gate-bias stress enables us to observe the hysteresis of the \( I_{DSS} - V_{GS} \) characteristic, which is a measure of the \( V_T \) instability due to switching oxide traps located near the SiC interface. As such, it gives us a fair way of comparing the level of oxide-trap activation (over a similar range of distance in the oxide from the SiC interface) that has occurred due to various different types of bias-stress conditions because the oxide-trap charging should be the same. A larger hysteresis indicates more active oxide traps and an increase in the hysteresis indicates that a particular stress increased the number of active oxide traps available to participate in the back-and-forth positive-charging and neutralization process.

This measurement also enables us to observe trap activation that might be missed by simpler unipolar \( V_T \) shift measurements. For example, it is possible that not much charging of additional active oxide traps will occur during a PBTS (unless high-temperature electron trapping is occurring in the oxide or there is a build-up of negatively charged interface traps). But a room-temperature back-and-forth stress-and-measure sequence will allow any oxide traps activated under positive bias to be charged under negative bias (without subjecting the device directly to a NBTS), thereby exposing their presence. A positive gate stress typically results in a positive shift in \( V_T \) and a negative gate stress causes \( V_T \) to shift in a negative direction for the Vendor B devices, which are rated for −6 V at 175 °C (see Table I).

Figure 7 shows the \( V_T \) shift response of three different vintages of commercial Vendor A SiC power MOSFETs when exposed to a slight overstress of +25 V at 175 °C. Once again, the two earlier-vintage Vendor A devices exhibited large \( V_T \) shifts, this time in the positive direction, which began at cumulative stress times greater than \( 10^4 \) s, and ranged from 2 to 5 V after 120 h of PBTS. And once again the most-recent-vintage Vendor A devices show a dramatic improvement in \( V_T \) stability. The observed voltage shifts in older (May 2014) devices were much larger than expected and occurred significantly earlier in time, even when compared to the oldest devices that were released two years earlier.

The results plotted in Fig. 7 were for \( V_T \) calculated using the linear \( V_T \) shift of the most-recently-tested-vintage commercial SiC power MOSFETs from Vendor A and Vendor B due to a +25 V, 175 °C PBTS. Results are very similar to Fig. 7.
direction. As described previously, a direct tunneling mechanism drives this phenomenon. Since the application of a gate stress at room temperature does not lead to additional defect formation in the gate oxide, as the magnitude of the measured \( V_T \) hysteresis remains unchanged for the same bias and measurement conditions.\(^{21}\) \( V_T \) hysteresis measurements performed at room temperature can be used to provide a measure of oxide-trap activation occurring during high-temperature gate-bias stressing.

Figure 10 shows the \( V_T \) hysteresis response of two different vintages of commercial SiC power MOSFETs from Vendor A, measured at room temperature, as a function of cumulative stress time for a \(-15\,\text{V}, 175\,\text{°C}\) NBTS. The \( V_T \) hysteresis was determined by the back-and-forth room-temperature \(+15\,\text{V}\) stress-and-measure sequence shown on the right-hand side of Fig. 1 and illustrated in Fig. 4, performed periodically during the NBTS. The data reveals a noticeable difference in the response of the newer (August 2014) Vendor A devices compared to earlier (May 2014) devices. The earlier-vintage Vendor A devices exhibited significant trap activation at stress times greater than \(10^4\,\text{s}\), consistent with \( V_T \) shift results shown in Fig. 5 in terms of timing. On the other hand, the most-recent-vintage Vendor A devices show only the slightest of increases due to the NBTS. This is to be expected for these devices, which did not drift negatively during the unipolar NBTS.

Figure 11 shows a comparison of the \( V_T \) hysteresis response of recent-vintage Vendor A and Vendor B devices, measured at room temperature, as a function of cumulative stress time for a \(-15\,\text{V}, 175\,\text{°C}\) NBTS overstress. The most-recent-vintage Vendor A results from Fig. 10 are replotted in Fig. 11 on a slightly finer scale. The Vendor B device starts out with a larger \( V_T \) hysteresis, and also exhibits a low but steady rate of trap activation versus cumulative stress time, which is consistent with the results in Fig. 6. But it should again be noted that these are overstress NBTS conditions for these devices, especially for the Vendor B devices which are rated for only \(-6\,\text{V}\) at 175°C (see Table I).

Figure 12 shows the \( V_T \) hysteresis response of two different vintages of commercial SiC power MOSFETs from Vendor A and Vendor B, measured at room temperature, as a function of cumulative stress time for a \(+25\,\text{V}, 175\,\text{°C}\) PBTS. The most-recent-vintage Vendor A results from Fig. 10 are replotted in Fig. 12. TheVendor B device starts out with a larger \( V_T \) hysteresis, and also exhibits a low but steady rate of trap activation versus cumulative stress time, which is consistent with the results in Fig. 6. But it should again be noted that these are overstress NBTS conditions for these devices, especially for the Vendor B devices which are rated for only \(-6\,\text{V}\) at 175°C (see Table I).

Figure 13 shows a comparison of the \( V_T \) hysteresis response of recent-vintage Vendor A and Vendor B devices, measured at room temperature, as a function of cumulative stress time for a \(+25\,\text{V}, 175\,\text{°C}\) PBTS.
measured at room temperature, as a function of cumulative stress time for a +25 V, 175 °C PBTS overstress. The most-recent-vintage Vendor A results from Fig. 12 are replotted in Fig. 13 on a much finer scale. Although the Vendor B device starts out with a larger $V_T$ hysteresis, it exhibits no increase in oxide-trap activation versus cumulative stress time, whereas the most-recent-vintage Vendor A devices show a slight increase. This is generally consistent with the $V_T$ shift results in Fig. 9.

In comparing the $V_T$ hysteresis results shown in Figs. 11 and 13, it is observed that the Vendor B devices have a larger initial number of active near-interfacial oxide traps present than the latest-vintage Vendor A devices. The Vendor A devices exhibit a little bit of additional oxide-trap activation under both NBTS and PBTS, whereas the Vendor B devices vary with the polarity of the stress. They are rock solid under PBTS, but show a noticeable increase under NBTS, consistent with the $V_T$ shift results shown in Figs. 9 and 6, respectively. It should also again be noted that the NBTS conditions were a significant overstress for the Vendor B devices, which are rated for only –6 V at 175 °C (see Table I).

5. Conclusions

We have characterized and compared three vintages of commercially-available SiC MOSFETs from one major manufacturer of these devices (Vendor A—including their most recent commercial devices), and the most recent devices from a second leading manufacturer (Vendor B), using an improved BTI test methodology. Whereas previous-vintage Vendor A devices exhibited large $V_T$ shifts under both NBTS (–15 V, 175 °C) and PBTS (+25 V, 175 °C) overstress conditions, along with significant increases in $V_T$ hysteresis, the most-recent-vintage commercially-available Vendor A devices show absolutely no negative $V_T$ shift during NBTS. This contrasts with a negative $V_T$ shift of just over 1 V for the latest-vintage Vendor B devices (earlier-vintage Vendor B devices were not compared). Under PBTS conditions, Vendor B devices fared better than the latest Vendor A devices, although both sets of devices had shifts well below than 1 V (0.25 and 0.60 V, respectively) during the 120h stress.

The latest-vintage Vendor A devices exhibited small levels of oxide-trap activation under both bias polarities determined by the $V_T$ hysteresis measurements, whereas the Vendor B devices were rock solid during PBTS, but did exhibit some noticeable activation during NBTS, consistent with the $V_T$ shift results.

These results are consistent with the notion that there are two dominant mechanisms affecting $V_T$ stability in SiC MOSFETs—oxide-trap activation, and oxide-trap charging via a direct tunneling mechanism.

We employed an improved reliability test method to evaluate the $V_T$ stability of these commercial devices. Improved test methods, especially those that include measurements at both room and elevated temperature and which minimize delay time following the removal of the bias stress, are needed to ensure that good devices have been successfully distinguished from bad devices.

Finally, it should be noted that although faster measurements (on the order of µs) will likely result in larger observed $V_T$ shifts, which are occurring during the bias stress, they likely will not affect the reliability of most applications employing these devices since they do not lead to increased leakage in the OFF state or increased resistance in the ON state.

26) A. Lelis, R. Green, D. Habersat, and M. El, presented at 2014 MRS Fall Meet.