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Breakdown mechanisms in AlGaN/GaN HEMTs: An overview

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This paper reviews the physical mechanisms responsible for breakdown current in AlGaN/GaN high electron mobility transistors (HEMTs). Through a critical comparison between experimental data and previously published results we describe the following mechanisms, which can be responsible for the increase in drain current at high drain voltage levels, in the off-state: (i) source–drain breakdown, due to punch-through effects and/or to a poor depletion of the buffer; (ii) vertical (drain-bulk) breakdown, which can be particularly prominent when the devices are grown on a silicon substrate; (iii) breakdown of the gate–drain junction, due either to surface conduction mechanisms or to conduction through the (reverse-biased) Schottky junction at the gate; (iv) impact ionization triggered by hot electrons, that may induce an increase in drain current due to the lowering of the barrier for the injection of electrons from the source. © 2014 The Japan Society of Applied Physics

1. Introduction

Thanks to the recent advancements in the growth and fabrication processes, the performance of high electron mobility transistors (HEMTs) based on GaN has significantly improved. The main advantages of using GaN as a material for the realization of HEMTs are (i) the high sheet charge density (>10¹¹ cm⁻²) of the two-dimensional electron gas (2DEG), which results in a low on-resistance of the transistors; (ii) the high thermal conductivity of GaN (>2 W cm⁻¹ K⁻¹), which permits to reach high levels of power dissipation while keeping the channel temperature low; (iii) the high breakdown field (3.3 MV/cm¹), which allows to fabricate devices with breakdown voltages in the order of hundreds or thousands of volts, depending on gate–drain spacing and on buffer thickness. These unique features make GaN an almost perfect material for the manufacturing of high power transistors: thanks to the recent efforts of the scientific and industrial communities, GaN-based transistors with breakdown voltages in excess of 1.5–1.9 kV have been recently demonstrated,²,³ thus clearing the way for the adoption of HEMTs in power electronics. Moreover, thanks to the low (on-resistance) × (device capacitance) product, GaN-based power HEMTs can reach high switching frequencies (>40 MHz²⁹), and can therefore be used for the fabrication of high efficiency power conversion systems: converters with efficiencies in excess of 96–98% have already been demonstrated,⁴,⁵ thus proving the superiority of GaN with respect to more conventional semiconductors for power electronics.

Despite the high performance of GaN-based HEMTs, the lifetime of these devices can be shorter than expected, due to the existence of a number of physical mechanisms responsible for device degradation. Recent studies demonstrated that GaN HEMTs may degrade due to the following processes: (i) degradation of the gate Schottky junction, induced by off-state stress.⁶–¹¹ This mechanism induces an increase in the gate leakage current, due to the generation of localized shunt paths in proximity of the gate edge; (ii) semi-permanent or permanent degradation due to hot electrons;¹²–¹⁴ this mechanism occurs when the devices are operated in the on-state, and—in most of the cases—results in a decrease in drain current, due to the accumulation of negative charge close to the gate edge and/or in the gate–drain access region.¹⁵ (iii) delamination of the passivation, due to the exposure to high temperature/power levels, which may result in additional charge trapping and leakage processes.¹⁶ (iv) time-dependent degradation processes.⁹ due to the generation of defects within the AlGaN/GaN heterostructure. Besides these mechanisms, power devices operated at high drain voltages may show important breakdown (BD) processes;⁹,¹⁷–²⁵ breakdown consists in a rapid increase in drain current, which occurs—in the off-state—when the drain voltage reaches a critical value. Breakdown may be catastrophic (i.e., induce a sudden failure of the devices); this typically happens when BD measurements are carried out in voltage controlled mode, by increasing the drain voltage until a un-controllable increase in drain current is triggered. A sustainable breakdown condition can be reached if the measurements are carried out in current-controlled mode;²⁵,²⁶ by using this method it is possible to separately evaluate the contribution of gate, source, and bulk leakage to the overall BD current, thus extracting information on the physical origin of breakdown for several operating conditions.

As can be understood, breakdown represents an important problem for high power/high voltage HEMTs: for this reason, over the past years several groups have investigated the physical origin of BD,⁹,¹⁷–²⁵ with the aim of developing models to explain this phenomenon, and of proposing technological improvements to increase the robustness of the devices. This paper reviews the physical mechanisms responsible for breakdown in GaN-based power transistors: to this aim, original results are compared with data taken from the literature. The following, relevant, breakdown mechanisms are discussed in detail:

- Source–drain breakdown, due to short-channel effects, and/or punch-through.
- The presence of relatively high breakdown current components at the gate, which can be either related to the leakage through the Schottky junction, or to surface-related conduction.
- Vertical breakdown, which can be due to a poor compensation of the buffer, to the use of a conductive substrate, and can be limited by the adoption of suitable back barrier or heterostructure configurations.
- Impact ionization mechanisms, that may induce a significant increase in drain current due to the generation of electron–hole pairs close to the gate.
2. Experimental methods

The original results described within this paper were obtained on AlGaN/GaN HEMTs, grown on silicon carbide or on silicon substrate by metal–organic chemical vapor deposition (MOCVD). For the investigation we used both devices with single heterostructure and HEMTs with double heterostructure (AlGaN/GaN/AlGaN); gate–drain spacing ranges between 2 and 10 µm, depending on the analyzed set of devices. Breakdown was characterized by means of drain current vs drain voltage ($I_D-V_D$) measurements, which were carried out in current-controlled mode (as described in Refs. 25 and 26), to avoid the catastrophic failure of the devices induced by the measurements. Electroluminescence (EL) was also used to investigate the luminescence mechanisms induced by hot electrons when the devices are operated in sustainable breakdown conditions.

The data collected within this paper were compared to the results present in the literature, to provide a critical review of the individual breakdown processes.

3. Results and discussion

3.1 Introductory considerations on sustainable breakdown measurements: $I_D-V_D$ curves and EL characterization

Figure 1 reports the typical results of current-controlled (sustainable) breakdown measurements, carried out at several gate voltage levels. The measurements were taken on AlGaN/GaN HEMTs grown on a silicon carbide substrate; the devices have a gate–source distance of 0.8 µm, a gate–drain distance of 4 µm, a gate length of 0.5 µm, and a gate width of 100 µm. The pinch-off voltage of these devices is equal to $-2.6$ V; the measurements were taken by means of a semiconductor parameter analyzer (Agilent E5260), with gate voltages between $-3$ and $-6$ V. From Fig. 1, several consideration can be made: (i) for all the analyzed gate voltages, drain current shows a remarkable increase when drain–source voltage ($V_{DS}$) becomes higher than $V_{BR} = 150$ V (breakdown voltage), indicating the existence of significant breakdown processes; (ii) for $V_{DS} < V_{BR}$ (i.e., below the breakdown voltage), drain current is almost equal to gate current, indicating that—for moderate $V_{DS}$ levels—drain current is dominated by gate–drain leakage; (iii) when gate voltage is close to the pinch-off [e.g., in the case $V_G = -3$ V, Fig. 1(a)], and for $V_{DS} > V_{BR}$, source current shows a strong increase, becoming significantly higher than gate current. As a consequence, breakdown (drain) current almost completely originates from drain–source leakage. Off-state drain–source conduction can be due to short-channel effects and/or punch-through of electrons from the source to the drain, due to the non-optimized depletion of the channel. These parasitic conduction processes, and the related remedies, are discussed in detail in Sect. 3.2. (iv) drain–source sub-threshold leakage can be almost completely suppressed by going towards more negative gate voltages [e.g., Fig. 1(d)], thanks to a better depletion of the buffer. In these conditions, breakdown (drain) current almost completely originates from gate–drain leakage. The mechanisms responsible for gate–drain leakage and breakdown will be discussed in detail in Sect. 3.3.

When operated in sustainable breakdown conditions, HEMTs can emit a weak luminescence signal. A description of this mechanism is given in Fig. 2, which reports a false color image of the distribution of EL on device surface, together with the corresponding current-controlled $I_D-V_D$ curves. EL signal is emitted due to the relaxation of energetic electrons, which are accelerated by the high electric field. Several papers discussed the origin of EL in AlGaN/GaN HEMTs [27–32] according to Ref. 32, EL may be generated either due to intra- or inter-valley transitions (Fig. 3). In the first case, the electrons accelerated by the electric field reach a high-energy non-equilibrium condition, within the Γ valley; light emission occurs due to the relaxation of these hot electrons, via optical transitions which may involve phonons or ionized impurities. On the other hand, in the case of inter-valley processes, the accelerated electrons may acquire enough energy to be injected into the satellite valleys of the conduction band; this process is favored by the inelastic scattering with phonons. These electrons then relax towards the Γ valley, thus emitting photons (energy conservation is guaranteed by the interaction with optical phonons). As shown by the EL micrographs in Fig. 2, under sustainable breakdown conditions luminescence is emitted in proximity of localized spots; these regions may correspond to the presence of defects, where the injection of highly energetic electrons—and thus light emission—may be locally favored.

3.2 Drain–source sub-threshold leakage: physical origin and remedies

As described in Sect. 3.1, when AlGaN/GaN HEMTs are operated in the off-state, with a gate voltage relatively close
to the pinch-off voltage, breakdown current is dominated by drain–source (sub-threshold) leakage [see the case in Fig. 1(a)]. Drain–source leakage is strongly dependent on the voltage applied to the gate during the sustainable breakdown measurements [Figs. 1(a)–1(d)]; Fig. 4 gives a more quantitative description of the influence of gate-bias on the drain–source breakdown current in AlGaN/GaN HEMTs (same devices as in Fig. 1). For a drain bias of 160 V, drain–source current is almost completely suppressed by changing the gate voltage from $-3$ to $-6$ V (the pinch-off of this device is $-2.6$ V), i.e., by improving the depletion of the buffer with more negative gate voltages. These effects are particularly prominent on short-channel devices (with gate length $L_G < 1$ μm), and are usually ascribed to a poor depletion of the region under the gate, which results in current flow within the GaN buffer. In the channel beyond the gate, the current density is up to a factor of 100 higher than in the current loop beneath the gate. However, the contours in the channel are very closely spaced, because the channel is narrow, and appear as a solid black line in the figure. © 2006 IEEE. Reprinted with permission from Ref. 20.
channel region, whose thickness is limited to few tens of nanometers. A typical comparison of the breakdown properties of single- and double-heterostructure (SH and DH, respectively) devices is shown in Fig. 6, for devices with increasing gate–drain distance. The SH HEMTs have a 20 nm AlGaN barrier (with a 23% indium content), on top of a 2400 nm GaN buffer layer; in the case of DH HEMTs, the heterostructure consists in a 1840 Al5Ga95N buffer, a thin (15 nm) GaN channel layer, and an AlGaN barrier layer (thickness: 20 nm, Al content: 23%). The results in Fig. 6 indicate that—indisputably of the gate–drain distance—the devices with single heterostructure show a soft-breakdown, related to the existence of high drain–source punch-through components; this effect is significantly smaller for the DH devices, for which the (current-controlled) \( I_D - V_D \) curves show a significantly higher breakdown voltage, whose value increases linearly with the gate–drain distance (as extensively described in Ref. 33). Bidimensional simulations (see Fig. 7 and Ref. 24) indicate that the use of a double heterostructure can significantly improve the depletion of the buffer, thus reducing the electron density and limiting the punch through current components. The thickness of the GaN channel region must be carefully optimized with the aim of achieving both a high electron density in the 2DEG, and a good confinement of the electrons in the channel.

3.3 Gate-related breakdown current components

When the HEMTs are biased in the off-state, with a high drain voltage, the gate–drain junction is exposed to a high reverse-bias. In absence of drain–source leakage (i.e., if the gate voltage is sufficiently low to avoid punch-through current components, or in the case of DH devices) drain current is dominated by the reverse leakage of the gate Schottky junction [see for instance Fig. 1(b)]. Gate breakdown can be due to several mechanisms: Tan et al.17) discussed the role of surface gate–drain leakage in determining drain current breakdown. They suggested that surface states—created by defects or contamination—may generate a significant surface conduction, due to hopping. When the devices are in pinch-off, with a high drain bias, electrons can tunnel from the gate to these surface states, thus generating gate–drain leakage. Breakdown (i.e., a sudden increase in drain current) is reached due to thermal runaway, when the power dissipation at device surface exceeds a certain threshold (see Fig. 8).17) This kind of breakdown mechanism has a negative temperature coefficient, i.e., breakdown voltage decreases with increasing temperature. Surface leakage components can be reduced by adopting advanced passivation schemes: many groups are currently adopting in-situ (i.e., MOCVD or MBE) nitride as a passivation layer.34,35) this allows to reduce the reverse-gate leakage of several orders of magnitude, thus significantly improving the behavior of the devices in breakdown conditions. The role of surface states in the breakdown process was confirmed also.
by Saito et al.,\textsuperscript{36} they indicated that the presence of positive charge (e.g., due to nitrogen vacancies) at the AlGaN layer surface increases the electric field over the AlGaN barrier, thus favoring tunneling and impact ionization processes. As a consequence, leakage current (breakdown voltage) increases (decreases) with increasing concentration of charged defects at the surface of the AlGaN layer.

Even if the surface is carefully optimized, other mechanisms may significantly contribute to gate–drain leakage through the AlGaN barrier: the most relevant are defect-assisted tunneling,\textsuperscript{37} thermionic emission at the Schottky gate,\textsuperscript{35} Poole–Frenkel emission,\textsuperscript{37} and the existence of leakage paths due to the presence of extended defects.\textsuperscript{11} These leakage components can reduce the breakdown voltage of HEMTs; in general, gate-related leakage can be almost completely suppressed through the use of a metal–insulator–semiconductor (MIS) scheme as an alternative to the conventional Schottky-gate structure.\textsuperscript{38}

3.4 Vertical (bulk-related) breakdown

As described in the previous sections, gate- and source-related breakdown current components can be significantly reduced through the use of optimized device structures, i.e., MIS-HEMTs (for lowering gate-induced leakage current) and double heterostructure devices (for lowering drain–source punch-through). Devices with high gate–drain spacing can reach breakdown voltages in excess of 500–1000 V. Under these conditions, vertical (drain–bulk) leakage may become relevant. Figure 9 reports the current-controlled breakdown curves measured on a MIS-HEMT with gate–drain spacing of 10 μm; while drain–source and gate current are below the detection limit, the drain (breakdown) current originates entirely from vertical leakage.

These current components can be reduced by improving the insulating properties of the buffer: a simple and effective approach is to use AlGaN (instead of GaN) for the fabrication of the buffer layer.\textsuperscript{39} Since AlGaN has a bandgap higher than GaN, this results in an increase in the vertical breakdown voltage. Another possibility is to use thick GaN-buffer layers; Rowena et al.\textsuperscript{40} demonstrated that a significant improvement of the breakdown voltage can be obtained by increasing the thickness of the GaN buffer layer on which i-GaN is grown (Fig. 10). This is partly due to the fact that—with increasing buffer thickness—the density of dislocations (in GaN grown on a thick buffer) shows a significant decrease.

They demonstrated a breakdown field of 2.3 MV/cm (very close to the theoretical value of 3 MV/cm) for epilayers grown by MOCVD with a total thickness of 5.5 μm.

Another promising technique for reducing vertical leakage has been recently demonstrated for GaN HEMTs grown on n-SiC substrates.\textsuperscript{41} The idea is to split the vertical voltage drop between the nitride layers and the upper layers of the SiC substrate. Hilt et al.\textsuperscript{41} proposed to use Ar-implantation to render isolating the top-most part (some hundreds of nanometers) of the SiC substrate. The implantation-induced damage in the SiC crystal is still present after MOCVD nitride growth; dynamic properties of the HEMTs are not altered by this procedure. A breakdown voltage of 880 V was demonstrated with a gate–drain distance of 18 μm by means of this technique.

Lu et al.\textsuperscript{42} proposed to remove the Si substrate to further increase the breakdown voltage of the HEMTs; by transferring the HEMT on an insulating carrier wafer, such as polycrystalline AlN or glass, they demonstrated a significant reduction of vertical leakage conduction, and breakdown voltages in excess of 1500 V, by simply using HEMTs with a 2 μm total epilayer thickness. In case the substrate is removed, heat dissipation must be optimized through the use of carrier layers with high thermal conductivity, such as polycrystalline aluminum nitride wafers. A similar approach was proposed by Herbecq et al.\textsuperscript{43} who were able to demonstrate a breakdown voltage of 1.9 kV (with a buffer thickness of less than 2 μm), after removing the substrate locally between gate and drain.

Another mechanism which can be responsible for vertical leakage was proposed in 2010 by Umeda et al.;\textsuperscript{44} they suggested that the blocking voltage of the HEMTs can be limited by the fact that a sheet of electrons is formed at the interface between GaN and the silicon substrate. This inversion layer can lead to a significant leakage current, at the edges of the devices. They proposed to implant acceptor atoms in the silicon wafer, to create two p⁺ regions in proximity of the edges of the transistor. This allows one to prevent the flow of electrons towards the edges of the devices, thus significantly reducing vertical leakage. The implanted regions (referred to as “channel stoppers”) permit to drastically increase the breakdown voltage; Umeda et al.\textsuperscript{44}
They showed that when they provided a quantitative description of this effect (see Fig. 11).

Most of the mechanisms described so far (gate–drain leakage, drain–source punch-through, vertical leakage, etc.) involve only electrons, which are the majority carriers in the weakly n-type GaN substrates, and can be injected from the gate, from the source, or from the bulk. Recent studies suggested that also holes generated through impact ionization may contribute to the breakdown of AlGaN/GaN HEMTs. A negative effect of the intrinsic n-type doping of the buffer is the DIBL; calculations indicate that the height of the barrier for the injection of electrons from the source to the buffer decreases with increasing depth. Recent studies suggested that—under off state conditions—the electrons can be injected from the source to the high-field region (gate edge on the drain side), thus initiating impact ionization in the channel. This may lead to a strong increase in drain current: Hanawa et al., based on bidimensional simulations, provided a quantitative description of this effect (see Fig. 11). They showed that when $V_{DS}$ is close to the breakdown voltage, impact ionization may occur in the region between gate and drain; this results in the generation of electron/hole pairs; as a consequence, the density of holes in the buffer layer can be very high ($>10^{15}$ cm$^{-3}$), particularly at the source side, where also the electron densities are high. The holes generated by impact ionization can flow into the buffer, and be captured by deep donors; this leads to a decrease in the negative space charge in the buffer, and to the reduction of the barrier for the injection of electrons to the GaN, thus resulting in a significant increase in drain current. Typically, if breakdown is due to impact ionization, $V_{DS}$ has a positive temperature coefficient; this is due to the fact that the electron mean free path, which is limited by phonon scattering, is shorter at higher temperatures. As a consequence, at high temperatures high electric fields are required to give to the electrons the energy required to reach impact ionization. In bi-dimensional simulations, the carrier generation rate due to impact ionization is usually expressed as

$$ G = \frac{\alpha_n |J_n| + \alpha_p |J_p|}{q}, $$

where $\alpha_n$ and $\alpha_p$ are the ionization rates for electrons and holes, $J_n$ and $J_p$ are the electron and hole current densities, and $q$ is the electron charge. $\alpha_n$ and $\alpha_p$ are expressed as

$$ \alpha_n = A_n \exp\left(\frac{-B_n}{|E|}\right), $$

$$ \alpha_p = A_p \exp\left(\frac{-B_p}{|E|}\right). $$

Here $E$ is the electric field, while $A_n$, $B_n$, $A_p$, $B_p$ are coefficients whose values can be deduced from the theoretical work by Bulutay. It is clear that to reduce the contribution of impact ionization to breakdown it is necessary to limit the electric field; this is possible through the use of suitable source-field plates, through the optimization of the dielectrics, and through an accurate design of gate head. It is worth noticing that, although possible at theoretical level, further work must be done to demonstrate the role of impact ionization in inducing the breakdown of AlGaN/GaN HEMTs. In GaAs devices impact ionization can be easily identified, since it generates a significant increase in gate current, and a measurable electroluminescence signal due to electron–hole recombination; on the other hand, in GaN-based transistors the contribution of impact ionization to gate current and band-to-band electroluminescence is significantly lower, and still has to be extensively described.

3.5 Breakdown and impact ionization

Most of the mechanisms described so far (gate–drain leakage, drain–source punch-through, vertical leakage, etc.) involve only electrons, which are the majority carriers in the weakly n-type GaN substrates, and can be injected from the gate, from the source, or from the bulk. Recent studies suggested that also holes generated through impact ionization may contribute to the breakdown of AlGaN/GaN HEMTs. A negative effect of the intrinsic n-type doping of the buffer is the DIBL; simulations indicate that the height of the barrier for the injection of electrons from the source to the buffer decreases with increasing depth. Recent studies suggested that—under off state conditions—the electrons can be injected from the source to the high-field region (gate edge on the drain side), thus initiating impact ionization in the channel. This may lead to a strong increase in drain current: Hanawa et al., based on bidimensional simulations, provided a quantitative description of this effect (see Fig. 11). They showed that when $V_{DS}$ is close to the breakdown voltage, impact ionization may occur in the region between gate and drain; this results in the generation of electron/hole pairs; as a consequence, the density of holes in the buffer layer can be very high ($>10^{15}$ cm$^{-3}$), particularly at the source side, where also the electron densities are high. The holes generated by impact ionization can flow into the buffer, and be captured by deep donors; this leads to a decrease in the negative space charge in the buffer, and to the reduction of the barrier for the injection of electrons to the GaN, thus resulting in a significant increase in drain current. Typically, if breakdown is due to impact ionization, $V_{DS}$ has a positive temperature coefficient; this is due to the fact that the electron mean free path, which is limited by phonon scattering, is shorter at higher temperatures. As a consequence, at high temperatures high electric fields are required to give to the electrons the energy required to reach impact ionization. In bi-dimensional simulations, the carrier generation rate due to impact ionization is usually expressed as

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$$ \alpha_n = A_n \exp\left(\frac{-B_n}{|E|}\right), $$

$$ \alpha_p = A_p \exp\left(\frac{-B_p}{|E|}\right). $$

Here $E$ is the electric field, while $A_n$, $B_n$, $A_p$, $B_p$ are coefficients whose values can be deduced from the theoretical work by Bulutay. It is clear that to reduce the contribution of impact ionization to breakdown it is necessary to limit the electric field; this is possible through the use of suitable source-field plates, through the optimization of the dielectrics, and through an accurate design of gate head. It is worth noticing that, although possible at theoretical level, further work must be done to demonstrate the role of impact ionization in inducing the breakdown of AlGaN/GaN HEMTs. In GaAs devices impact ionization can be easily identified, since it generates a significant increase in gate current, and a measurable electroluminescence signal due to electron–hole recombination; on the other hand, in GaN-based transistors the contribution of impact ionization to gate current and band-to-band electroluminescence is significantly lower, and still has to be extensively described.

4. Summary

In summary we have described the main mechanisms responsible for high breakdown current in AlGaN/GaN based HEMTs. The results described within this paper demonstrate that breakdown voltage (defined as the drain voltage required to reach a given drain current level) can be limited by the presence of a number of leakage mechanisms. At high drain bias, drain current may show a significant increase, due to (i) the punch-through of electrons injected from the source; (ii) the presence of high gate-leakage current components, due either to surface conduction, or to the tunneling of electrons through the AlGaN barrier; (iii) vertical conduction through the substrate, due to the use of conductive silicon substrates, to the intrinsic defectiveness of the buffer layer, or to the parasitic conduction mechanisms related to the presence of an inversion layer between the Si substrate and the nitrides; (iv) impact ionization, which may generate holes, thus locally decreasing the barrier for the injection of electrons from the source. These breakdown mechanisms have been discussed based on the data presented in the literature, and on original results. A hard degradation occurs due to positive-feedback mechanisms, such as thermal runaway or avalanche processes, for very high drain voltages.

The results described within this paper indicate that breakdown current can originate from a number of parasitic mechanisms, that—in most of the cases—can be limited.
or totally reduced, through a careful optimization of the procedures used for growth and processing. Methods for decreasing the source, gate, or bulk related current components are critically discussed in the text.

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Enrico Zanoni was born in Verona, Italy, in 1956. He received the Laurea degree in physics (cum laude) from the University of Modena and Reggio Emilia, Modena, Italy, in 1982, after a student internship with the S. Carlo Foundation, Modena. During 1985–1988, he was an Assistant Professor with the Faculty of Engineering, University of Bari, Bari, Italy. From 1988 to 1993, he frequently visited the U.S. and established research collaborations with Bell Laboratories; Hughes Research Laboratories; IBM T. J. Watson Research Center; Massachusetts Institute of Technology, Cambridge, MA, USA; TRW (currently, Northrop Grumman); University of California, Santa Barbara, CA, USA; and many other industrial and academic laboratories. During 1996–1997, he was a Full Professor of industrial electronics with the University of Modena and Reggio Emilia. He is currently with the University of Padova, Padua, Italy, where he was an Assistant Professor during 1988–1992, an Associate Professor of electronics during 1992–1993, a Full Professor of microelectronics during 1993–1996, and has been a Full Professor of digital electronics with the Department of Information Engineering since 1997. He has been a Representative of the University of Padova for the European project MANPOWER and Manufacturable Power Monolithic Microwave Integrated Circuits for Microwave Systems Applications, a European Coordinator for the subproject “Reliability” of the European project EUREKA PROMETHEUS (automotive electronics), a Principal Investigator of the European project “Procedures for the early phase evaluation of reliability of electronic components by the development of European Committee for Electrotechnical Standardization (CENELEC) Electronic Components Committee rules” on qualification and reliability of integrated circuits, and a European Coordinator of the subproject “Reliability” of the European Defence Agency project “Key Organization for Research on Integrated Circuits in GaN Technology”. He is nationally or locally responsible for several Italian research projects, such as the Italian Space Agency, the Italian Research Ministry Projects, and the Italian National Council of Research. He is the author or coauthor of approximately 450 papers in refereed international journals and conference proceedings, including more than 35 invited papers. His microelectronics group is composed of five professors, three assistant professors, and, on average, 15 Ph. D. students and two postdoctoral researchers. This research group publishes approximately 80 papers each year on a wide range of research topics, including analog and RF signal CMOS design, biochip development, the analysis of radiation hardness, and the reliability of electronic devices and circuits. His research interests include microelectronics, particularly concerning the design, characterization, reliability, and failure analysis of electronic devices and circuits.

Gaudenzio Meneghesso received the B.S. degree in electronics engineering, working on the failure mechanism induced by hot electrons in MSFET and HEMTs, and the Ph. D. degree in electrical and telecommunication engineering from the University of Padova, Padova, Italy, in 1992 and 1997, respectively. In 1995, he was with the University of Twente, Enschede, The Netherlands, with a Human Capital and Mobility fellowship (within the SUSTAIN Network) working on the dynamic behavior of protection structures against electrostatic discharge (ESD). Since 2011, he has been a Full Professor with the Department of Information Engineering, University of Padova. He has published about 600 technical papers, of which more than 60 are invited papers and eight have won Best Paper Awards at the 1996, 1999, 2007, and 2009 European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) and at the 2006 Electrical Overstress/Electrostatic Discharge Symposium. His research interests include electrical characterization, modeling, and reliability of microwave and optoelectronic devices on III–V and III–N; electrical characterization, modeling, and reliability of RF MEMS switches for reconfigurable antenna arrays; development of ESD protection structures for CMOS and SmartPower integrated circuits; and the characterization and reliability of organic semiconductor devices. Dr. Meneghesso was the recipient of the Italian Telecom award for his thesis work in 1993. For several years, he has served on the Executive Committee of the IEEE International Electron Devices Meeting as the European Arrangements Chair in 2006 and 2007. He has been serving on the Technical Program Committee (TPC) of the IEEE International Reliability Physics Symposium since 2005 and on the Management Committee since 2009. He is in the Steering Committee of several international conferences, including the European Solid-State Device Research Conference, the ESREF, the Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE), and the European Workshop on Heterostructure Technology (HETECH), and has been serving on the TPC of several international conferences. Since 2007, he has been an Associate Editor of the IEEE ELECTRON DEVICES LETTERS for the compound semiconductor devices area. He has been nominated to IEEE Fellow Class 2013, with the following citation: “for contributions to the reliability physics of compound semiconductor devices”. In 2010, he joined the Administrative Committee of the IEEE Electron Devices Society.