Crystalline In–Ga–Zn–O FET-based configuration memory for multi-context field-programmable gate array realizing fine-grained power gating

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Crystalline In–Ga–Zn–O FET-based configuration memory for multi-context field-programmable gate array realizing fine-grained power gating

Munehiro Kozuma1, Yuki Okamoto1, Takashi Nakagawa1, Takeshi Aoki1, Masatake Ikeda1, Takeshi Osada1, Yoshiyuki Kurokawa1, Takayuki Ikeda1, Naoto Yamade1, Yutaka Okazaki1, Hidekazu Miyain1, Masahiro Fujita2, Jun Koyama1, and Shunpei Yamazaki1

1Semiconductor Energy Laboratory Co., Ltd., Atsugi, Kanagawa 243-0036, Japan
2VLSI Design and Education Center (VDEC), University of Tokyo, Bunkyo, Tokyo 113-0032, Japan

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A multi-context (MC) field-programmable gate array (FGPA) enabling fine-grained power gating (PG) is fabricated by a hybrid process involving a 1.0 μm c-axis aligned crystalline In–Ga–Zn–O (CAAC-IGZO) field-effect transistor (FET), which is one of CAAC oxide-semiconductor (OS) FETs, and a 0.5 μm complementary metal oxide semiconductor (CMOS) FET. The FPGA achieves a 20% layout area reduction in a routing switch and an 82.8% reduction in power required to retain data of configuration memory (CM) cells at 2.5 V driving compared to a static random access memory (SRAM)-based FPGA. A controller for fine-grained PG can be implemented at an area overhead of 7.5% per programmable logic element (PLE) compared to a PLE without PG. For each PLE, the power overhead with fine-grained PG amounts to 2.25 and 2.26 nJ for power-on and power-off, respectively, and break-even time (BET) is 19.4 μs at 2.5 V and 10 MHz driving. © 2014 The Japan Society of Applied Physics

1. Introduction

Multi-context (MC)1 field-programmable gate arrays (FPGAs) switch between its circuit configurations quickly, and fine-grained FPGAs consisting of small programmable logic elements (PLEs) show flexibility when switching circuit configurations. A combination of these configurations is expected to be promising. However, MC-FPGAs require more than one set of configuration memory (CM) cells and fine-grained FPGAs require a relatively large number of CM cells. Accordingly, the circuit area and power consumption of these cells inevitably increase significantly in a static random access memory (SRAM)-based MC-FPGA with a fine-grained configuration.2,3 Power gating (PG) can be reduced power consumption more effective when performed in individual fine-grained units. However, fine-grained power gating requires a complex controller, causing non-negligible area overhead and thus hindering its implementation.4 An SRAM-based FPGA is required to perform a configuration operation each time it is powered on because SRAM is volatile. The use of nonvolatile memory such as magneto-resistive random access memory (MRAM) or flash memory as the CM can eliminate the configuration operation each time the FPGA is powered on; however, special rewriting circuits are required for this purpose to lead to other issues such as high power for data rewriting and an increased circuit area.5–7

C-axis aligned crystalline In–Ga–Zn–O (CAAC-IGZO) field-effect transistors (FETs), which are one of CAAC oxide-semiconductor (OS) FETs, have attracted a great deal of attention because of their extremely low off-state current and display applications.8–14 Furthermore, CAAC-IGZO FETs have been employed in LSIs such as a central processing unit (CPU),15 nonvolatile oxide semiconductor random access memory (NOSRAM),16 and an image sensor17 fabricated by a hybrid process involving CAAC-IGZO FET and complementary metal oxide semiconductor (CMOS) FET. Moreover, CAAC-IGZO FET-based nonvolatile memory incorporated in CM of an FPGA can eliminate a configuration operation each time the FPGA is powered on and also the FPGA is confirmed to realize faster operating speed.18,19

This study shows that a CAAC-IGZO FET-based CM works well for an MC-FPGA and effectively enables fine-grained PG through concurrent context switch and PG on non-active (NA) PLEs. The first advantage of such a configuration is that the use of CAAC-IGZO-FET-based CM can suppress an increase in power for retaining data and can constitute more than one CM cell set. The FPGA achieves an 82.8% reduction in power required to retain data of the CM cells at 2.5 V driving compared to an SRAM-based FPGA. The second advantage is that the incorporation of these CM cells into PLEs can simplify a controller for fine-grained PG. The controller, which utilizes a power switch (PSW), can be implemented at an area overhead of 7.5% per PLE. For each PLE, the power overhead with fine-grained PG amounts to 2.25 and 2.26 nJ at 2.5 V and 10 MHz for power-on and power-off, respectively.

This paper is organized as follows: the overview of the CAAC-OS technology is described in Sect. 2. The structure of our MC-FPGA is explained in Sect. 3 and the evaluation results of our prototype chip are shown in Sect. 4. Finally, the paper is concluded in Sect. 5.

2. Overview of CAAC-OS technology

Kimizuka et al. of National Institute for Research in Inorganic Materials (NIRIM) solved the structure of homologous IGZO crystals using the general formula InGaOz(ZnO)m (m is a natural number).20–23 Nomura et al. reported the thin-film transistor characteristics of single crystalline IGZO obtained by high-temperature treatment at 1400 °C.24,25

CAAC-OS is an oxide semiconductor including crystals aligned along the c-axis. As indicated in the cross-sectional transmission electron microscope (TEM) image shown in Fig. 1, the crystals are aligned along the c-axis in CAAC-IGZO films. In this figure, arrows represent a–b planes of the film and show that these a–b planes are aligned parallel to the cross-section. Therefore, these CAAC-OS films can achieve highly reliable FETs because of their high crystallinity.26

The MC-FPGA is fabricated by a hybrid process involving a 1.0 μm CAAC-IGZO FET and a 0.5 μm CMOS FET.16,17 Figure 2 shows the drain current–gate voltage (Ig–Vg)
characteristics of a CAAC-IGZO FET with a channel length \( L \) /channel width \( W \) of 1 \( \mu \)m/4 \( \mu \)m and a gate insulator (GI) thickness of 20 nm. The electron field-effect mobility \( \mu_{FE} \) and subthreshold swing \( S \) of the CAAC-IGZO FET are 7.4 cm\(^2\)/V·s and 93 mV/dec, respectively. The reported off-state current of a CAAC-IGZO FET with a gate length of 3 \( \mu \)m at 85 °C is \( 5 \times 10^{-23} \) A/\( \mu \)m, which is well below the measurement limit of a semiconductor parameter analyzer (\( 10^{-17} \) A/\( \mu \)m).\(^27\) This extremely low off-state current is an important factor in the basic configuration of the MC-FPGA.

Figure 3 shows the \( I_d-V_g \) characteristics of both n-channel (NMOS) and p-channel metal oxide semiconductor (PMOS) FETs \( (L/W=0.5 \mu \mathrm{m}/1 \mu \mathrm{m} \text{ and } \text{GI thickness}=10 \text{nm}) \). The electron field-effect mobilities of NMOS and PMOS FETs are 340 and 200 cm\(^2\)/V·s, respectively, and their subthreshold swings are 63 and 62 mV/dec, respectively. The on-/off-state current ratio \( (I_{on}/I_{off}) \) of each FET exceeds \( 10^{9} \) and their off-state current reaches approximately \( 10^{-12} \) A/\( \mu \)m.

In the MC-FPGA, the CAAC-IGZO FET only contributes to controlling configuration data writing to the CM, while the CMOS FET performs normal circuit operations. Thus, the drive capability of the CAAC-IGZO FET does not directly affect the operating speed of the FPGA, which can be enhanced by the CMOS FET. The extremely low off-state leakage current of the CAAC-IGZO FET is effective in improving the CM data retention.

3. Design

3.1 MC-FPGA

Figures 4(a) and 4(b) show a photograph of the 4465 × 2950 \( \mu \)m\(^2\) MC-FPGA die along with and its block diagram of the MC-FPGA, respectively. The MC-FPGA consists of 20 PLEs, 20 input/output (I/O) circuits, multipath gates (MPGs) for controlling connections between the PLEs or the PLE and the I/O circuit, word and bit drivers for configuration, and a configuration controller. The main circuits of the MC-FPGA are described below.

Figures 5(a) and 5(b) show the circuit diagram and the micrograph of an MPG used as a routing switch, respectively. The path gate consists of a path transistor (M2) and a CM cell, which contains a CAAC-IGZO FET (M1) and a storage capacitor (C1). This path gate can achieve an approximately 20% layout area reduction in the MPG compared to an SRAM-based path gate. The off-state current of M1 is extremely low; thus, the gate of M2 becomes floating when M1 is turned off. A capacitance of the capacitor C1 is 184 fF, which corresponds to the retention time exceeding 10 years when the leakage current of the CAAC-IGZO FET at 85 °C is \( 5 \times 10^{-23} \) A/\( \mu \)m. Consequently, the CM cell can be regarded as a nonvolatile memory in which voltage is maintained in C1, and does not consume power during data retention. The conduction between MPG input and output is determined by the voltages of C1 and one of the two transistors M3 present in the context selector selected by Cline[1:0]. The fine-grained MC-FPGA configuration is more advantageous than the SRAM-based MC-FPGA because the SRAM-based MC-FPGA requires a relatively larger area and higher power for data retention when the circuit expands.

The circuit diagram and the micrograph of a multi-configuration memory (MCM) cell used as a CM cell of the PLE are shown in Figs. 6(a) and 6(b), respectively. As in the MPG, the CM cell can be considered as nonvolatile memory in which voltage is maintained in C1, and does not consume...
power during data retention. The MCM cell generates output in accordance with the voltage of C1. Cline[1:0] select one of the two transistors M3 in the context selector, allowing the MCM to output from one of the two CM cells.

In the MPG and the MCM, data is written to the CM cells by controlling the write transistor M1 through output lines Wline[1:0] driven by the word driver and supplying configuration data through output lines Bline and Blineb driven by the bit driver. Unlike a high-voltage driver as observed in flash memory or a high-current driver as observed in MRAM, these CM cells can use a driver similar to that in SRAM.

Figures 7(a) and 7(b) show block diagrams of PLEs. In these PLEs, PG is performed on all logic circuits, such as flip-flops and a look-up table (LUT), except MCMs. Each of the PLE consists of 32 MCMs and functions equivalent to ordinary logic elements, and, one MCM supplies data as a control signal to the PSW gate. Therefore, the PSW can be controlled in each PLE by controlling this MCM using global signals Cline[1:0] for context switch. Furthermore, a controller for PG can be achieved by adding the PSW at an area overhead of 7.5% per PLE. Because the power required for context switch is independent of PG, the net PG-induced power overhead only corresponds to the energy for charging and discharging the PSW gate voltage. Thus, the MC-FPGA can easily perform fine-grained PG.

Fig. 5. (Color online) (a) Circuit diagram and (b) micrograph of a MPG (L and W units: µm). Bline is a data signal line and Wline[1:0] are control signal lines of selection transistors M1. The path gate contains a CM cell and the on and off states of a path transistor M2 is determined using the voltage of a storage capacitor C1. Cline[1:0] select one of the transistors M3 in the context selector. In Fig. 5(b), the dotted line marks the MPG and the broken line delimits the path gate.

Fig. 6. (Color online) (a) Circuit diagram and (b) micrograph of a MCM cell (L and W units: µm). Bline is a data signal line and a Blineb is an inversion data signal line. Wline[1:0] are the control signal lines of selection transistors M1. The on and off states of the transistors M2 are determined using the voltage of the storage capacitor C1. The CM cell outputs one of GND and VDD. Cline[1:0] select one of the transistors M3 in the context selector. In Fig. 6(b), the dotted line marks the MCM and the broken line marks the CM cell.
Out[0] are signals corresponding to divider outputs. Out[0] is an external asynchronous input signal for context switch, and a quarter divider at 2.5 V and 10 MHz driving. Cext is an when the circuit con

First, the context switch operation of the MC-FPGA is

4. Results and discussion

4.1 Performance evaluation of MC-FPGA

The MC-FPGA consists of 20 PLEs, two sets of context data, and 7.52 kbits of CM cells, which are distributed among MPGs (6.08 kbits), PLEs (1.28 kbits), and I/O circuits (0.16 kbits).

The power required for data retention in CM cells (power in the CM cell and the CM driver) at 2.5 V driving is estimated to be 92 nW for this MC-FPGA by SPICE simulation. In contrast, the power required for data retention in the CM cells is estimated to be 534 nW for an SRAM-based MC-FPGA having the same configuration, suggesting that the MC-FPGA reduces this power requirement by 82.8%. Because power consumption of the CM cells is expected to be relatively higher in the SRAM-based FPGA than that in the MC-FPGA when the circuit expands and the number of CM cells increases, this MC-FPGA is more advantageous than the SRAM-based FPGA.

The power required for data writing in the CM cells estimated by SPICE simulation at 2.5 V and 10 Mbps is 18.8 µW and 15.7 µW for the MC-FPGA and the SRAM-based FPGA, respectively. These calculations indicate that the MC-FPGA requires approximately 20% more power to perform configuration than the SRAM-based MC-FPGA. However, the CAAC-IGZO FETs provide a nonvolatile CM to the MC-FPGA, eliminating the need for a configuration operation each time the MC-FPGA is powered on. Specifically, if an SRAM MC-FPGA is applied to a device that is not frequently supplied with power to reduce power consumption, such as a mobile device, it consumes power for data writing each time the power supply is restarted. In contrast, if the MC-FPGA is applied to a mobile device, it infrequently consumes power for data writing, and thus, a substantial increase in power consumption is negligible.

4.2 Configuration memory

The MC-FPGA consists of 20 PLEs, two sets of context data, and 7.52 kbits of CM cells, which are distributed among MPGs (6.08 kbits), PLEs (1.28 kbits), and I/O circuits (0.16 kbits).

Next, the power consumption of MC-FPGAs is measured for various configurations to determine the power reduction induced by fine-grained PG. In a configuration without PG, 5 PLEs form a shift register (SR), and PG is not performed on the other 15 NA PLEs. These NA PLEs are of little relevance to substantial circuit operations. In a configuration with PG, 5 PLEs form an SR, and PG is performed on other 15 NA PLEs. The input signals of these NA PLEs are fixed to ground (GND) by setting the configuration data. Pulse signals are circulated in the five-stage shift registers at 2.5 V and 10 MHz driving during the power consumption measurements. The MC-FPGA power consumptions are 4.3863 and 4.1248 mW without and with PG, respectively. The ratios of the PLE power consumption to the total MC-FPGA power consumption is estimated by SPICE simulation under the same conditions. These ratios amounted to 0.35841 and 0.00153% without and with PG, respectively. Accordingly, the PLE power consumptions are 15.721 µW and 63 nW.

Fig. 7. (a) Programmable logic element block diagram and (b) PG area circuit diagram.

Fig. 8. (Color online) Switch operation waveforms of the fabricated chip in one clock (100 ns). Cext is an external asynchronous input signal for context switch, and Out[2:0] are signals output from a counter. A half divider is formed at 0 ns, and the external input signal Cext is changed at 355 ns. At 400 ns, internal signal Cline[1:0] are changed in synchronization with a clock rise. At 500 ns, an Out[0] is not counted up and a quarter divider is obtained. The quarter divider operates after 500 ns.

Clock

Reset

Datain[4:0]

Fig. 8. (Color online) Switch operation waveforms of the fabricated chip in one clock (100 ns). Cext is an external asynchronous input signal for context switch, and Out[2:0] are signals output from a counter. A half divider is formed at 0 ns, and the external input signal Cext is changed at 355 ns. At 400 ns, internal signal Cline[1:0] are changed in synchronization with a clock rise. At 500 ns, an Out[0] is not counted up and a quarter divider is obtained. The quarter divider operates after 500 ns.
4.2 Estimation of power overhead

The electric energy for changing the configuration without PG to the configuration with PG is examined in detail by SPICE simulation as power overhead due to PG. Simulated time-dependent changes in power induced by PG at 2.5 V and 10 MHz driving at power-off and power-off are shown in Figs. 9(a) and 9(b), respectively. The main factor contributing to the power overhead due to PG is the power used for controlling the context signals (Cline[1:0]) and the PSW. The internal signals Cline[1:0] start to change at 0 ns and power-off and power-off occur after 75 and 45 ns, respectively. The PE is considered powered on/off when the PSW is correctly turned on or off or when the PSW gate voltage reaches the threshold voltage of the PMOS FET (0.67 V). The configuration data ensures that signals output from NA PLEs subjected to PG are not used in other operating PLEs. Consequently, even if the time required for power-off is finite, it does not affect circuit operations. The electric energy required to control the context signal is 0.98 and 0.99 nJ at power-on and power-off, respectively, while the electric energy required to control the NA PLEs is 1.27 and 1.27 nJ at power-on and power-off, respectively. As a result, the power overhead due to power-on and power-off is 2.25 and 2.26 nJ, respectively. The standby power of the NA PLEs is 232 µW. Break-even time (BET) at which the PG power overhead required to control the context and the NA PLEs at power-on and power-off becomes equal to the standby power of the NA PLEs without PG is 19.4 µs. From these results, BETs of 138.2, 36.4, and 23.7 µs are obtained when 1, 5, and 10 NA PLEs are subjected to PG, respectively. As the number of NA PLEs subjected to PG increases, the rate of electric energy required to control the context signal in power overhead can decrease; thus, the BET becomes shorter.

5. Conclusions

An MC-FPGA is fabricated by a hybrid process involving a 1.0 µm CAAC-IGZO FET and a 0.5 µm CMOS FET. The CAAC-IGZO FET-based CM achieves a 20% layout area reduction in an MPG and an 82.8% reduction in power required for data retention of the CMs compared to an SRAM-based MC-FPGA. These area and power reductions facilitate the implementation of a fine-grained configuration. A fine-grained MC-FPGA is combined with fine-grained PG performed on PLEs, an MCM is used as a PG controller part, and concurrent context switch and PG are performed on NA PLEs. Fine-grained PG can be easily performed by adding a PSW at an area overhead of 7.5% per PLE. Power overheads of 2.25 and 2.26 nJ due to PG are obtained at power-on and power-off, respectively, and the BET is 19.4 µs at 2.5 V and 10 MHz driving.

Fig. 9. (Color online) Power overhead in PG operations: (a) in power-off and (b) in power-on. Each data point represents a 200 ns moving average. "Context signal with PG", "NA PLEs with PG", and "NA PLEs without PG" represent the power required to control the context signal in the PG configuration, the power required by the 15 NA PLEs in the PG configuration, and the power required by the 15 NA PLEs in the PG-free configuration, respectively.


