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To cite this article: Sang Ho Lee *et al* 2023 *Jpn. J. Appl. Phys.* **62** SC1016

Japanese Journal of Applied Physics **62**, SC1016 (2023) **REGULAR PAPER**
https://doi.org/**10.35848/1347-4065/acaca9**

Bulk-fin field-effect transistor-based capacitorless dynamic random-access memory and its immunity to the work-function variation effect

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Received October 20, 2022; revised December 13, 2022; accepted December 18, 2022; published online January 10, 2023

In this study, we developed a capacitorless dynamic random-access memory (DRAM) (1T-DRAM) device based on a junctionless (JL) bulk-fin field-effect transistor structure with excellent reliability and negligible variability against work-function variation (WFV). We investigated the variation in the transfer characteristics and memory performance of the memory cell owing to WFV. In particular, to investigate the WFV effect, we analyzed the transfer characteristics and memory performance of 200 samples using four metal-gate materials—TiN, MoN, TaN and WN. Consequently, we discovered that the WFV affected the transfer characteristics of the JL bulk-fin field-effect transistor. However, the proposed 1T-DRAM demonstrated that the sensing margin and retention time produced minimal effect owing to the adoption of a structure storing holes in the fin region. Consequently, the proposed 1T-DRAM exhibited strong WFV immunity and excellent reliability for memory applications.

1. Introduction

Recently, the high-κ/metal-gate (HK/MG) technology has been widely used in industries owing to its excellent gate controllability.[1–6] The HK/MG technology can suppress the short-channel effect and address the gate leakage current issue caused by thin gate oxides, which presents a problem in conventional SiO_2 transistors.[7–11] Thus, metal-gate materials such as TiN, MoN, TaN and WN are used instead of poly-Si gates. However, depending on the grain orientations of metals, they have probabilistically different work-function (WF) values.[12–19] Thus, the grain orientation of a metal gate causes a work-function variation (WFV), thereby affecting the transfer characteristics including the threshold voltage (V_{th}), subthreshold swing (*SS*), on-current (I_{on}) and off-current (I_{off}). This side effect is one of the critical issues encountered in the implementation of the HK/MG technology, and it not only affects logic transistors but also influences memory transistors.[20–25] So far, a few studies on WFV have been reported in the literature;[12–19] however, the impact of WFV on memory characteristics is yet to be investigated. Recently, Lee et al. studied and investigated the effect of WFV on the transfer characteristics and memory performance of a gate-all-around junctionless (JL) field-effect transistor-based capacitorless dynamic random-access memory (1T-DRAM).[20] In the aforementioned study, a long retention time of more than 10 ms was obtained. However, owing to the WFV, poor retention times of 0.051 ms and 2.2 ms were obtained. Nevertheless, studies on the effect of WFV are still limited, and no solution has yet been presented.

In this study, we simulated 200 samples of a 1T-DRAM based on JL bulk-fin field-effect transistor (FinFET) gate materials, such as TiN, MoN, TaN and WN, to demonstrate that the proposed 1T-DRAM devices exhibited excellent immunity to WFV. The proposed 1T-DRAM demonstrated that the sensing margin and retention time produced little effect owing to the fin structure.

2. Device structure and simulation method

Figure 1 presents a three-dimensional (3D) view and schematic cross-section of the JL bulk-FinFET-based 1T-DRAM. The gate length (L_g) is 20 nm, gate-to-source length (L_{gs}) is 30 nm, height of the channel fin (H_{fin}) is 30 nm, fin width (W_{fin}) is 10 nm, height of the body fin ($H_{body\text{-}fin}$) is 100 nm, gate dielectric (HfO_2) thickness (T_{ox}) is 2 nm, and metal grain size (G_{size}) is 5 nm. The doping concentrations of the source, channel, and drain regions are $1 \times 10^{20}\,cm^{-3}$ (*n*-type), $5 \times 10^{17}\,cm^{-3}$ (*n*-type) and $1 \times 10^{20}\,cm^{-3}$ (*n*-type), respectively. Table I summarizes the device parameters for each of the proposed devices. In our analysis, four different gate materials—TiN, MoN, TaN and WN—were simulated, and their properties are listed in Table II.

A Sentaurus technology computer-aided design (TCAD) simulation was used to investigate the transfer characteristics and memory performances.[26] For the accuracy of the TCAD simulation, various physical models such as the Shockley–Read–Hall recombination model, Auger recombination model, Fermi–Dirac statistical model, doping-dependent and field-dependent mobility models, nonlocal band-to-band tunneling model, trap-assisted-tunneling model, bandgap narrowing model, and quantum confinement model were considered.[26]

3. Results and discussion

3.1. Effect of WFV on transfer characteristics

Figure 2 presents an example of one of the 200 samples. The WF values of the grains in TiN, MoN, TaN and WN were randomly generated. To investigate the change in the transfer characteristics and memory performance owing to WFV, 200 sample gate materials were simulated and studied for JL bulk-FinFETs. The V_{th} values were extracted using the constant-current method at $100\,nA\ \mu m^{-1}$.[27–29]

Figure 3 presents the transfer curves of the 200 JL bulk-FinFET-based 1T-DRAM samples fabricated using the TiN, MoN, TaN and WN gate materials. Note that each metal

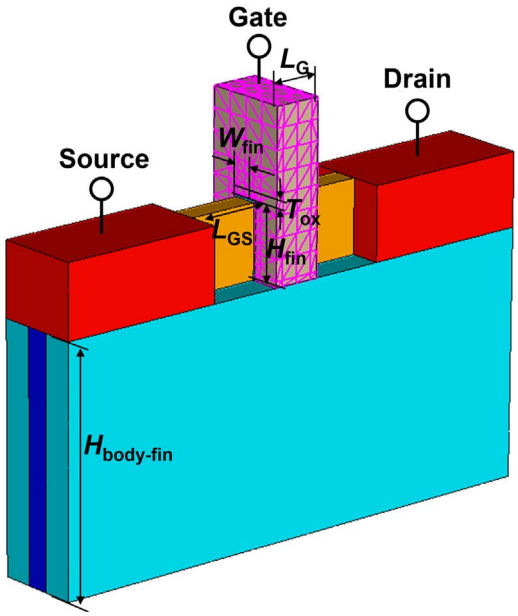

Fig. 1. (Color online) 3D schematic view of the proposed JL bulk-FinFET-based 1T-DRAM.

Table I. Device parameters of the proposed transistor used for simulations.

Parameters	Values
Gate length (L_g)	20 nm
Gate-to-source length (L_{GS})	30 nm
Height of the channel fin (H_{fin})	30 nm
Fin width (W_{fin})	10 nm
Body fin ($H_{body\text{-}fin}$)	100 nm
Gate dielectric (HfO_2) thickness (T_{ox})	2 nm
Gate work-function	—
Source/Drain doping concentration	n-type, 1×10^{20} cm^{-3}
Channel fin doping concentration	n-type, 5×10^{17} cm^{-3}
Body fin doping concentration	p-type, 2×10^{18} cm^{-3}
Substrate doping concentration	n-type, 1×10^{18} cm^{-3}

Table II. Physical properties of various metals.[12)]

Material	Orientation	Probability (%)	Work-function (eV)
TiN	⟨100⟩	60	4.6
	⟨111⟩	40	4.4
MoN	⟨110⟩	60	5.0
	⟨112⟩	40	4.4
TaN	⟨100⟩	50	4.0
	⟨200⟩	30	4.15
	⟨220⟩	20	4.8
WN	⟨111⟩	65	4.5
	⟨200⟩	15	4.6
	⟨220⟩	15	5.3
	⟨311⟩	5	4.2

material consists of two or more grains and each grain has a different WF value depending on the grain orientation. This phenomenon induces WFV in the JL bulk-FinFET-based 1T-DRAM samples. Therefore, the 200 samples presented different drain currents versus gate voltage (I_{ds}–V_{gs}) curves and V_{th}s. In addition, the larger the deviation in the grains' WF, the wider the dispersion of the graph, as depicted in Fig. 3. For example, TiN metal-gate transistors presented a narrow I_{ds}–V_{gs} distribution, whereas MoN metal-gate transistors demonstrated a relatively wide I_{ds}–V_{gs} distribution.

Figure 4(a) presents the mean values of the extracted V_{th}s of three metal-gate materials—TiN, MoN and WN. Their V_{th} values were 0.267 V, 0.479 V and 0.366 V, respectively. For the TaN metal gate, all the V_{th} values could not be extracted because all drain currents in the I_{ds}–V_{gs} curves were greater than 100 nA μm^{-1}, which was a reference value.[27–29)] The standard deviations (SDs) for the V_{th} values were 14.8 mV, 46.0 mV and 46.0 mV, respectively. The relative standard deviations (RSDs) were 5.43%, 8.83% and 12.6%, respectively. Note that the RSD is the SD divided by the mean and multiplied by 100. In other words, when the RSD is large, the SD and variance are greater than the average values. The units of RSDs are percentages, and the RSD is a coefficient that can be used to compare variances in datasets with different means.[4)] The RSD of the TiN metal-gate transistors was approximately half that of the MoN and WN metal-gate transistors. Therefore, TiN metal-gate transistors have better robustness against V_{th} variations resulting from WFV.

Figure 4(b) presents the distribution of the *SS*s of the three metallic materials. The means of the *SS*s for the three metal-gate transistors have similar values, 92.0 mv dec^{-1}, 85.6 mv dec^{-1} and 90.5 mV dec^{-1}, respectively. TiN metal-gate transistors have *SS*s in the 84.0–104.0 mv dec^{-1} range. However, the *SS*s of MoN and WN metal-gate transistors are in the 72.0–108.0 mv dec^{-1} and 80.0–108.0 mv dec^{-1} ranges, respectively. This phenomenon can be attributed to the fact that TiN metal-gate transistors have a narrow V_{th} distribution. However, the MoN and WN metal-gate transistors have a wide distribution of V_{th}. Therefore, the *SS* also follows the tendency of V_{th}.

Figure 4(c) presents the distribution of I_{on}s. The mean I_{on} values of TiN, MoN, TaN and WN metal transistors are 2.63×10^{-5} A μm^{-1}, 1.85×10^{-5} A μm^{-1}, 3.51×10^{-5} A μm^{-1} and 2.29×10^{-5} A μm^{-1}, respectively. The mean I_{on} values of the TaN metal-gate transistors appear greater than those of the TiN, MoN and WN metal-gate transistors; this is because the larger the WF of a metal gate, the higher the V_{th}. The effective WF for transistors is computed by using the following equation

$$\text{Effecitve } WF = \frac{x_1}{N} \times \Phi_{x1} + \frac{x_2}{N} \times \Phi_{x2} + \frac{x_3}{N} \times \Phi_{x3} + \cdots, \quad (1)$$

where x_i (i = 1 to N) is the probability value of the assigned grain orientation, N is the number of the grain, and Φ_{xi} is the *WF* value of the assigned grain orientation.[13)] The effective *WF* values for TiN, MoN, TaN and WN were found to be 4.52 eV, 4.76 eV, 4.205 eV and 4.62 eV, respectively. The higher the WF, the higher the value1 of V_{th}, which also implies a decrease in the I_{on} value. Therefore, I_{on} also follows the tendency followed by V_{th}.

Figure 4(d) presents the distribution of I_{off}. The I_{off} values of the TaN metal-gate transistors are the highest, followed by those of TiN metal-gate transistors, WN metal-gate transistors, and MoN metal-gate transistors, depending on the effective *WF*. The mean of I_{off} follows the tendency of the effective *WF*. The figures of merit (FOMs) of the transfer characteristics are summarized in Table III. As shown in Table III, the SD for MoN metal-gate transistors is greater than that for the TiN metal-gate transistors; notably, the larger the WF of the metal gate, the higher the V_{th}.

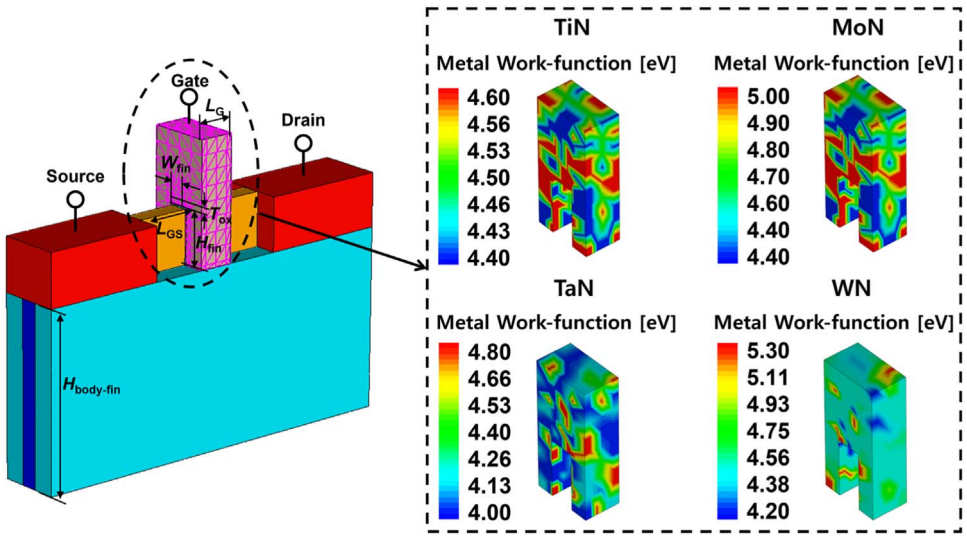

Fig. 2. (Color online) Examples depicting different orientations of grains in JL bulk-FinFET-based 1T-DRAM with TiN, MoN, TaN and WN gate materials.

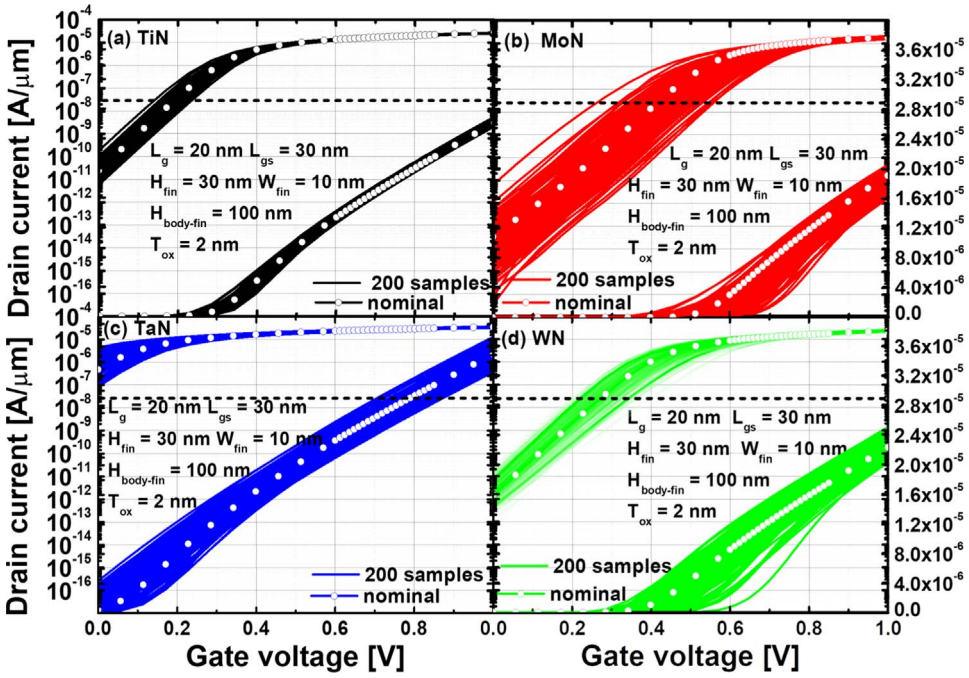

Fig. 3. (Color online) I_{ds}–V_{gs} curves of the 200 samples of bulk-FinFET with (a) TiN, (b) MoN, (c) TaN and (d) WN gate materials based on the HK/MG technology. The current is normalized by the total fin width ($W_{fin} + 2H_{fin}$).

3.2. Effect of WFV on memory performances

Figure 5(a) presents a contour map of the hole density in the proposed 1T-DRAM cell in states "1" and "0." Note that most 1T-DRAMs store holes in the body region near the metal gate.[20–25] However, the proposed JL bulk-FinFET-based 1T-DRAM device stores holes in $H_{body\text{-}fin}$ rather than H_{fin}, as shown in Fig. 5(a). Figure 5(b) presents the energy band diagram of the proposed 1T-DRAM cell in states "1" and "0." The energy band was extracted from the center of the channel. As depicted in Fig. 5(b), the electron potential energy in the bulk-fin region was lowered by the stored hole. Therefore, the storage region was located far from the metal gate and was not directly affected by the metal gate. Thus, the effect of WFV can be minimized using a structure that stores holes in $H_{body\text{-}fin}$. The operating bias of the 1T-DRAM is summarized in Table IV.

Figure 6 presents the memory performance of the 200 JL bulk-FinFET-based 1T-DRAM samples with TiN, MoN, TaN and WN. Although the sensing margins and retention times appear to be affected by the WFV, all samples are sufficient for RT to meet 64 ms, which is the memory criterion set by the international roadmap for devices and systems (>64 ms).[30,31] Consequently, we can conclude that the proposed JL bulk-FinFET-based 1T-DRAM is a reliable memory cell immune to WFV. The FOMs of the memory performance are summarized in Table V.

4. Conclusions

This paper presents the variations in transfer characteristics and memory performance caused by the WFV in the metal gate of a 1T-DRAM cell based on a JL bulk-FinFET. In Ref. 20, as mentioned above, owing to the WFV, poor

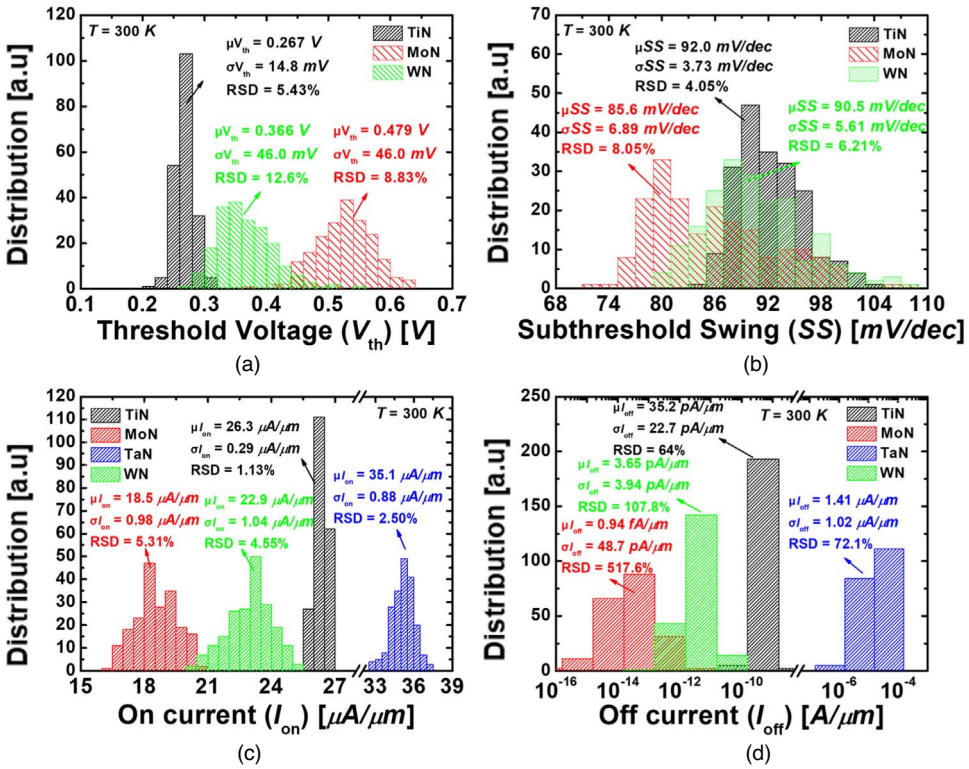

Fig. 4. (Color online) Histograms of the 200 samples of bulk-FinFET with (a) TiN, (b) MoN, (c) TaN and (d) WN gate materials based on the HK/MG technology.

Table III. Comparison between the mean, SDs and RSDs of the transfer characteristics of the bulk-FinFET 1T-DRAM with different gate metals: TiN, MoN, TaN and WN.

		TiN metal gate	MoN metal gate
Threshold Voltage (V_{th}) @ W/L × 10^{-7}	Mean	0.267 V	0.526 V
	SD	14.8 mV	46.0 mV
	RSD	5.43%	8.83%
Subthreshold swing (SS)	Mean	92.0 mV dec^{-1}	85.6 mV dec^{-1}
	SD	3.73 mv dec^{-1}	6.89 mv dec^{-1}
	RSD	4.05%	8.05%
On-current (I_{on}) @ V_{gs} = 1.0 V	Mean	2.63×10^{-5} A μm^{-1}	1.85×10^{-5} A μm^{-1}
	SD	2.98×10^{-7} A μm^{-1}	9.85×10^{-7} A μm^{-1}
	RSD	1.13%	5.31%
Off-current (I_{off}) @ V_{gs} = 0.0 V	Mean	3.52×10^{-11} A μm^{-1}	9.40×10^{-14} A μm^{-1}
	SD	2.27×10^{-11} A μm^{-1}	4.87×10^{-13} A μm^{-1}
	RSD	64%	517.6%
		TaN metal gate	WN metal gate
Threshold Voltage (V_{th}) @ W L^{-1} × 10^{-7}	Mean	—	0.366 V
	SD	—	46.0 mV
	RSD	—	12.6%
Subthreshold swing (SS)	Mean	—	90.5 mV dec^{-1}
	SD	—	5.61 mv dec^{-1}
	RSD	—	6.21%
On-current (I_{on}) @ V_{gs} = 1.0 V	Mean	3.51×10^{-5} A μm^{-1}	2.29×10^{-5} A μm^{-1}
	SD	8.78×10^{-7} A μm^{-1}	1.04×10^{-6} A μm^{-1}
	RSD	2.50%	4.55%
Off-current (I_{off}) @ V_{gs} = 0.0 V	Mean	1.41×10^{-6} A μm^{-1}	3.65×10^{-12} A μm^{-1}
	SD	1.02×10^{-6} A μm^{-1}	3.94×10^{-12} A μm^{-1}
	RSD	72.1%	107.8%

retention times were obtained. Unfortunately, studies on the effect of WFV on memory performances are still limited and no solution has yet been presented. However, our proposed fin-shaped structure can be a good candidate for immunity to WFV regarding memory performances. In our analysis, to investigate the WFV effect, we analyzed the transfer characteristics and memory performance of 200 samples using four metal-gate materials. Owing to the random distribution of the metal-gate grain orientation, the 200 samples presented different V_{th} values. However, the proposed 1T-DRAM

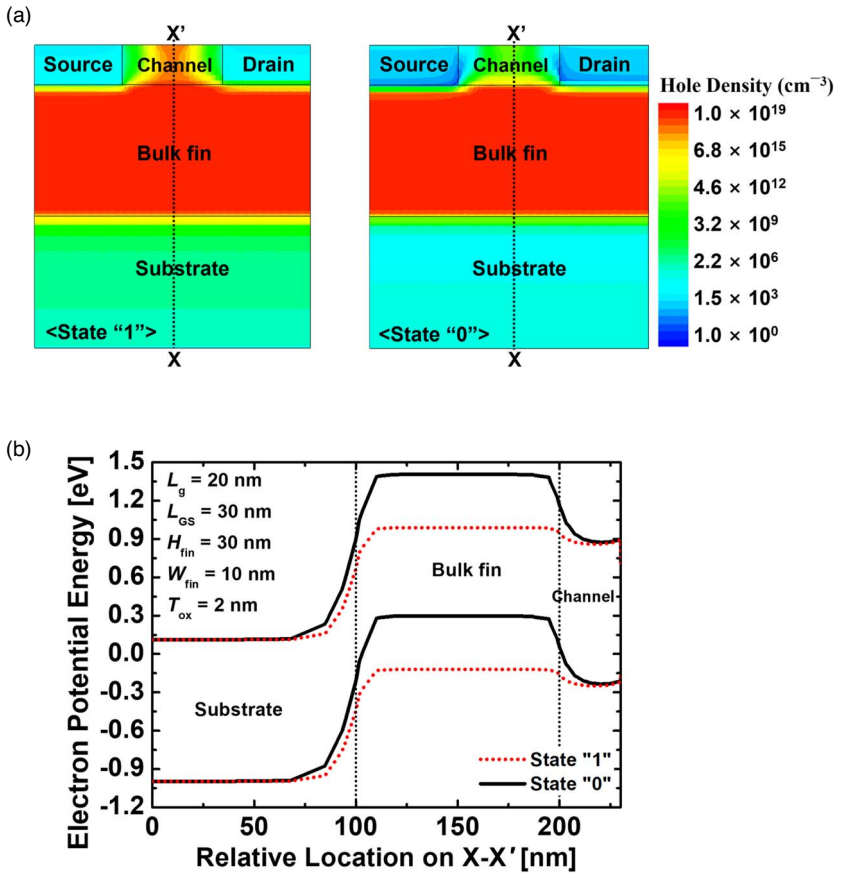

Fig. 5. (Color online) (a) Contour map of the hole density of the proposed 1T-DRAM cell in states "1" and "0." (b) Energy band diagram of the proposed 1T-DRAM cell in states "1" and "0." The energy band is extracted at the center of the channel.

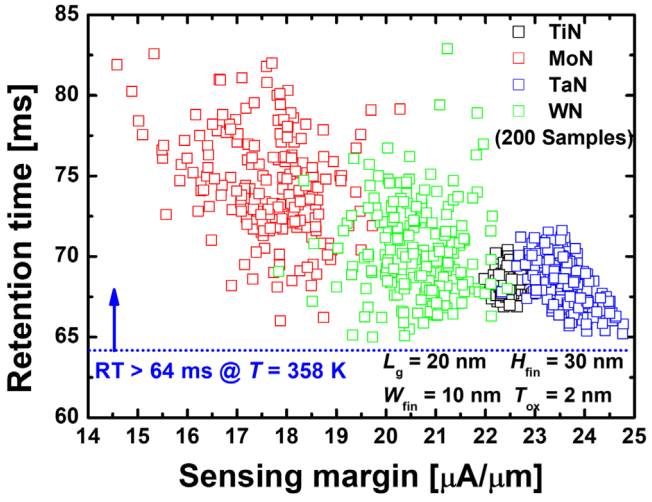

Fig. 6. (Color online) Comparison of retention time versus sensing margin for JL bulk-FinFET-based 1T-DRAMs with TiN, MoN, TaN and WN.

Table IV. Operating bias scheme for memory application analysis.

	Write "1"	Write "0"	Read	Hold
Gate voltage (V_{gs})	−2.0 V	0.0 V	1.0 V	0.0 V
Drain voltage (V_{ds})	1.5 V	−1.5 V	0.5 V	0.0 V
Substrate voltage (V_{sub})	0.0 V	0.0 V	0.0 V	0.0 V

indicated that the sensing margin and retention time produced minimal effect, owing to the adoption of a structure that stored holes in the fin region. Thus, the proposed 1T-DRAM is a bulk-FinFET structure with strong WFV immunity and excellent reliability for memory applications. Consequently, when designing 1T-DRAMs while simultaneously considering the WFV, the devices should be implemented with the JL bulk-FinFET structure.

Table V. Comparison between the mean, SDs and RSDs of the memory performance indicators of the bulk-FinFET 1T-DRAM with different gate metals: TiN, MoN, TaN and WN.

		TiN metal gate	MoN metal gate
Sensing margin	Mean	22.24 μA μm^{-1}	17.66 μA μm^{-1}
	SD	0.157 μA μm^{-1}	0.990 μA μm^{-1}
	RSD	0.69%	5.59%
Retention time	Mean	68.50 ms	74.47 ms
	SD	0.668 ms	3.19 ms
	RSD	0.98%	4.28%
		TaN metal gate	WN metal gate
Sensing margin	Mean	23.63 μA μm^{-1}	20.64 μA μm^{-1}
	SD	0.453 μA μm^{-1}	0.771 μA μm^{-1}
	RSD	1.92%	3.73%
Retention time	Mean	68.32 ms	70.37 ms
	SD	1.55 ms	2.91 ms
	RSD	2.26%	4.13%

Acknowledgments

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (No. NRF-2020R1A2C1005087). This study was supported by the BK21 FOUR project funded by the Ministry of Education, Korea (4199990113966). This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the

Ministry of Education (NRF-2021R1A6A3A13039927). This research was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (2021M3F3A2A03017764). This research was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (2022M3I7A1078936). This investigation was financially supported by Semiconductor Industry Collaborative Project between Kyungpook National University and SamSung Electronics Co. Ltd. The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

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