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Experimental and Numerical Studies on dV/dt Robustness of 1200 V High-Voltage Integrated Circuits Using Self-Isolation Structure

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Experimental results on the high-voltage level shifter and dV/dt robustness of 1200 V high voltage integrated circuits (HVICs) using a self-isolation (SI) structure are reported for the first time. Generally, because high dV/dt stress is applied to HVICs during insulated gate bipolar transistor (IGBT) switching, significant displacement current flows through a high-voltage isolation capacitance. This current acts as the base current of parasitic pnp and npn transistors, and causes a potential drop in their base region. In the worst case, this parasitic operation causes device destruction. In this study, not only the normal operation of HVICs but suppression of the parasitic transistors under high dV/dt condition are experimentally demonstrated by considering a high-side layout design and back diverter electrode. [DOI: 10.1143/JJAP.45.43]

KEYWORDS: HVICs, level shift, self-isolation, dV/dt, robustness, self-shielding, diverter

1. Introduction

Applications of high-voltage integrated circuits (HVICs) are expanding worldwide. In several motion control fields, low-voltage integrated circuits (LVICs) have started to be replaced with HVICs, because of the requirements of total system cost reduction and more accurate control. A typical block diagram of an insulated gate bipolar transistor (IGBT) gate driver is shown in Fig. 1. A high-side output signal for the IGBT gate is transmitted from the low-side level using a high-voltage level shifter. More accurate dead-time control between the high-side gate driver (GDUH) and low-side gate driver (GDUL) is possible by control logic compared with using an optocoupler and LVICs. Figure 2 shows the circuit configuration of a typical high-voltage level shifter using a high-voltage n-channel metal–oxide–semiconductor field effect transistor (MOSFET).

Among several high-voltage isolation structures, the self-isolation structure is the most cost effective in comparison with the conventional junction isolation structure and dielectric isolation structure.[1–4] This is because the initial wafer cost is low due to the use of simple uniformly doped p-type substrates and the complementary metal–oxide–semiconductor (CMOS) process is relatively simple.

Generally, HVICs have large parasitic capacitance due to their high voltage isolation structure not depending on isolation type, and high dV/dt stress is often applied to HVICs during IGBT switching. If the parasitic devices, such as a thyristor or a bipolar transistor, in HVICs are activated by the dV/dt stress, output failure or destruction of the HVICs might occur. It is considered that a typical dV/dt stress is approximately 5 kV/μs. Therefore, one of the most important tasks in HVICs design is to ensure sufficient robustness against the high dV/dt stress occurring in IGBT gate driver circuits, e.g., 30 kV/μs.

In the case of the SI structure, because the n-well region is connected to the emitter terminal of the high-side IGBT, significant displacement current flows through a depletion layer capacitance of the n-well/p-sub junction during IGBT switching. This current acts as a base current of parasitic devices in HVICs. In order to prevent HVICs from device destruction, potential drop in the n-well and p-sub region, induced by displacement current, should be minimized.

Regarding dV/dt robustness on HVICs, experimental results of 600-V-class devices using the SI structure have been reported.[5] Generally, the resistivity of the substrate for 1200-V-class devices is higher than that of 600-V-class devices, and the increase of resistivity has an adverse effect on dV/dt robustness. There has been a TEG level exper-

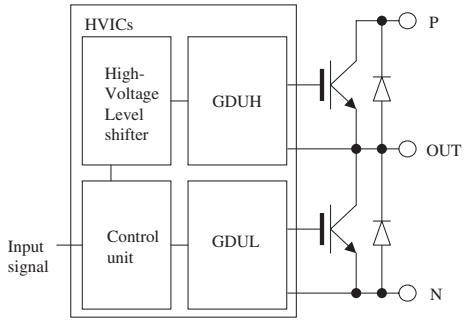


Fig. 1. Typical block diagram of HVICs with half-bridge configuration. GDUH: High-side gate driver unit, GDUL: low-side gate driver unit.

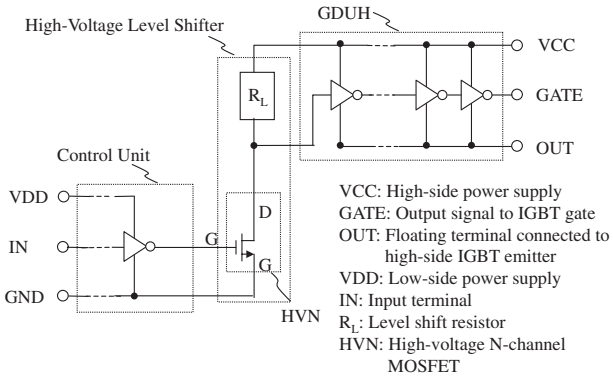


Fig. 2. Circuit configuration of typical high-voltage level shifter using HVN. The voltage drop in R_L is the input signal to GDUH.

imental report about 1200 V HVICs to date.[6] The purpose of our study is to improve the understanding of dV/dt robustness on 1200 V HVICs from the view point of suppressing the parasitic transistor operation.

2. Device Structure

Two categories of active devices are designed in this experiment, as shown in Fig. 3;

1) High-voltage n-channel MOSFET (HVN)
2) Medium-voltage p- and n-channel MOSFETs (MVP and MVN)

High-voltage n-channel MOSFET (HVN) is used as a key device in high-voltage level shifters that transmit the GND-level signal to the high-side (OUT) level. A cross section of a HVN with 1200 V blocking capability with the double RESURF structure is shown in Fig. 4. In order to obtain sufficient blocking capability of HVN, the 230 Ω cm FZ-P type substrate is chosen. Both total charges in the n-well and in the p-offset in the double RESURF region are optimized to obtain maximum blocking capability. Therefore, the n-well and p-offset of this edge region are fully depleted when drain rated voltage applied. The OUT terminal is connected to the high-side IGBT emitter terminal. The n-well acts as a drift region, as well as a pinch resistance region. The high-side n-well is connected to the high-side voltage supply. If there is no n-well pinch resistance between the drain and VCC electrode, the drain current flows not through the level shift resistor but through the n-well region, and the on- and off-signals cannot be transmitted. Hence the parasitic pinch resistor must be a larger value than that of level shift resister (R_L).

The self-shielding technique is used for high-voltage interconnection in order to prevent the degradation of blocking capability. The details of the self-shielding technique have been reported previously.[6]

Gate drivers and control logic are composed of MVN and MVP that have offset drift regions as active devices. The blocking capability of MVP and MVN was designed for the 15 V driver. Each of them has blocking capability exceeding 30 V and threshold voltage of 2 V. The same device structures are used in low-side and high-side n-well regions. These devices were fabricated by the 13-mask CMOS process using uniformly doped p-type substrate.

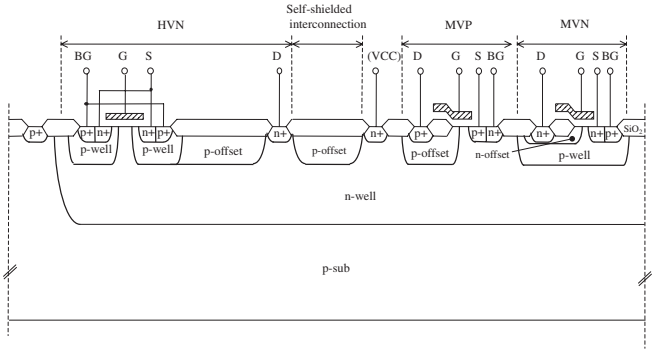


Fig. 3. Schematic cross section of key devices in self-isolation structure. MVP and MVN are used in control unit; GDUH and GDUL as CMOS or active switch. HVN and self-shielded interconnection are used only in GDUH. Metals, insulation layers and passivation are omitted in this figure.

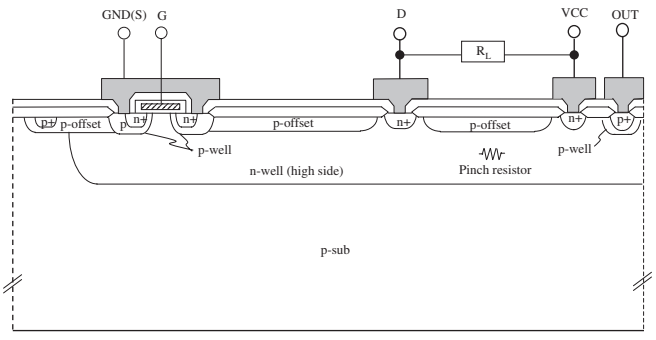


Fig. 4. Cross section of self-shielded high-voltage interconnection and high-voltage level shifter. Parasitic pinch resistance must be made higher than that of level shift resistor (R_L). R_L is formed in high-side n-well region.

3. Design of High-Voltage Isolation Structure

Operations of isolation structures were estimated using a two-dimensional numerical simulator. A p-substrate that has 350 µm thickness and resistivity of 230 Ω cm is used in the simulation. A potential contour of the high-side edge region is shown Fig. 5. Approximately 130 µm is depleted. The maximum impact ionization rate is observed at the source side or drain side depending on the p-offset charge density.

There are parasitic devices that are activated by the displacement current in HVICs during IGBT switching. They are summarized schematically in Fig. 6 and in Fig. 7 as an equivalent circuit. In Fig. 7, I_1 shows displacement current, and $C_{nw(H)}$ corresponds to n-well/p-sub junction capacitance. A matter of great importance in HVIC design is to prevent device destruction under the high dV/dt condition. Two important parasitic transistors are in this structure. One is the parasitic p-well (high-side)/n-well (high-side)/p-sub transistor (T_{pnp}) shown in Fig. 8. The other is the n-well (high-side)/p-sub/n-well (low-side) transistor (T_{npn}) shown in Fig. 9. Some of the displacement current (I_1) flows beneath a high side p-well region, and builds up a potential drop in the n-well region. If the potential drop is large enough to provide forward bias to the p-well/n-well junction, a parasitic pnp transistor is turned on. On the other hand, the displacement current (I_1) also builds up a potential drop in the p-substrate. This potential drop results in the turning on of the parasitic npn transistor. If the sum of the common base current gains, α pnp and α npn, of parasitic transistors exceeds unity, a parasitic thyristor is turned on in the worst case.

In Fig. 8, a parasitic pnp transistor is described as a

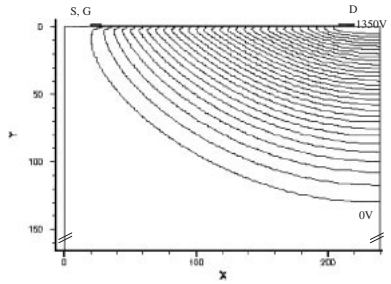


Fig. 5. Potential contours of 1200 V edge termination for HVICs using self-isolation structure. 1350 V is applied to drain (D) terminal in device simulation.

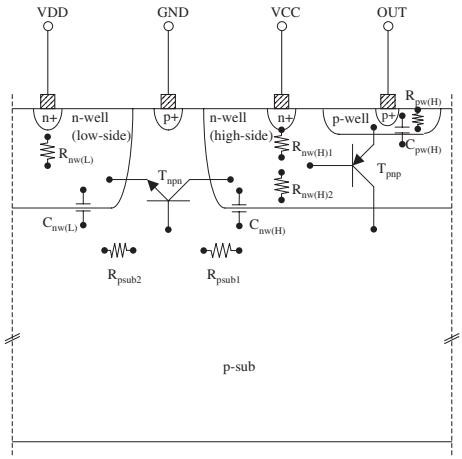


Fig. 6. Schematic cross section of parasitic devices in HVICs. GDUH is formed in n-well (high-side) region, and GDUL is formed in n-well (low-side), respectively. Suppressing the parasitic pnp transistor (T_{pnp}) and parasitic npn transistor (T_{npn}) is the key issue in HVIC design.

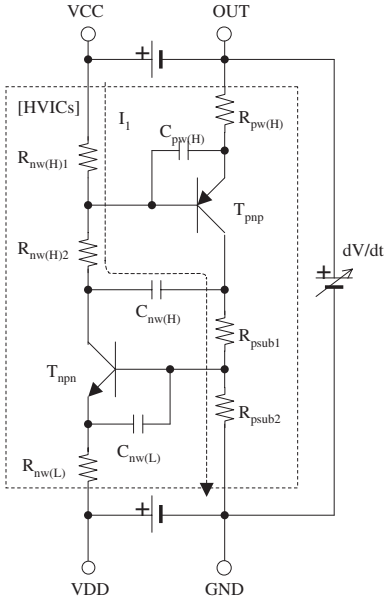


Fig. 7. Equivalent circuit of parasitic devices in HVICs. dV/dt represents the voltage difference between OUT terminal and GND terminal. Large displacement current (I_1) flows under the dV/dt applied condition.

simplified model with a displacement current flow line. P-well diffusion is part of the MVN in this figure.

Since the n-well charge density is limited by the RESURF principle in the SI structure, the distance between n+ contacts at the periphery of the p-well should be limited in high-side design to reduce the potential drop.

The displacement current (I_1) flowing through the n-well/p-sub junction capacitance can be defined by

$$I_1 = C(t)\left(\frac{dV}{dt}\right). \tag{1}$$

The junction capacitance is given by[7)]

$$C(t) = \frac{\varepsilon_s}{W_d} = \sqrt{\frac{q\varepsilon_s N_A}{2\left(V(t) + Vbi - \dfrac{2kT}{q}\right)}}, \tag{2}$$

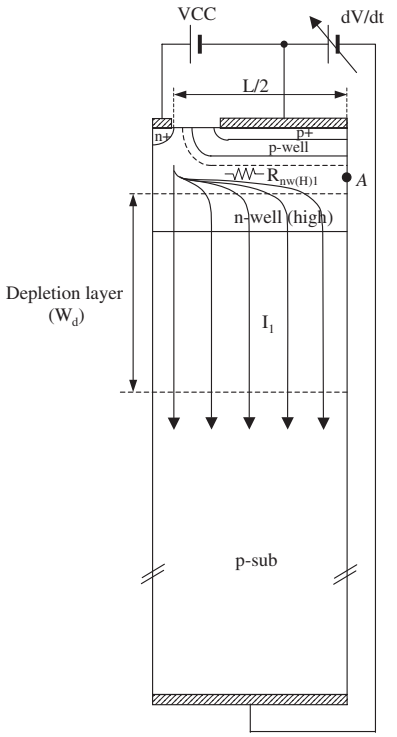


Fig. 8. Schematic cross section and operation of simplified parasitic pnp (T_{pnp}) transistor model. Displacement current (I_1) flows beneath p-well region in high-side n-well when high dV/dt is applied.

ε_s: semiconductor permittivity, W_d: thickness of depletion layer, q: magnitude of electric charge, N_A: impurity density, Vbi: built-in potential, $V(t)$: high-side n-well voltage, k: the Boltzmann constant, T: junction temperature.

Although $C(t)$ has voltage dependence, the junction capacitance can be fixed at the maximum value $C(0)$ in the worst-case estimation of the parasitic action. The maximum junction capacitance is obtained when the p-well potential is the same as the p-sub potential ($V(t) = VCC$). Since $V(t) \gg 2kt/q$,

$$C(0) = \frac{\varepsilon_s}{W_d} = \sqrt{\frac{q\varepsilon_s N_A}{2(VCC + Vbi)}}. \tag{3}$$

Here, all displacement current is assumed to flow through point A shown in Fig. 8, in the worst case. The voltage drop beneath the p-well in the high-side n-well region should be smaller than the sum of high-side power supply voltage (VCC) and built-in potential of the n-well/p-well junction (Vbi) when the displacement current flows through the high-side n-well region. If the device dimensions satisfy eq. (4) under this assumption, the parasitic pnp transistor is suppressed.

$$VCC + Vbi > I_1 R_{nw(H)1}\frac{L}{2} \tag{4}$$

L, which is indicated in Fig. 8, corresponds to the distance between n+ contacts at the periphery of the p-well, hence

$$VCC + Vbi > \sqrt{\frac{q\varepsilon_s N_A}{2(VCC + Vbi)}}\left(\frac{dV}{dt}\right)R_{nw(H)1}\frac{L}{2}. \tag{5}$$

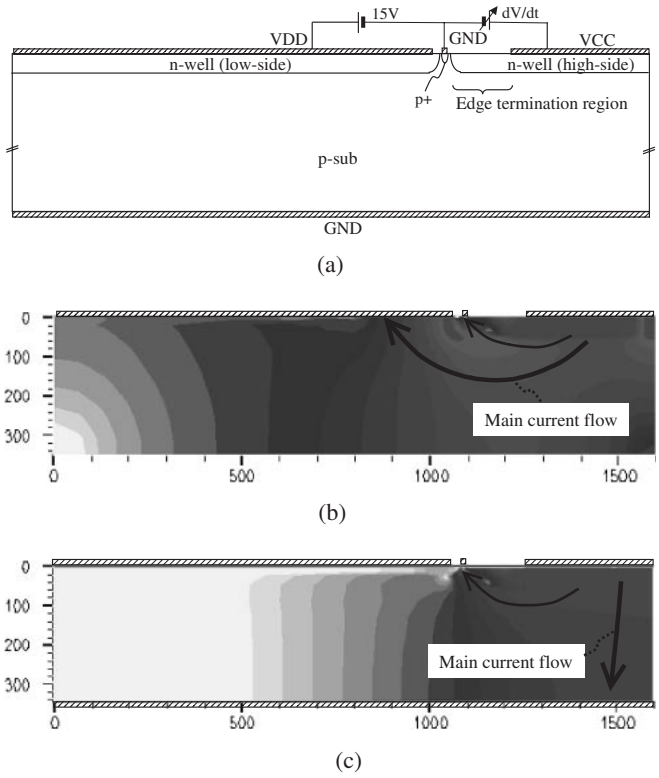


Fig. 9. The difference in total current density distribution of parasitic npn transistor (T_{npn}) model between structures with open back and shorted back under the same dV/dt conditions ($VCC = 300\,\mathrm{V}$, $VDD = 15\,\mathrm{V}$, $dVCC/dt = 30\,\mathrm{kV/\mu s}$). Dark color: higher current density, light color: lower current density. Horizontal scale is different from (b) and (c). (a) Schematic of simulated structure. (b) Total current density distribution of structure with open back. (c) Total current density distribution of structure with shorted back.

Therefore, the maximum L should be satisfied a following relation as described below.

$$L < \frac{2}{R_{\mathrm{nw(H)1}}\left(\frac{dV}{dt}\right)}\sqrt{\frac{2(VCC + Vbi)^3}{q\varepsilon_s N_A}} \tag{6}$$

Relationship (6) is acceptable and has been included in the HVICs design.

A simplified parasitic n-well (high-side)/p-sub/n-well (low-side) transistor is shown in Fig. 9(a). In the SI structure, displacement current also flows toward the GND terminal that is in contact with the p-substrate. If the GND terminal is set at the periphery of the high-side n-well region, all the displacement current flows toward this surface GND contact, and builds up a potential drop which is large enough to provide forward bias to the p-sub/n-well (low side) junction. Figure 9(b) shows the total current density in this case, when $30\,\mathrm{kV/\mu s}$ is applied to the high-side n-well. In this figure, bipolar operation can be clearly seen and almost the entire current flows to the low-side n-well region. In order to avoid this parasitic operation, it is necessary to set a diverter in this structure. If GND terminals are set at both the surface and back of the p-substrate, most of the displacement current flows toward the back electrode which acts as a diverter, as shown in Fig. 9(c). In the parasitic NPN transistor model, the behavior of the current beneath the low-side n-well region depends on the wafer thickness. In the case of 350 μm thickness, the current is diverted effectively, and no bipolar action can be seen in this figure.

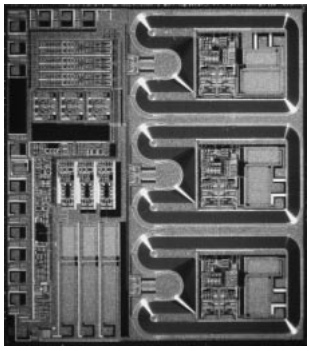


Fig. 10. Top view of 1200 V HVICs designed for three-phase IGBT gate driver using self-isolation structure in this experiment.

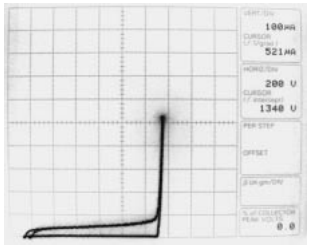


Fig. 11. Blocking capability of high-voltage self-isolation structure in 1200 V HVICs. VCC terminal is biased against GND terminal in this measurement.

4. Experimental Results and Discussion

A top view of 1200 V HVICs designed for a three phase IGBT inverter circuit is shown in Fig. 10. The die size is $4.3 \times 4.8\,\mathrm{mm}^2$, and the HVICs have control logic, a protection circuit (e.g., under voltage driving protection), and high-side and low-side gate drivers for 15-A-class IGBT. Sufficient blocking capability of 1340 V has been confirmed, as shown in Fig. 11. A VCC terminal is biased against the GND terminal in this measurement.

Although the dc bus voltage in 1200 V device applications is less than 900 V, the operation of the high-voltage level shifter is tested up to 1000 V. In order to reduce the power loss in the high-voltage level shifter, two HVNs are used for on and off signals in HVICs. Figure 12 shows waveforms of the level-shift operation. Amplitudes of input and output signals are 5 and 15 V respectively.

In order to confirm the behavior against high dV/dt, dV/dt robustness was evaluated using the test circuit shown in Fig. 13. This circuit gives two types of dV/dt noise to HVICs: such as $+dV/dt$ and $-dV/dt$. $+dV/dt$ accompanied by displacement current flowing from the high-side to the low-side charges up the n-well/p-sub junction capacitance, and $-dV/dt$ accompanied by the current from the low-side to the high-side discharges the junction capacitance. Because the current direction of the parasitic p-well/n-well/p-sub transistor is the same as that of $+dV/dt$, $+dV/dt$ robustness is the more important factor in a self-isolation structure. For this reason, the value of dV/dt corresponds to $+dV/dt$ in

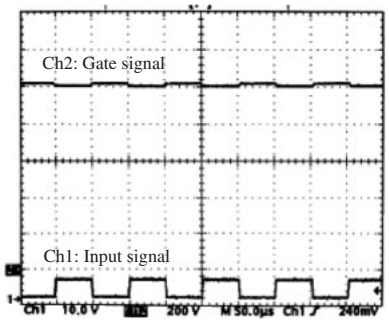


Fig. 12. High-voltage level shift waveforms of 1200 V HVICs using self-isolation structure. Operation frequency: 10 kHz. Ch1: 10 V/div, Ch2: 200 V/div, 50 μs/div (ambient temperature: 105°C).

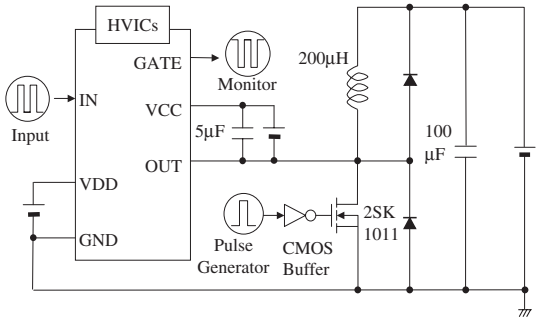


Fig. 13. dV/dt test circuit for HVICs. dV/dt is generated by turning off the current flowing to the inductor in the circuit.

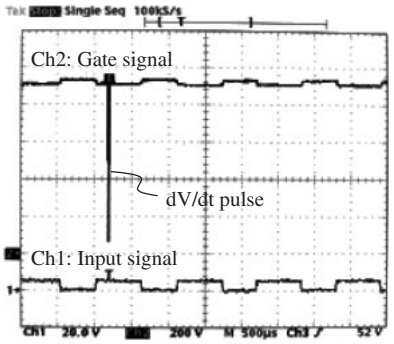
this experiment. A short pulse with high dV/dt, which corresponds to a short off period of the high-side IGBT, is also applied to HVIC in PWM inverter circuits. The dV/dt is generated by turning off the current flowing to the inductor, and a power MOSFET is used with a CMOS buffer. The dV/dt output was gradually increased by stepping up the applied dc voltage of the high-voltage power supply to 900 V. The maximum dV/dt output was set at 30 kV/μs in this circuit. Figures 14(a) and 14(b) show the measured input and gate signal voltages. As shown in these figures, there is neither output failure nor destruction up to 30 kV/μs in this test.

The other high-side driver circuits in different n-well regions were tested with the same dV/dt circuit, and the same results were obtained. These results indicate that the parasitic thyristor or transistor action in the HVIC was effectively suppressed by using the design rule and back diverter GND contact.

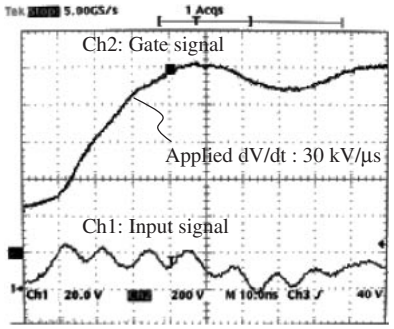
In order to confirm the validity of the previous estimation based on the parasitic transistor model, the dV/dt test was performed without the back electrode. The results are shown in Fig. 15. The device was destroyed below 10 kV/μs and collector voltage of 400 V. From this result, it is obvious that the parasitic transistors govern the dV/dt robustness of HVICs without a back electrode.

5. Conclusions

The 1200 V HVICs with the self-isolation structure was experimentally demonstrated for the first time. The device showed sufficient blocking capability. The operation of the high-voltage level shifter was confirmed up to 1000 V.



(a)



(b)

Fig. 14. Waveforms in the dV/dt test circuit. 30 kV/μs was applied to HVICs with a structure of shorted back (ambient temperature: 25°C). (a) Level shift waveforms in dV/dt test circuit when 30 kV/μs was applied (Ch1: 20 V/div, Ch2: 200 V/div, 500 μs/div). (b) Applied dV/dt waveforms (Ch1: 20 V/div, Ch2: 200 V/div, 10 ns/div).

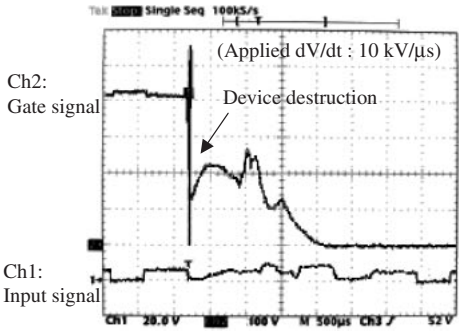


Fig. 15. Failure waveforms in dV/dt test for structure with open back. Ch1: 20 V/div, Ch2: 100 V/div, 500 μs/div (ambient temperature: 25°C).

Superior dV/dt robustness was confirmed by considering the suppression of parasitic transistors.

Acknowledgments

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