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TOPICAL REVIEW

From wide to ultrawide-bandgap semiconductors for high power and high frequency electronic devices

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Abstract

Wide and ultrawide-bandgap (U/WBG) materials have garnered significant attention within the semiconductor device community due to their potential to enhance device performance through their substantial bandgap properties. These exceptional material characteristics can enable more robust and efficient devices, particularly in scenarios involving high power, high frequency, and extreme environmental conditions. Despite the promising outlook, the physics of UWBG materials remains inadequately understood, leading to a notable gap between theoretical predictions and experimental device behavior. To address this knowledge gap and pinpoint areas where further research can have the most significant impact, this review provides an overview of the progress and limitations in U/WBG materials. The review commences by discussing Gallium Nitride, a more mature WBG material that serves as a foundation for establishing fundamental concepts and addressing associated challenges. Subsequently, the focus shifts to the examination of various UWBG materials, including AlGaN/AlN, Diamond, and Ga_2O_3. For each of these materials, the review delves into their unique properties, growth methods, and current state-of-the-art devices, with a primary emphasis on their applications in power and radio-frequency electronics.

1. Introduction

Wide bandgap (WBG) materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), have unequivocally demonstrated their versatility across various fields, including optics, power electronics, and radio frequency (RF) technology. This has led to a significant expansion of their applications and a burgeoning market presence. What sets them apart is their exceptional ability to operate effectively in high-temperature and challenging environments. The progress in WBG materials is now driving substantial interest in an emerging class of semiconductors known as ultrawide-bandgap (UWBG) materials, distinguished by even wider bandgaps. Both WBG and UWBG materials exhibit remarkable resistance to electric field breakdown due to their large bandgap, offering a multitude of advantages to electronic devices and systems. These benefits encompass enhanced efficiency, the capability for high-temperature operation, smaller footprints, simplified system designs, and reduced overall system costs. Ultimately, broader positive impacts such as diminished carbon emissions and closure of the digital divide can result from the successful development of these technologies. In terms of specific device applications, today GaN has asserted its dominance in lighting technology, with noteworthy contributions in radar and telecommunication as well. Additionally, GaN has made significant inroads into power electronics. SiC, on the other hand, has excelled in medium to high-power electronics and serves as an excellent substrate for GaN RF technology. Consequently, there exists both a symbiotic and competitive relationship between SiC and GaN, shaping the current landscape of applications and markets. Their collective successes have firmly established WBG materials on the technological map, paving the way for the exploration of UWBG materials.

Table 1. Material properties of GaN and emerging UWBG semiconductors and their Baliga and Johnson figure of merits [3, 4] (references therein).

Material Parameters	GaN	β-Ga_2O_3	Diamond	AlN
Bandgap E_g (eV)	3.4	4.8	5.5	6.0
Critical Field E_{cr} (MV cm^{-1})	3–3.5	8–10.3	10–13	15.4
Electron mobility μ_e (cm^2 V^{-1} s^{-1})	1000	180	4500	426
Hole mobility μ_h (cm^2 V^{-1} s^{-1})	24	—	3800	—
Relative permittivity ε_r	10.4	10	5.7	9.76
Electron saturation velocity v_{sat} (10^7 cm s^{-1})	1.5–2.0	1.1	2.3	1.3
Thermal conductivity K (W m^{-1} K^{-1})	253	11–27	2290–3450	285–319
Baliga FOM (10^6 V^2 Ω^{-1} cm^{-2})	27 900	36 300	554 000	336 000
Johnson FOM (10^{12} V s^{-1})	11	18	29–47	31.9

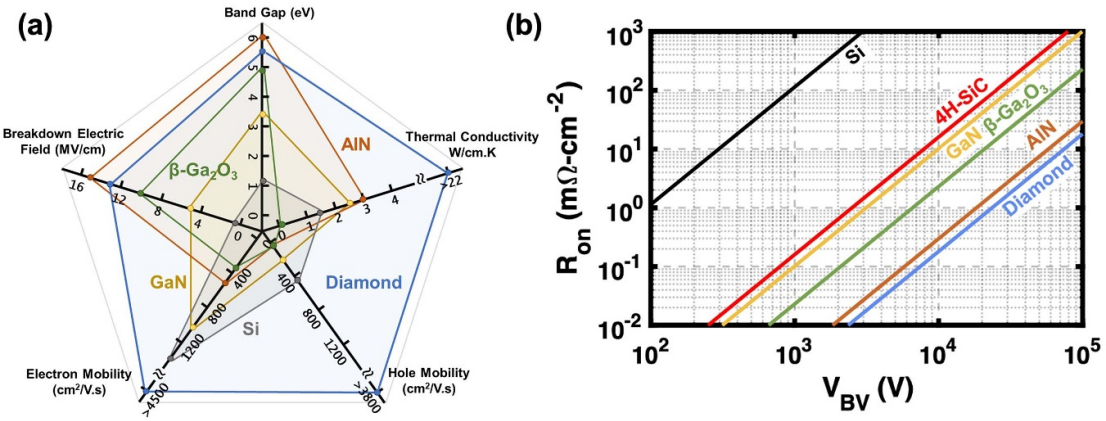

Figure 1. (a) Material properties of U/WBG semiconductors presented in a spider chart; (b) the theoretical BFOM of these materials compared to Si.

The significance of semiconductor technology and its sustainability are frequently assessed through its market size. In the power semiconductor sector, the projected global market for Silicon Carbide is $6 billion, and for Gallium Nitride $2 billion by the year 2027 [1]. This substantial growth can be predominantly attributed to the expansion of hybrid and electric vehicles and several other key sectors, including, power supplies, military/aerospace applications, as well as renewable energy and smart grids. In the GaN RF market, an annual revenue of $1.8 billion in 2022 is predicted to increase to $2.7 billion by 2028 [2]. This significant commercial revenue stems from the utilization of high electron mobility transistors (HEMTs) for power amplifiers in wireless base stations. Furthermore, the increased efficiency and reliability offered by RF-oriented GaN find valuable applications in radar systems within the defense sector.

UWBG materials, like AlGaN/AlN, diamond, and β-Ga_2O_3, have similar applications to those of WBG materials; however, with significantly larger bandgaps than 3 eV, they promise to offer even higher performance metrics. The electronic properties of GaN and UWBG materials are listed in table 1 and illustrated in figure 1. A simple method to quantify a device's suitability for power applications (specifically low frequency unipolar power switching) is by the Baliga figure of merit (BFOM): $V_{br}{}^2/R_{on,sp}$ or $\frac{1}{4}\varepsilon\mu E_{cr}{}^3$, where V_{br} is the breakdown voltage, $R_{on,sp}$ is the specific on-resistance, ε is the dielectric constant, μ is the carrier mobility, and E_{cr} is the critical electric field. A higher value indicates that a device can sustain high blocking voltages while incurring minimal on-state losses, which can be visualized in figure 1(b). Thus, the critical electric field, which typically scales with the bandgap has a large influence on the BFOM. For high frequency power applications, the Johnson figure of merit (JFOM) is used: $v_{sat}E_{cr}/2\pi$, where v_{sat} is the saturation velocity. According to both FOMs, UWBG materials provide significant improvement in comparison to GaN which itself greatly surpasses Si in high power and frequency device performance.

In this comprehensive review article, our primary focus is on the exploration of electronic device technology led by GaN as a well-established technology, along with emerging technologies such as AlGaN/AlN, Diamond, and β-Ga_2O_3. Our discussion will revolve around various aspects of these materials of interest, including their material properties, growth techniques, devices, and applications, providing an ample overview of their significance in the field of electronic device technology. While we recognize the significance of Silicon Carbide, it is not included in this article, and we would like to direct interested readers to some outstanding recent reviews on this subject [5, 6].

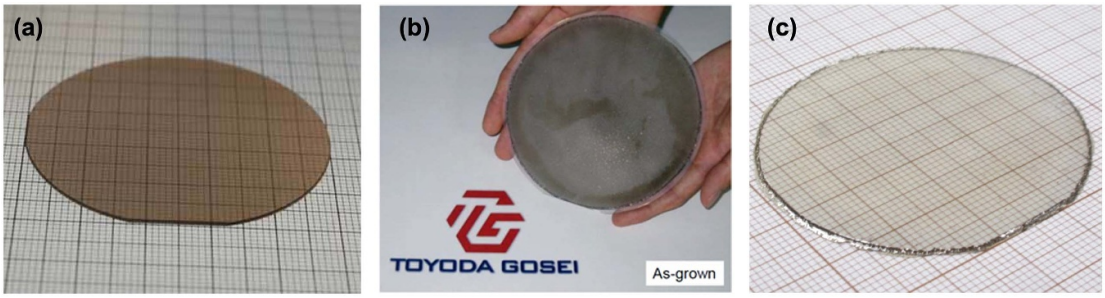

Figure 2. (a) Image of 2 inch. c-plane ammonothermal-GaN substrate (manufactured at AMMONO company) [20]; (b) 6 inch GaN crystal grown on MOCVD-GaN seeds using Na-flux method [21]; (c) 2 inch HVPE-GaN wafer with a thickness of 500 μm and an etch pit density of 5×10^4 cm^{-2} [22].

2. Gallium nitride (GaN)

2.1. Material properties

The electron mobility in bulk GaN at room temperature is dependent on the doping, where it can reach 1000 cm^2 (V·s)$^{-1}$ at low doping concentrations of 10^{15}–10^{16} cm^{-3} and decreases to 200–600 cm^2 (V·s)$^{-1}$ in the doping range of 10^{17}–10^{18} cm^{-3}. The hole mobility is much lower, typically less than 100 cm^2 (V·s)$^{-1}$, and drops to around 10–30 cm^2 (V·s)$^{-1}$ in the doping range of 10^{17}–10^{18} cm^{-3}. A detailed mobility model for GaN describing the doping and temperature dependence is well documented [7]. On the other hand, the electron mobility in the two-dimensional electron gas (2DEG) formed at the AlGaN/GaN interface can reach up to 2000 cm^2 (V·s)$^{-1}$ at room temperature [8], motivating the development of GaN-based HEMTs. For high-field transport, the highest electron saturation velocity in GaN was reported to be 2–2.5 $\times$ 10^7 cm s^{-1} [9, 10], while the hole saturation velocity was limited to 0.7 $\times$ 10^7 cm s^{-1} [11, 12].

The intrinsic breakdown in a material is caused by avalanche initiated by the impact ionization at high electric fields. A critical field of 3–3.5 MV cm^{-1} is estimated for GaN by the empirical formula in terms of its 3.4 eV bandgap [4]. In recent years, avalanche has been routinely achieved in GaN PN structures with proper doping profiles and efficient field management designs due to the availability of higher-quality native GaN substrates. Several photo-multiplication-based methods have been utilized in experiments to extract the impact ionization coefficients for electrons and holes in GaN [13–15]. Based on these coefficients, a physics-based model describing the critical field regarding doping concentration in GaN has been proposed [16].

For high power and frequency devices, the thermal properties of the materials become increasingly important as self-heating becomes a larger issue. The thermal conductivity (TC) of a material dictates how efficiently it can dissipate heat. For GaN, the TC is moderately high, around 170–220 W (m·K)$^{-1}$ [17, 18], and was reported to be sensitive to the doping concentration and dislocation density.

2.2. Growth and doping

2.2.1. Bulk substrate growth

The past few decades have witnessed the rapid development of GaN-based electronic devices from experimental prototypes to successful commercialization. The scalability and quality of native GaN substrates play a critical role in reducing the manufacturing costs of GaN to further boost its commercial appeal, however, they still require more research efforts within the nitride community. The decomposition pressure at the melting point for GaN is around 6 GPa [19], leading to intrinsic difficulties in adopting the traditional melt growth method for bulk GaN substrates. Numerous research efforts in developing new crystal growth technology for GaN have been made, mainly consisting of three growth methods: ammonothermal growth, sodium-flux (Na-flux) growth, and hydride vapor phase epitaxy (HVPE). Figure 2 shows the images of the bulk GaN substrates grown by each of these methods.

The ammonothermal method begins by solubilizing polycrystalline (PC) GaN feedstock in supercritical ammonia under high pressure (100–500 MPa) [23, 24]. Then, the dissolved materials are transported to the recrystallization region along a temperature gradient and growth on the seeding crystals occurs at temperatures of 500 °C–600 °C [23, 25, 26]. 2 inch GaN bulk substrates with a dislocation density down to 5×10^3 cm^{-2} were successfully demonstrated with the ammonothermal growth method [20]. The method's primary limitation is its relatively slow growth rate of around a few micrometers per hour.

Na-flux growth also belongs to the category of solution growth approaches but produces a more favorable growth condition by using sodium flux. The typical temperature and pressure during growth are

around 750 °C–900 °C and 5 MPa [27–30], respectively. Today, this method can produce a 6 inch crystallographically flat GaN wafer with high structural quality [31], and the typical dislocation density of the Na-flux method is around 10^4–10^6 cm^{-2} [32].

Finally, the knowledge of HVPE growth of GaN was appropriated from the growth of GaAs and InP. In this method, chloride gas reacts with a gallium source and forms a gaseous phase in the source zone (800 °C–900 °C). The product is then transported to the nitrogen source in the deposition zone (1000 °C–1100 °C) for further reaction and crystallized as GaN [22, 33]. The most significant advantages of HVPE growth include the atmospheric pressure condition and a high growth rate on the order of several hundreds of micrometers per hour [34]. However, the size and thickness of the wafer are limited by the bowing of the crystallographic planes due to the lattice mismatch between GaN and the seeding materials.

2.2.2. Epitaxial layer growth

Several epitaxial growth methods have been developed for GaN thin-film growth on either native or nonnative substrates, including HVPE [35–38], molecular beam epitaxy (MBE) [39–42], and metalorganic chemical vapor deposition (MOCVD) [43–45]. When growing on nonnative substrates, a low-temperature AlN buffer layer is usually adopted to improve the surface morphology and increase the crystal quality by mitigating the lattice mismatch between GaN and foreign substrates [46]. Homoepitaxial growth on native GaN substrates does not require such a buffer layer. MBE growth provides precise control of the impurity and thickness of the film during the growth; however, it usually requires a high-vacuum atmosphere. MOCVD is considered to be the leading technique for the growth of III–V-nitride materials for mass production [47]. The use of high-purity chemical sources, characteristic of this method, yields a high degree of composition control and uniformity, high growth rates, and large-scale manufacturing potential.

2.2.3. Doping

Si is the most commonly used dopant element for donors in GaN by substituting the Ga sites [48]. The Si doping concentration can be well controlled by adjusting the flow rate of the gaseous source, for example, SiH_4 or Si_2H_6, over the range from 10^{16} to 10^{19} cm^{-3} without forming cracks and surface pits during growth [49, 50]. It was demonstrated that Si offered shallow donor states (around 10–20 meV) in GaN [51, 52], giving rise to a nearly complete ionization ratio at room temperatures. Furthermore, nitrogen vacancies in GaN can also provide unintentional n-type doping in GaN [53, 54].

P-type doping in GaN was also successfully achieved by using Mg as acceptors, which led to the invention of the blue LED utilizing a GaN PN junction. However, Mg-doped GaN tends to be electrically insulating if grown in the presence of hydrogen. The role of H atoms in passivating the Mg acceptors in GaN was elucidated as the H atoms were found to form neutral Mg–H complexes [55, 56]. The Mg–H bonds can be broken by low-energy electron beam irradiation or a high temperature thermal anneal above 700 °C [55, 57], which gives free holes in GaN. Due to the relatively high activation energy of Mg (130–180 meV reported) in GaN [58–60], the ionization ratio of Mg acceptors is typically less than 10%. Achieving a high hole concentration and high p-type conductivity with Mg remains critical for the GaN community.

Given the material properties and growth techniques summarized in the previous sections, we will discuss a few fundamental device structures and their applications to elucidate the importance of GaN in power and radio-frequency electronics.

2.3. GaN devices and applications

2.3.1. High power devices

2.3.1.1. Schottky barrier diodes (SBDs)

The SBD is one of the basic rectifiers used in power electronics. Due to its majority carrier transport mechanism, it has the advantage of low turn-on voltage, fast switching, and thus low switching losses. However, the thermionic field emission transport at the metal–semiconductor interface leads to a rapid increase of leakage current at high surface electric fields, limiting the breakdown performance of GaN SBDs. Thus, from a device engineering perspective, efficient edge termination designs are needed to relax the field concentration at the anode edge to improve the breakdown.

Almost all reported GaN SBDs are based on an n-type drift region due to the excellent controllability of n-type GaN growth. Nickle (Ni) is one of the most commonly used contact metals for GaN. GaN SBDs can be simply fabricated by depositing a Schottky contact after the epitaxial growth of the drift region. In this configuration, the field concentration at the anode edge leads to a premature breakdown. The field plate structure (figure 3(a)) is an effective method to mitigate the peak electric field at the edge of the anode, thus enhancing the breakdown voltage [61, 62]. A GaN SBD over 1 kV was reported in 2010 by using a field plate on SiN_x layers for edge termination. Furthermore, growth optimization yielded a structure with a high bulk electron mobility of 930 cm^2 $(V{\cdot}s)^{-1}$, which contributed to a low specific on-resistance of 0.71 $m\Omega{\cdot}cm^2$ [61].

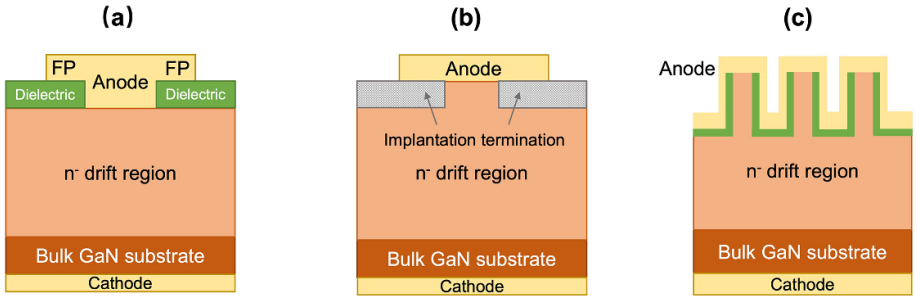

Figure 3. Schematics of different edge terminations in GaN SBDs: (a) GaN SBD with field plate (FP); (b) GaN SBD with ion implantation termination; (c) GaN SBD with trench metal–insulator–semiconductor configuration.

As shown in figure 3(b), the implantation of several species, such as Argon (Ar) and Fluorine (F), was reported to successfully convert n-type GaN to a highly-resistive region [63–66]. This high-resistivity region helps spread the potential along the surface, resulting in a mitigated electric field at the edge and reduced leakage current. Utilizing this technique, a 1.7 kV GaN SBD with Ar implantation termination has been achieved [64], and F implantation also showed a boost of breakdown voltage from 155 V to 775 V in GaN SBDs [67]. Similarly, plasma nitridation can increase the energy barrier height at the edge by compensating the nitrogen vacancies [68], offering a superior breakdown voltage of 995 V compared to 335 V without nitridation termination [69].

Trench metal–insulator–semiconductor barrier Schottky diodes (TMBS) have been proposed to effectively modulate the surface electric field at the Schottky contact to achieve a more uniform field distribution [70–72]. A representative TMBS structure is shown in figure 3(c). However, the peak field at the trench corner may also lead to field crowding and premature failure in the dielectrics. Thus, Zhang *et al* reported a novel TMBS structure with Ar implantation beneath the trench oxide, which mitigated this issue [73]. This method effectively enhanced the breakdown voltage from 500 V to 700 V after implantation treatment without degrading the forward characteristics.

2.3.1.2. PN junction diodes (PNDs)

GaN PNDs show lower leakage current and better thermal stability compared to GaN SBD diodes, despite their relatively high turn-on voltage. In contrast to SBDs, the peak electric field in PNDs appears near the junction instead of at the metal contacts as in GaN SBDs. Thus, the peak electric field can be buried inside the bulk, which prevents premature breakdown and improves the feasibility of achieving avalanche in vertical GaN PN diodes. Thanks to the increasing availability of native bulk GaN substrates with low dislocation density, the avalanche phenomenon has been more routinely reported in GaN PN structures. While avalanche is recognized as a performance benchmark in power devices, the off-state leakage current is another important metric in determining the power loss. The relationship between dislocation density and leakage current under the prerequisite of avalanche has been experimentally examined [74]. It was suggested that Poole–Frenkel effects dominated when the dislocation density was in the range of 10^4 cm^{-2} and variable-range-hopping mechanisms dominated when a higher dislocation density (10^6 cm^{-2}) was present in the device.

In GaN PND fabrication, mesa etches are the most versatile edge termination method used. Several edge terminations based on mesa etch are shown in figures 4(a)–(d). The deep mesa etch of the entire drift region creates a uniform electric field distribution, almost the same as in a 1D ideal planar structure [75]. Combined with a sidewall passivation layer, a deep mesa-etched diode was able to produce an 880 V avalanche in a GaN PN diode. A small-angle bevel mesa was also reported to effectively modulate the electric field near the PN junction [76, 77]. However, the bevel design is very sensitive to the ratio of the doping concentration and the bevel degree [78]. Field plating on a beveled mesa further mitigates the peak electric field near the junction, showing great potential in high-voltage kV-class GaN PND with avalanche capability [79, 80]. A 3.48 kV breakdown voltage and low specific on-resistance of 0.95 $m\Omega{\cdot}cm^2$ have been achieved using field plating in a GaN PN structure [80]. Recently, a junction termination extension (JTE) based on multiple-step mesa etched was successfully demonstrated in vertical GaN PN diode, resulting in an avalanche breakdown voltage of over 6 kV in GaN [81, 82]. Mg implantation into the sidewall after a mesa etch demonstrated a 1.5 kV avalanche in vertical GaN PNDs [83] without the need for an anneal to activate Mg. Instead, the implanted positive species create a depletion layer underneath the sidewall, shielding the high electric field at the surface, thus reducing the surface leakage.

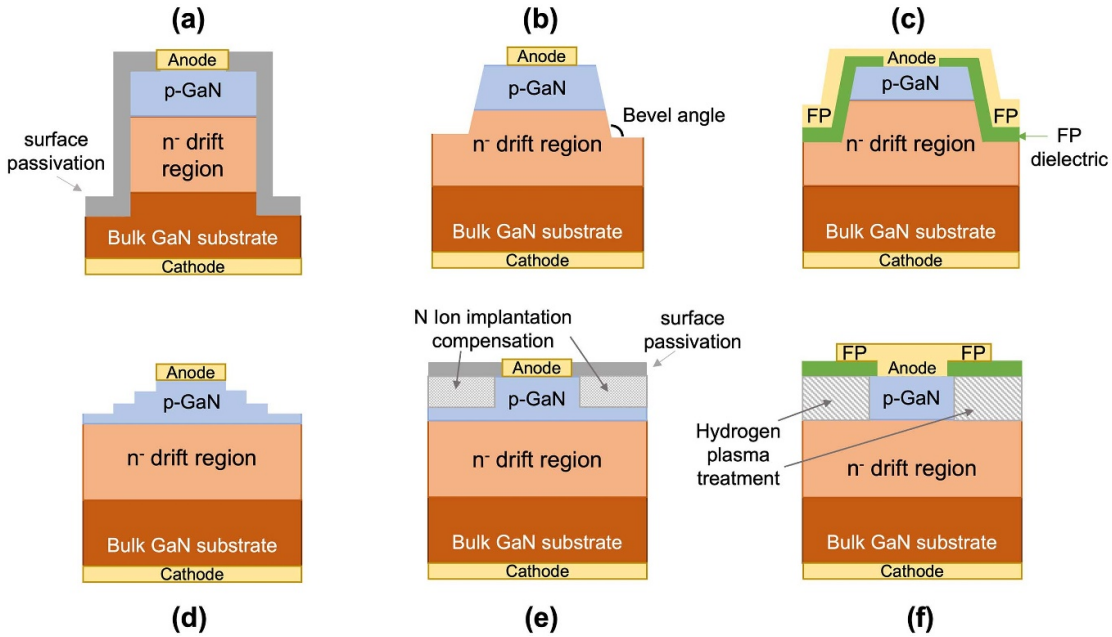

Figure 4. Schematics of different edge terminations adopted in GaN PNDs leading to avalanche breakdown: (a) GaN PND with deep mesa etch; (b) GaN PND with bevel angle mesa etch; (c) GaN PND with field plate on top of a beveled mesa; (d) GaN PND with junction termination extension (JTE) based on multiple-step mesa etch; (e) GaN PND with ion implantation compensation; (e) GaN PND with field plate on top of passivated p-GaN by hydrogen plasma treatment.

Nitrogen ion implantation compensation offers a planar edge termination without the requirement of a mesa etch (figure 4(e)). The partially compensated p-GaN layer helps to laterally distribute the electric field to support a high voltage [84, 85]. A SiN_x surface passivation layer is required to suppress the surface leakage. Contrary to the activation process of an Mg-doped p-GaN layer, hydrogen plasma treatment was demonstrated to passivate the Mg in p-GaN again by forming neutral Mg–H complexes, creating a high-resistivity layer [86–88]. Hydrogen plasma based guard ring structures showed a vertical GaN PND with 1.7 kV breakdown and 0.65 $m\Omega{\cdot}cm^2$ specific on-resistance [89]. Adding a field plate on the passivated p-type layer helped reduce the electric field around the corner of the junction (figure 4(f)), resulting in a 2.8 kV avalanche breakdown device, justifying the application of hydrogen plasma treatment in fabricating high-voltage GaN PNDs [90].

2.3.1.3. Junction barrier diodes and superjunctions

Junction barrier diodes (JBS) incorporate the merit of low turn-on voltage and reduced leakage current from an SBD and PND design. GaN JBS diodes fabricated by Mg ion implantation followed by a multi-cycle rapid thermal annealing (RTA) method exhibited a >600 V breakdown voltage but a very large specific on-resistance >100 $m\Omega{\cdot}cm^2$ [91]. Later, multiple pulsed thermal annealing at 1350 °C was reported to partially recover the implantation damage and activate the implanted Mg, leading to an improved specific on-resistance of 1.7 $m\Omega{\cdot}cm^2$ with a 600 V breakdown [92]. Matys *et al* obtained the high activation ratio of implanted Mg by implementing the thermal annealing under ultra-high pressure at 500 MPa, leading to a high-quality p-type JTE structure, offering a nondestructive breakdown voltage of 675 V with a low on-resistance of 0.67 $m\Omega{\cdot}cm^2$ [93]. Recently, Zhou *et al* also demonstrated the avalanche capability in Mg-implanted GaN JBS [94].

A superjunction structure (SJ) theoretically gives rise to a better trade-off relationship between breakdown voltage and the specific on-resistance since the charge balancing does not require lowering the doping concentration in the drift region to achieve a high-voltage blocking. However, due to the difficulties in achieving a deep column of p-type GaN, vertical SJs in GaN are rarely reported. Xiao *et al* demonstrated a heterogeneous GaN SJ by using p-type NiO as a p-type column filling [95]. The schematics of the fabricated device and SEM cross-section images are shown in figures 5(a) and (b). The forward characteristics of the device exhibited two stages of turn-on behavior, corresponding to NiO/GaN and GaN PN junction, respectively. The fabricated SJ offered a 1.1 kV breakdown voltage with an on-resistance of 0.15 $m\Omega{\cdot}cm^2$, exceeding the unipolar GaN limit. The leakage current was attributed to the sidewall interface of GaN/NiO and avalanche was not observed. With the development of Mg ion implantation technology in GaN, increasing reports of homogeneous GaN SJs can be expected.

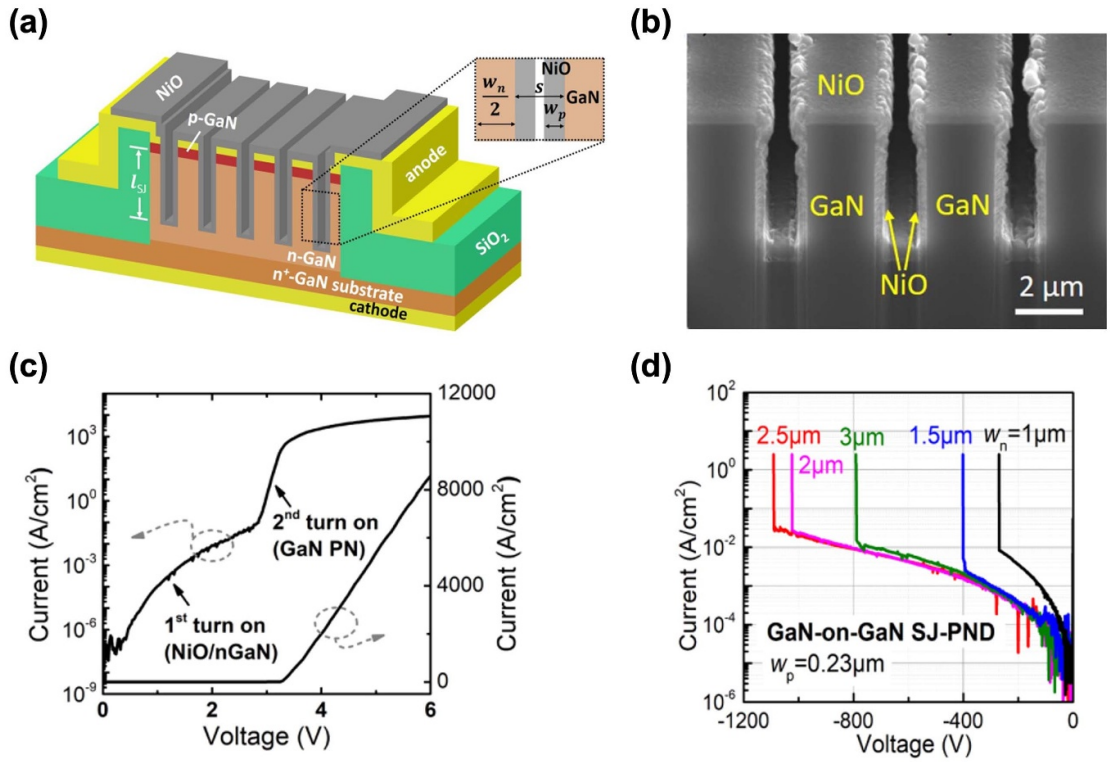

Figure 5. (a) Schematic of the vertical GaN superjunction diode and the zoom-in of a SJ unit-cell; (b) cross-section FIB-SEM images of the SJ region of the fabricated SJ-PNDs; (c) forward I–V characteristics of GaN SJ-PNDs plotted; (d) reverse I–V characteristics of the GaN-on-GaN SJ-PNDs with different spacings [95].

2.3.1.4. HEMTs for power electronics

A 2DEG can be generated at an AlGaN/GaN interface without any intentional doping due to the polarization-induced charges [96, 97]. High electron mobilities up to 2000 cm^2 $(V{\cdot}s)^{-1}$ at room temperature and high sheet carrier densities of 10^{13} cm^{-2} can be obtained in the 2DEG channel [8]. Low-resistance transistors based on the 2DEG channels in the AlGaN/GaN heterostructures are referred to as HEMTs. The GaN HEMT has been one of the most successfully commercialized devices in the GaN family. In 2014–2015, Transphorm Inc. first announced their cascode packaged 600 V GaN HEMTs as power switches which meet the standards of the Joint Electron Devices Engineering Council (JEDEC), marking a milestone in the commercialization of GaN in system products [98, 99].

Typically, GaN HEMTs adopt a lateral configuration, consisting of several epitaxial layers on foreign substrates, such as Si, Sapphire, or SiC. The mismatch of the lattice constants and coefficients of thermal expansion between GaN and the foreign substrates usually leads to a high dislocation density (10^8–10^{10} cm^{-2}) [100–102], which can be a major source of leakage current and degrade the electrical properties of the 2DEG. Thus, an AlN nucleation layer is typically used as a starting layer for GaN growth to mitigate the stress during the growth and cooling process [46, 103, 104]. On top of an AlN nucleation layer, proper design and growth of buffer layers are critical for HEMTs. A step-graded AlGaN buffer, several microns in thickness, or a GaN/AlN superlattice structure can be adopted to further mitigate the lattice mismatch before growing the AlGaN/GaN channel [105, 106], which helps to maintain the excellent electrical properties of the 2DEG.

Due to the nature of the 2DEG channel, HEMTs are usually normally-on devices; however, normally-off operation is preferred in most electronic applications. The cascode configuration, depicted in figure 6(a), allows the normally-off operation of a GaN HEMT without changing the device structure by utilizing a normally-off Si metal-oxide-semiconductor field-effect-transistor (MOSFET) in series with the GaN HEMT device [107–109]. A monolithically integrated Si–GaN cascoded FET has been demonstrated, offering a threshold voltage (V_{th}) of 3.2 V, a specific on-resistance of 3.3 $m\Omega{\cdot}cm^2$, and a high breakdown voltage of 696 V [110]. However, the complexity of the packaging process and the limitation of high-temperature operation by the Si devices remain challenges to be addressed [111].

The recessed gate structure (figure 6(b)) fabricated by etching the AlGaN barrier layer beneath the gate followed by the deposition of a dielectric layer is another approach to achieve normally-off HEMTs [112–114]. The thinning of the AlGaN layer beneath the gate selectively removes the 2DEG in that region

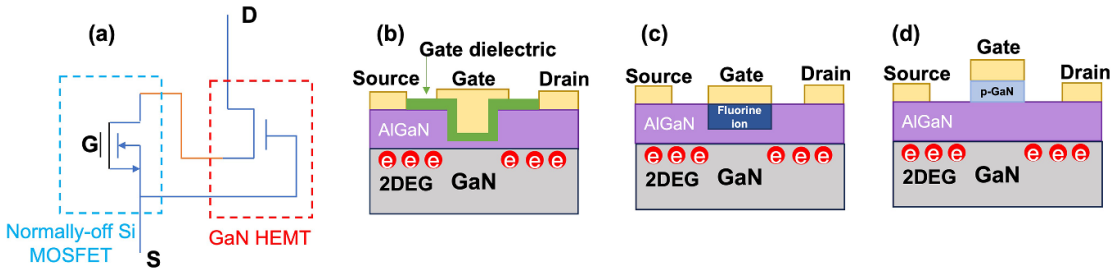

Figure 6. Schematic view of different architectures in achieving normally-off mode GaN HEMT: (a) cascode configuration in series with a normally-off Si metal–oxide–semiconductor field-effect-transistor, with the effective gate (G), drain (D), and source (S) depicted; (b) GaN HEMT with a recessed gate; (c) GaN HEMT with fluorine implantation under the gate; (d) GaN HEMT with a p-GaN gate.

and shifts the threshold voltage. The etch process is critical, as the plasma-induced damage and the surface roughness caused by etching can degrade the electrical properties of the 2DEG channel [115]. The choice of the gate dielectric is also important for reducing surface states and gate leakage, thus improving the channel mobility and the stability of the threshold voltage [116–119]. The integration of a slant field plate enabled an enhancement mode GaN HEMT with a high breakdown voltage of 1.7 kV and a specific on-resistance of 3 $m\Omega \cdot cm^2$ [120]. Fluorine implantation (figure 6(c)) is another attractive method to offer a normally-off operation without plasma etching [121, 122]. The implanted negative fluorine ions change the surface potential and deplete the 2DEG underneath. However, the hysteresis related to the charge trapping effect and the stability of the fluorine ions in the AlGaN/GaN structure are still practical concerns for this method [123, 124].

Finally, the p-GaN/AlGaN gate (figure 6(d)) is an alternative promising technique to achieve a positive threshold voltage [125–127]. The presence of a p-type layer elevates the band diagram in the AlGaN barrier layer, resulting in the depletion of 2DEG at zero bias. A high Mg concentration is required for the desired threshold voltage due to the low ionization ratio of Mg acceptors, however, the crystal quality of GaN may deteriorate with a high Mg concentration [111]. Another feature of the p-GaN gate architecture is the formation of a 'p–i–n' structure across the p-GaN gate, AlGaN barrier, and the GaN channel, which injects additional holes and increases the current capabilities [128]. Additionally, the hole injections assist in de-trapping the electrons captured at the surface states near the drain edge. This helps mitigate current collapse in the device [129], a phenomenon in which the channel resistance increases and current decreases when a high voltage is applied and diminishes the efficiency.

2.3.1.5. Vertical transistors

Despite the excellent conductivity offered by the high carrier density as well as high mobility in GaN HEMTs, vertical configuration transistors are typically favored in power switch applications for higher current density, voltage scalability, and better suppression of the peak electric field.

The vertical trench MOSFET (figure 7(a)) was reported first during the early stages of research due to its relatively easy process in GaN technology. Normally-off operation and tuning of the threshold voltage are possible in trench MOSFETs by adjusting the doping concentration of the p-type buried layer and by choosing the gate dielectric material and thickness. Otake *et al* demonstrated a vertical V-shape trench MOSFET, with a threshold voltage of 5.1 V [130]. In 2015, Oka *et al* reported a 1.2 kV-class trench MOSFET with a specific on-resistance of 1.8 $m\Omega \cdot cm^2$ by using field plate edge termination in conjunction with a hexagonal trench gate layout [131]. The low channel mobility arising from the etched semiconductor/gate dielectric interfaces was shown to significantly degrade the on-state performance of the GaN trench MOSFET. To address this issue, the GaN interlayer-based trench MOSFET (OG-FET), as shown in figure 7(b), was proposed and prototyped by Gupta *et al* [132, 133]. The OG-FET incorporated a thin unintentionally doped (UID) GaN interlayer grown at the sidewall of the trench followed by an *in-situ* gate dielectric deposition. The regrown channel offered higher mobility by reducing impurity and interface state scattering. Ji *et al* reported an OG-FET with a channel mobility of 185 $cm^2\ (V \cdot s)^{-1}$, resulting in an on-resistance of 2.2 $m\Omega \cdot cm^2$ for a 1.4 kV transistor enabled by the double FP design [134]. Recently, Tanaka *et al* demonstrated a 1.2 kV vertical GaN MOSFET based on an all-planar ion implantation process without etch [135].

Unlike the trench MOSFET, a current aperture vertical electron transistor (CAVET), shown in figure 7(c) takes advantage of the high mobility of a 2DEG, offering lower on-state resistances and higher current capabilities [136, 137]. CAVETs usually operate under normally-on conditions due to the existence of the

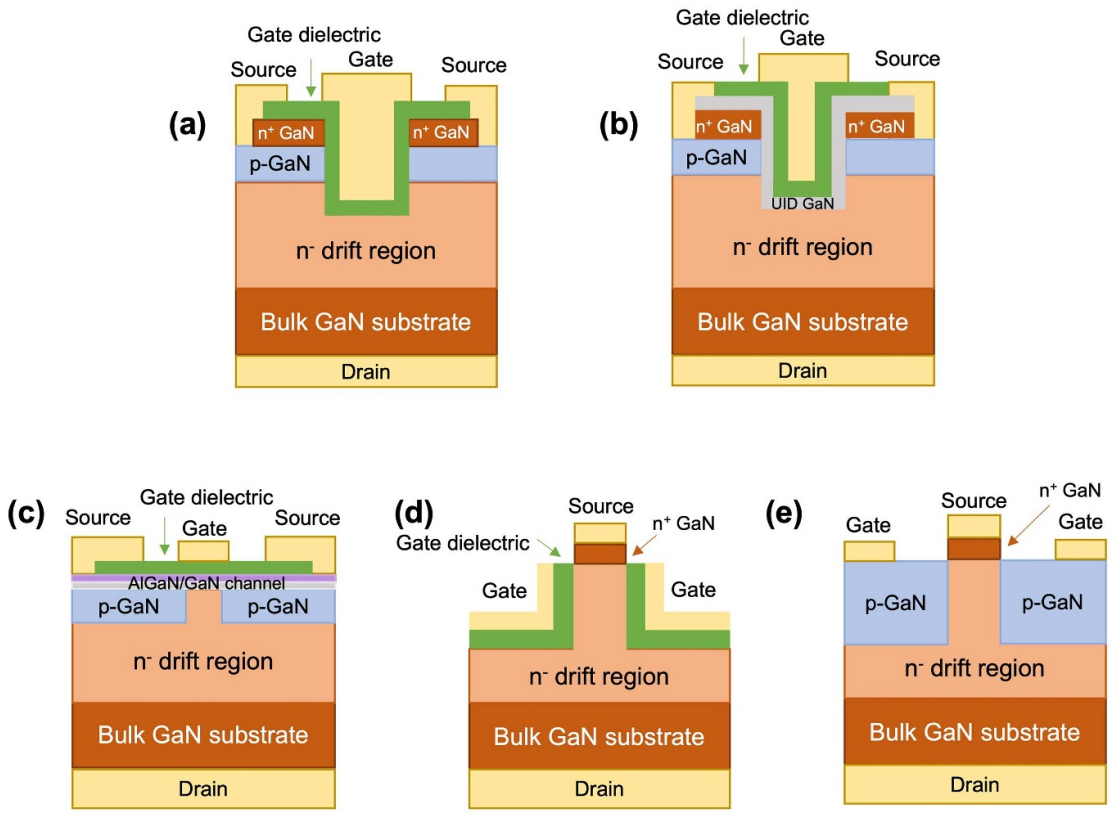

Figure 7. Schematic view of different architectures of vertical GaN transistors: (a) GaN trench MOSFET; (b) GaN interlayer-based trench MOSFET (OG-FET); (c) GaN current aperture vertical electron transistor (CAVET); (d) GaN FinFET; (e) GaN junction field-effect-transistor (JFET).

2DEG; however, normally-off devices can be achieved by adopting similar process techniques used for HEMTs, as mentioned in section 2.3.1.4 [138, 139]. In a CAVET, the current blocking layer is the key to obtaining a high breakdown voltage [140]. An active buried p-GaN layer is ideal for this and allows for avalanche capability; however, from a processing perspective, it is difficult to obtain due to the lack of a mature ion implantation process. Therefore, regrowth of the channel in the aperture is usually required for fabricating CAVETs. Shibata *et al* demonstrated a normally-off CAVET with a p-GaN gate, offering 1.7 kV breakdown voltage and 1 $m\Omega{\cdot}cm^2$ specific on-resistance [141], consequently justifying this device design. Carbon-doped semi-insulating GaN has also been studied as a current blocking and channel layer in vertical GaN transistors [142]. A recent demonstration of a GaN vertical transistor with a semi-insulating channel achieved an on–off ratio of 10^7 and only marginal trapping effects under 200 ns pulsed mode operation [143]. The growth and integration of a semi-insulating GaN layer may open alternative pathways in designing novel device configurations for vertical GaN transistors.

More recently, transistors utilizing a fin structure (often referred to as GaN-FinFETs), shown in figure 7(d) were prototyped [144–146]. Without the need for a p-type GaN layer, a sufficiently thin fin-shaped channel can be well controlled simply by electrostatic modulation of the gate. For that reason, normally-off operation can be achieved by narrowing the fin width and lowering the doping concentration in the fin. The GaN FinFET exhibited excellent on-state performance due to high electron mobility in the bulk GaN crystal. 1200 V class FinFETs have been demonstrated by Zhang *et al* with low on-resistance and normally-off behavior; however, these devices suffered from catastrophic breakdown [145]. The junction field-effect transistor (JFET), a subset of FinFETs in GaN is shown in figure 7(e). In this device, p-type GaN is regrown surrounding the n-type fin channel and pinches off the channel by expanding the depletion region of the PN junction. JFETs avoid the possible oxide reliability issues in an MOS structure, encouraging avalanche in a three-terminal device. A 1.2 kV GaN JFET was reported by Liu *et al* using nitrogen implantation termination [147]. This design exhibited robust avalanche capability up to 200 °C, showing great potential in medium-voltage power applications [148].

2.3.2. RF devices

2.3.2.1. RF and mm-wave HEMTs

Due to its WBG, high electron mobility, and saturated electron velocity, GaN offers obvious advantages for high-power and high-frequency transistors in terms of output power and efficiency [149]. The formation of a 2DEG channel at the AlGaN/GaN interface, characterized by high sheet carrier density and high electron mobility, leads to reduced channel resistances and enhanced current capabilities. This makes GaN superior to SiC, particularly in high-frequency applications, even though both materials exhibit similar breakdown properties. However, the absence of a process to grow bulk GaN hindered the development of GaN devices and slowed down its technological maturation. GaN technology witnessed a resurgence of interest when the first GaN LEDs were developed in 1993 by Nakamura *et al* [150] sparking a global competition for the advancement of the field. The development of LEDs not only propelled the GaN market but also facilitated breakthroughs in the RF domain, particularly with the introduction of the first microwave GaN power HEMT in 1996 and the debut of the first GaN monolithic microwave integrated circuit (MMIC) occurring in 2000 [151].

Among the many challenges faced by GaN RF electronics, thermal management became of high importance in high-power GaN monolithic MMICs as this issue hindered amplifier efficiency and reliability. This concern was mitigated through the introduction of SiC semi-insulating substrates during the growth of GaN HEMTs, boasting a TC that was seven times greater than that of GaAs, and ultimately enabled record power densities exceeding 10 W mm^{-1} [152]. Initial demonstration of GaN devices showcased a tenfold improvement in output power density performance relative to Si laterally-diffused metal–oxide–semiconductor (LDMOS) devices, which offered an output power density of 1 W mm^{-1} [153].

Process innovation and novel device design to combat current collapse consume a large fraction of the current research efforts in GaN HEMTs. The surface states on top of the AlGaN layer constitute the source of the electrons in the 2DEG channel, however, trapping effects related to these surface states are believed to be one of the major causes of current collapse (also referred to as dispersion) [154, 155]. There are three major technical routes to suppress this dispersion, which severely degrades the RF output power of GaN HEMTs. The first approach is the introduction of a passivation layer. Employing SiN_x was demonstrated to effectively reduce the surface states and led to a significant improvement of output power up to 11.2 W mm^{-1} at 10 GHz [156, 157]. Another method is the adoption of field plate technology [152, 158], which enabled the record output power of 41.4 W mm^{-1} at 4 GHz and 30.6 W mm^{-1} at 8 GHz in GaN HEMTs (figures 8(a) and (b)) [159, 160]. The double field plate not only mitigated dispersion effects but also helped in reducing the peak electric field at the drain-side edge of the gate. The third way to address the dispersion phenomenon is at the epitaxial level, by growing a thick capping layer on top of the AlGaN/GaN channel [161, 162]. The thick capping layer increases the distance from the surface to the channel, thus reducing the trapping effects related to the surface states. The capping layer is usually combined with recessed gate technology to achieve good gate control [163]. By effectively suppressing the gate leakage using fluorine plasma treatment of the recessed gate region, 17.8 W mm^{-1} at 4 GHz was achieved even without a SiN_x passivation layer [164].

Gate length scaling is the most straightforward way to push the operating frequency towards the Ka-band (26–40 GHz) and beyond. Thus, a GaN HEMT utilizing a T-shaped gate with a small gate length of 160 nm exhibited a power density of 10.5 W mm^{-1} at 40 GHz with a power added efficiency (PAE) of 33% [166]. Furthermore, the optimization of the deposition condition of the gate dielectric and the plasma treatment were proposed to passivate the surface states and reduce the gate leakage in HEMTs [167–170]. A HEMT with a thin SiN_x gate dielectric layer grown by plasma-enhanced atomic layer deposition (PEALD) showed a significant reduction in reverse leakage and enhanced breakdown voltage, leading to a 7.16 W mm^{-1} of output power density and a PAE of 60.3% at 28 GHz [171].

While a shorter gate length works effectively to further scale down the GaN HEMT towards higher frequency operation, a high aspect ratio (gate length to the gate-to-channel distance) must be maintained to suppress the short-channel effect [172]. An AlGaN/GaN HEMT adopting a 6 nm AlGaN barrier and a 60 nm gate length showed a current gain cut-off frequency (f_T) of 190 GHz and a maximum oscillation frequency (f_{max}) of 227 GHz [173]. However, changing the AlGaN barrier to a material with a stronger polarization effect, such as InAlN and AlN, was predicted to achieve a higher frequency [174]. A f_T up to 454 GHz has been demonstrated with a 3.5 nm AlN barrier layer and 20 nm gate length [175]. The success of the small-signal characteristics at these high frequencies is not the whole story, the large-signal performance, including the output power and the PAE, must also be validated for a GaN HEMT. GaN HEMT technologies utilizing the Ga-polar orientation have demonstrated good performance with 1.7 W mm^{-1} of output power density and 19.1% PAE at 95 GHz [176]. Similarly, at 86 GHz, a W-band Ga-polar GaN HEMT with an output power of 3.6 W mm^{-1} and 12.3% PAE was demonstrated [177].

With recent improvements in the epitaxial growth of N-polar GaN, N-polar GaN HEMTs have demonstrated some of the highest power densities at mm-wave frequencies, outperforming their Ga-polar

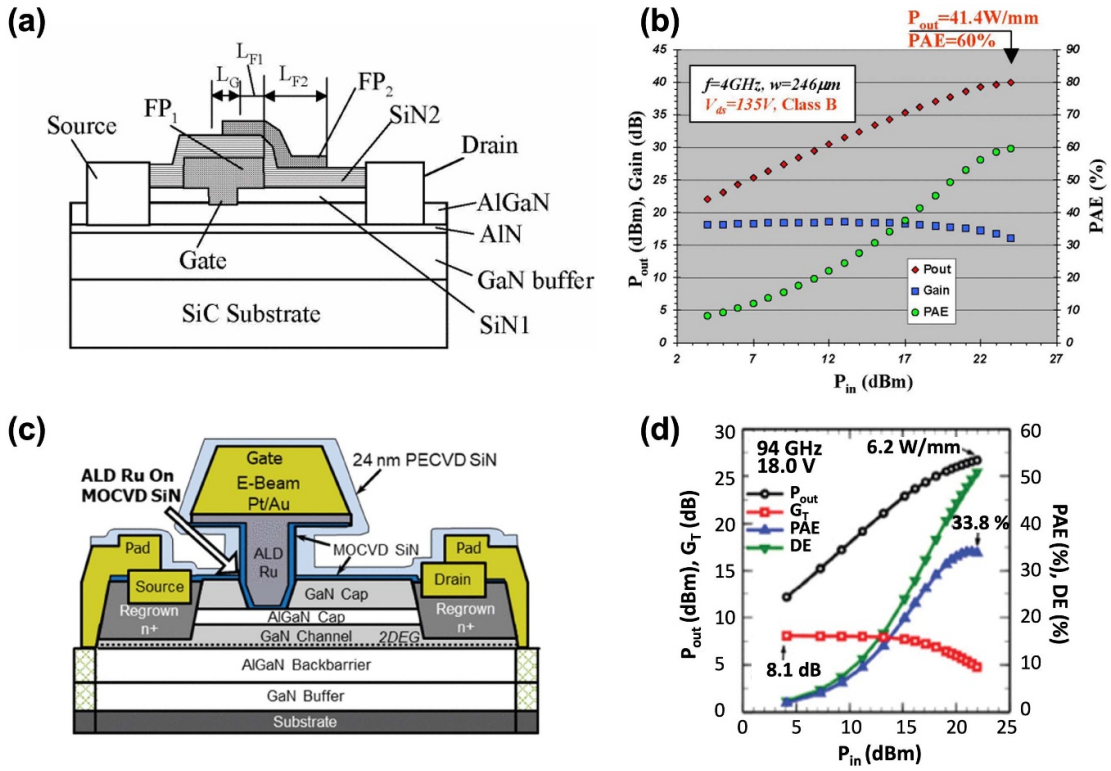

Figure 8. (a) Schematic structure of the double field plated GaN HEMT; (b) power sweep of the double field plated GaN HEMT achieving 41.4 W mm^{-1} power density at 4 GHz with 16 dB associated large signal gain and 60% power added efficiency (PAE) [160]; (c) schematic structure of an N-polar GaN deep recess MIS-HEMT with atomic layer deposition Ru as gate metal; (d) output power (P_{out}), linear transducer gain (G_T), PAE, and drain efficiency (DE) measured as a function of input power (P_{in}) at 94 GHz with quiescent bias conditions of 500 mA mm^{-1} $I_{DS,Q}$ and 18 V $V_{DS,Q}$ [165].

counterparts. The advantages of N-polar structures include higher scalability, lower resistivity ohmic contacts, lower gate capacitance, and a more effective back barrier. 8 W mm^{-1} output power at 94 GHz with a PAE of 28.8% has been achieved in an N-polar GaN HEMT using a self-aligned foot gate process [178]. Atomic layer deposited (ALD) Ru was shown to effectively fill in the T-shaped gate trench to help realize shorter gate length below 60 nm and minimize the gate resistance, giving rise to an output power density of 6.2 W mm^{-1} with a high PAE of 33.8% at 94 GHz (figures 8(c) and (d)) [165]. A record-high 9.65 dB linear transducer gain and demonstrated 42% PAE with associated 4.4 W mm^{-1} of output power density at 94 GHz have also been demonstrated for N-polar HEMTs on sapphire substrates [179].

2.3.2.2. Impact ionization avalanche time transit diodes (IMPATTs)

IMPATTs are powerful solid-state sub-THz sources in fundamental mode. When properly packaged, these devices can replace elaborate amplifiers and multiplier chains and offer exceptionally high output power at remarkably high frequencies. The output power in IMPATTs comes from the phase difference in voltage and current, caused by the time delay from carrier avalanche multiplication and transition through the drift region. To the first order, the operation frequency is inversely proportional to the thickness of the depletion region (W_{dep}), determined by $f_{opt} = \frac{v_{sat}}{2W_{dep}}$, and the operation voltage is set by the critical field of the material. Much higher performance is expected for GaN-based IMPATT diodes compared to Si and GaAs-based due to their high critical field and high electron saturation velocity. Owing to the advancement of low dislocation density bulk GaN growth, avalanche in GaN PN diodes is now more routinely achieved. Ji *et al* first demonstrated a GaN IMPATT diode as a series resonant oscillator, showing an oscillation frequency at 800 MHz [180]. Limited by the avalanche current and the lack of a heat sink, the frequency was much below the theoretical predictions. Later, Kawasaki *et al* mounted the GaN IMPATT diode on a copper heat sink in a pill package and operated the device under 500 ns pulse mode (figure 9) [181]. The device showed a maximum oscillation frequency of 9.5 GHz at a current density of 2.2 kA cm^{-2}, offering a peak output power of 14.45 mW. More recently, by decreasing the junction diameter and capacitance, more than 30 dBm output power was achieved up to 21 GHz by Kawasaki *et al* [182]. Further reduction of the series resistance and higher biasing current are expected to improve the device performance at higher frequencies.

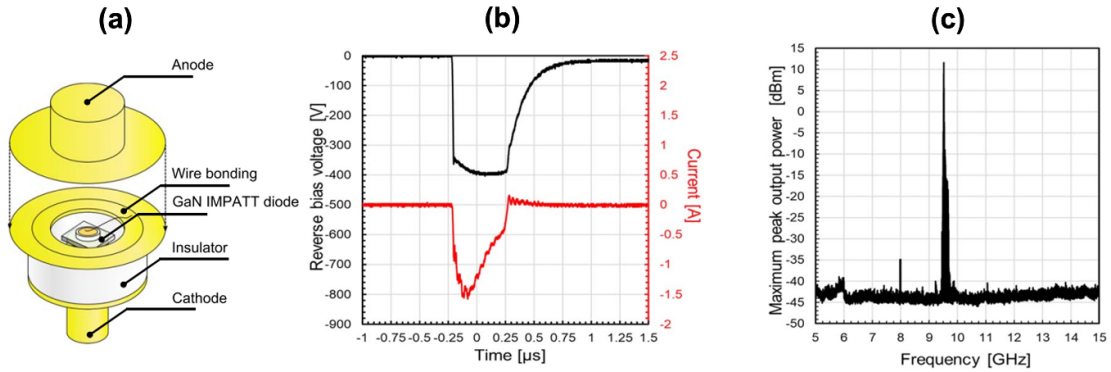

Figure 9. (a) Schematic view of a pill-packaged GaN IMPATT diode; (b) transient waveform for the input pulse bias during operation; (c) output power spectrum at the input bias shown in (b) [181].

3. Aluminum gallium nitride/aluminum nitride (AlGaN/AlN)

3.1. Material properties

From GaN, we transition into the UWBG materials family starting with AlGaN, another III–V material. AlGaN alloys with varying Al mole fractions are promising due to their tunable bandgaps spanning a wide range, from 3.4 to 6.0 eV. The material band gap increases as Al composition increases until 100% to form AlN. Higher critical electric fields can enable device operation with lower leakage current and higher breakdown voltages [183–185]. Thus, AlGaN with higher a Al composition is of high interest. At the opposite extreme of GaN, AlN has one of the widest direct bandgaps of 6.0 eV, generating significant attention for applications in UV optoelectronics. The large bandgap of AlN leads to a high critical electric field of 15.4 MV cm^{-1}, and a very high TC (highest reported 321 W $(m{\cdot}K)^{-1}$ [186]), which is naturally appealing for power and RF electronics as well.

Similar to GaN, a 2DEG is formed at an AlGaN/AlGaN interface (with two different AlGaN compositions) without any intentional doping due to polarization-induced charges. The 2DEG mobility in different AlGaN channels varies based on the Al composition of the channel, and the barrier material and is dominated by alloy scattering. For example, MBE-grown HEMTs with $Al_{0.06}Ga_{0.94}N$ and $Al_{0.15}Ga_{0.85}N$ channels were reported to have 2DEG mobilities of 590 cm^2 $(V{\cdot}s)^{-1}$ [187] and 430 cm^2 $(V{\cdot}s)^{-1}$ [188], respectively. While the mobility values are lower than in GaN 2DEG channels, higher breakdown voltages are expected with increasing Al mole fractions [189]. For example, assuming the critical electric field of GaN to be 3 MV cm^{-1}, >9 MV cm^{-1} was estimated for a 75% Al mole fraction AlGaN channel.

In AlN, the highest room temperature bulk electron mobility measured is 426 cm^2 $(V{\cdot}s)^{-1}$ with a Si doping concentration of 3×10^{17} cm^{-3}, and 125 cm^2 $(V{\cdot}s)^{-1}$ was achieved in more highly doped AlN (10^{18} cm^{-3}) [190]. Previously, the same group measured a value of only 125 cm^2 $(V{\cdot}s)^{-1}$ at low doping concentrations on the order of 10^{15} cm^{-3}. The vast mobility improvement was attributed to the decreased number of threading dislocations realized by suppressing the parasitic reaction of Al and N sources during growth.

3.2. Growth and doping

3.2.1. Bulk AlN growth

Among the different polymorphs of AlN, the wurtzite crystal structure, first reported by Heinrich Otto in 1924, is most commonly studied for both bulk and epitaxially grown AlN [191]. For the growth of bulk AlN single crystals, HVPE [192] and physical vapor transport (PVT) [193] are two of the most widely used methods. Typically, AlN crystals are difficult to grow using common crystal growth methods such as pulling and hot melt [194] due to their high melting point of 2800 °C and dissociation pressure of 20 MPa. While both the HVPE and PVT methods have been utilized to grow thick AlN films with low screw dislocation density (of the order 10^3 cm^{-2}) [195], HVPE growth is significantly slower in comparison to PVT methods [196]. Thus, PVT methods are predominantly used in the growth of bulk AlN substrates due to their simpler and safer growth process, faster growth rate, and good crystal integrity. Two PVT approaches are primarily used: growth of thick AlN on 4H–/6H–SiC substrates [197–199] shown in figure 10(a) and spontaneous nucleation followed by freestanding AlN growth [200, 201]. A detailed study of PVT-AlN growth on SiC templates for varying growth temperatures and orientations of SiC further exhibited that off-axis Si-face SiC

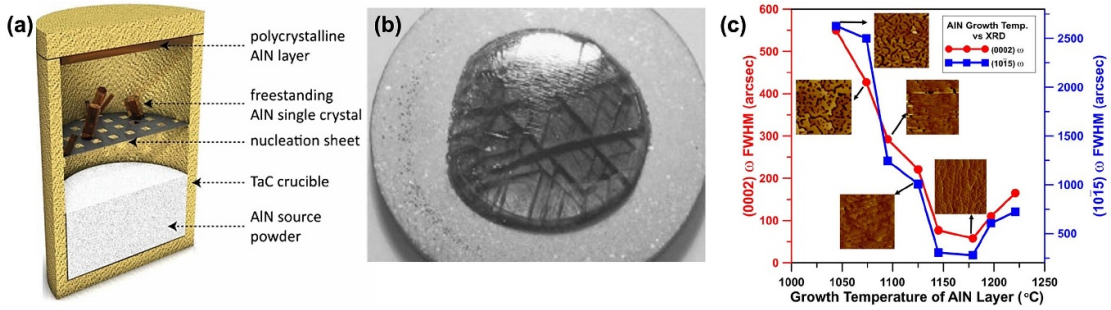

Figure 10. (a) Crucible design for spontaneous nucleation used for bulk AlN growth by physical vapor transport method [199]; (b) top view of grown AlN layer using sublimation growth method [194]; (c) symmetric (0002) and asymmetric (1 0^{-}1 5) x-ray diffraction analysis (XRD) scans of AlN layers grown at various growth temperatures (1045 °C–1220 °C) with nucleation layer (grown at 850 °C) with atomic force microscopy (AFM) surface morphologies at each temperature [205].

offers a flat morphology and better crystalline quality [202]. The largest AlN wafer prepared by PVT to date is 40 mm in diameter with a low impurity concentration of <0.01% [197, 203].

3.2.2. Epitaxial growth of AlN

To achieve epitaxial growth of AlN, several methods, including MOCVD, MBE, pulse laser deposition (PLD), and sputtering have been demonstrated. The MOCVD method is suitable for mass production because of its low deposition temperature and wide growth temperature range [204]. Using MOCVD, high-quality AlN homoepitaxy with low background impurity concentration was demonstrated on single crystal AlN substrates [193]. Thick (∼2 μm), crack-free AlN growths with high crystalline quality, shown in figure 10(c), were also achieved on sapphire substrates via a sandwich method [205] and by using a patterned sapphire substrate [206]. Epitaxial lateral overgrowth-AlN layers with low crack and threading dislocation densities have also been reported to grow on thin, stripe-patterned AlN seed layers directly deposited on Si (111) substrates [207].

The epitaxial growth of AlN using MBE is limited to a slow growth rate; however, the growth process is easier to control. Using MBE, the growth of AlN on a sapphire substrate was improved to yield a better surface morphology via a nitridation step [208]. Additionally, smooth and strain-free AlN was grown by MBE directly on a Si substrate with a nanowire template [209]. The PLD method is used for the growth of thinner AlN films with good crystallinity and stoichiometry at relatively low temperatures of 800 °C [210, 211]. Under optimum growth conditions, a single-crystal AlN layer as thin as ∼1.5 nm was demonstrated on a Si substrate [212]. For large-area deposition of AlN films, the sputtering method comes with the advantages of a simpler process and lower cost. Using RF reactive sputtering, AlN layers were directly grown on a *c*-axis sapphire substrate, and crystalline quality was found to improve with increasing nitrogen gas fraction during reactive sputtering and RF power [213].

3.2.3. Epitaxial growth of AlGaN

Following the realization of high-quality GaN grown on low-temperature AlN buffer layers in 1986 [46], the growth of AlGaN and AlGaN/GaN heterojunctions gained significant attention over the past three decades with vast application prospects in high temperature, high power, RF, and optoelectronic devices [214–217]. AlGaN films were first grown as buffer layers for the growth of GaN or AlN epilayers. Following the enhanced understanding of the growth mechanism and optimized growth process over the years, the quality of the AlGaN films was improved by adopting epitaxial growth techniques such as MBE [218] and MOCVD [219]. For example, an $Al_{0.2}Ga_{0.8}N$ layer grown at 1050 °C was demonstrated with the insertion of low-temperature AlGaN interlayers using MOCVD. This resulted in the simultaneous reduction of tensile stress and crack formation, which is typically observed from the growth of high-temperature AlGaN directly on GaN epilayers [220]. Fully relaxed, crack-free, 1.3 μm thick $Al_{0.32}Ga_{0.68}N$ layers were reported on GaN-on-porous-GaN pseudo-substrates (figure 11(a)) [221]. Moreover, UID AlGaN epilayers graded over Al compositions of 80%–90% and 80%–100% were also demonstrated using MOCVD [222]. Process condition optimizations such as low temperatures and ammonia-rich conditions were used to increase the growth rate of AlGaN up to 3.2 μm h^{-1} [223]. Concurrently, the Al composition was found to be affected by the growth temperature and growth rate.

The HVPE method is also used for the growth of AlGaN with low threading dislocation densities and smoother surfaces. The epitaxial growth of $Al_{0.10}Ga_{0.90}N$ on an AlN/nanopatterned sapphire substrate (NPSS) template by HVPE resulted in a low threading dislocation density of 1.4 × 10^{9} cm^{-2} of the AlGaN

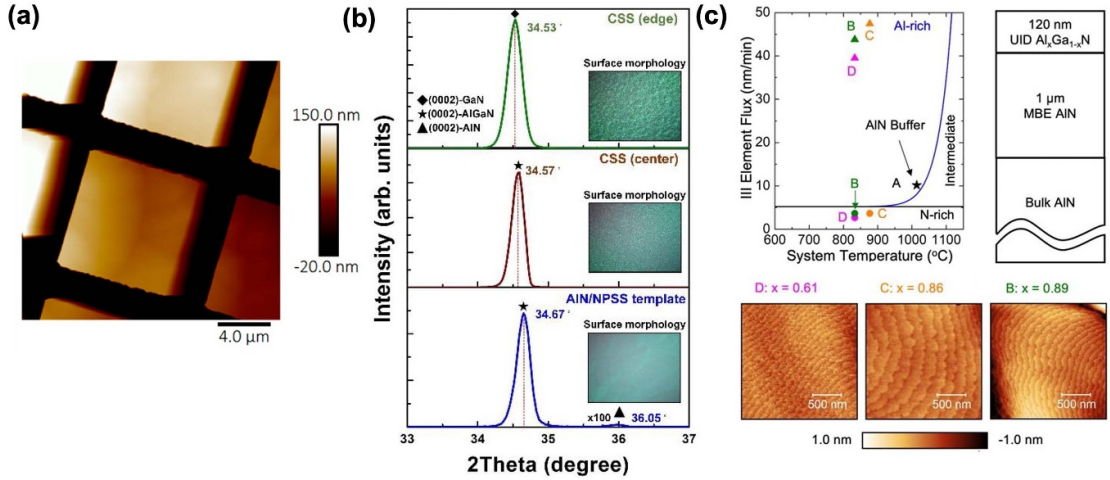

Figure 11. (a) 20 × 20 μm^2 AFM height images of 1.3 μm $Al_{0.32}Ga_{0.68}N$ grown on 10 × 10 μm^2 tiles of compliant pseudo-substrate [221]; (b) XRD scan patterns of the $Al_{0.10}Ga_{0.90}N$ grown on a conventional sapphire substrate (CSS) edge, CSS center, and AlN/nanopattered sapphire substrate (NPSS) templates by HVPE [224]; (c) AlGaN guideline map and AlN growth phase diagram for MBE. The black star indicates the buffer Al-rich AlN growth condition. Circles are the Al flux used in the AlGaN layers, and triangles are the total metal flux ($F_{Al} + F_{Ga}$) during AlGaN growth. The layer structures of the MBE-grown AlGaN and AlN on the bulk AlN substrate are shown with the 2 × 2 μm^2 AFM images of x = 0.61, 0.86, and 0.89 Al content UID-$Al_xGa_{1-x}N$ grown on bulk AlN substrates [226].

epilayer owing to in-plane stress relaxation [224]. Further process optimization in HVPE such as etching to suppress parasitic reactions was explored to achieve thick n-AlGaN cladding layers and free-standing AlGaN substrates on both GaN and AlN templates [225]. MBE-grown AlGaN alloys with high mole fractions of Al on single-crystal AlN substrates were also reported and shown in figure 11(c). For example, pseudomorph $Al_xGa_{1-x}N$ epitaxial layers with x ~0.6–1.0 were grown using MBE at a growth rate of 0.3 μm h^{-1} [226].

3.2.4. Doping in AlGaN/AlN

For the successful adoption of UWBG materials in technologically relevant applications, doping and its controllability are regarded as cornerstones. Doping of AlGaN is difficult to achieve compared to GaN, and the ability to dope such alloys significantly decreases with increasing Al content. This can be attributed to the fact that most dopant ionization energies increase with bandgap, therefore decreasing the fraction of free carriers that are thermodynamically activated [3]. For AlGaN/AlN, doping strategies that exploit broken crystal symmetries, such as polarization induced doping are useful for supplementing the traditional chemical substitutional doping. Modulation doping is also utilized for enhancing the number of confined carriers in the material system. Several p-type doping approaches, such as superlattice doping [227], Mg delta doping [228], and Mg–Si alternative co-doping [229] have been investigated for improving the doping efficiency of Al-rich AlGaN. Using Mg delta doping, a hole concentration of 8.3 × 10^{18} cm^{-3} with Mg doping concentration of 1.6 × 10^{19} cm^{-3} was achieved, indicating a doping efficiency of up to 51.9% [230]. On the other hand, Si is primarily used as the n-type dopant for AlGaN with high Al content [231], including AlN. For example, Taniyasu *et al* demonstrated n-type conduction in Si-doped AlN showing a room temperature Hall mobility of 426 cm^2 V^{-1} s^{-1} and electron concentration of 7.3 × 10^{14} cm^{-3}. The study also demonstrated p-type conduction in Mg-doped AlN with a Mg concentration of 2 × 10^{20} cm^{-3} and thermally annealed at 800 °C for 10 min. Beyond 2 × 10^{20} cm^{-3} concentrations, Mg doped AlN becomes highly resistive due to a self-compensation effect [232], a phenomenon also found in n-type Si doped AlN. Typically, an increase in the Si content leads to an increase in free electrons; however, this trend does not continue at higher doping levels. A further increase in the Si concentration leads to a decrease in the free electron concentration, commonly referred to as the compensation knee [232–234]. A variety of compensating defects can be the culprit, but the mechanism and identity of these defects have not been conclusively determined yet. Researchers have tried different dopants as well, and successful experimental achievement of both n-type AlN:Si films using the metal modulated epitaxy (MME) method and p-type AlN:Be films was demonstrated [235].

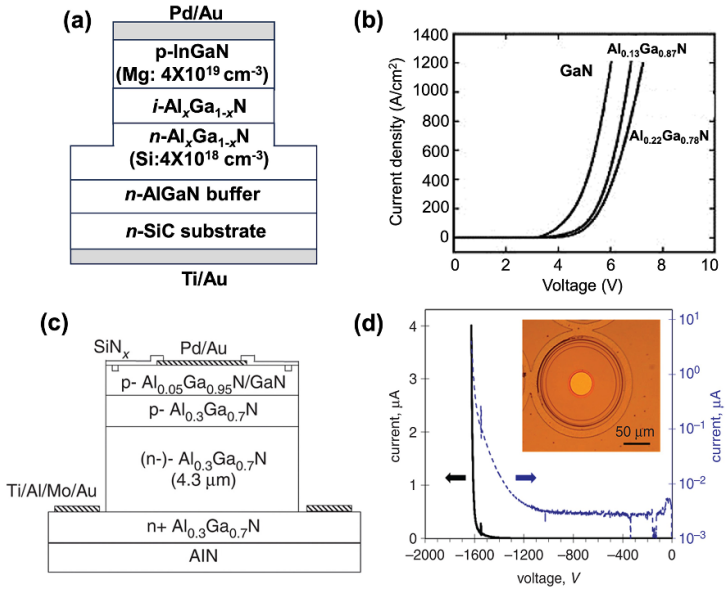

Figure 12. (a) Schematic illustration of the p-InGaN/i-$Al_xGa_{1-x}N$/n-$Al_xGa_{1-x}N$ diode structure; (b) forward I–V characteristics of the diodes with different Al compositions at RT [236]; (c) schematic illustration of a $Al_{0.3}Ga_{0.7}N$ PN diode and (d) reverse current–voltage characteristics of the $Al_{0.3}Ga_{0.7}N$ PN diode showing breakdown voltage of 1627 V (inset—an optical image of processed diode with 50 μm diameter p-contact metal) [237].

3.3. AlGaN devices and applications

3.3.1. High power devices

3.3.1.1. PIN diodes

The larger bandgaps of AlGaN compositions are promising for offering extremely low reverse leakage currents and exceptionally high breakdown voltages in AlGaN-based PIN diodes. In 2006, Nishikawa *et al* demonstrated metal-organic vapor phase epitaxy (MOVPE)-grown AlGaN PIN diodes with intrinsic layers of unintentionally doped $Al_{0.13}Ga_{0.87}N$ and $Al_{0.22}Ga_{0.78}N$, separately [236]. The PIN structure was grown on a conductive n-SiC substrate and capped by a p-InGaN layer that helped to reduce the ohmic contact resistances. Using only a ∼225 nm thick intrinsic layer, the $Al_{0.22}Ga_{0.78}N$ diode offered a breakdown voltage of 78 V with an on-resistance of 1 m$\Omega\cdot$cm^2, while the reference GaN diode exhibited a lower breakdown voltage of 54 V (figures 12(a) and (b)). The corresponding critical electric fields were calculated to be 3.5 MV cm^{-1} and 2.4 MV cm^{-1}, respectively, assuming the intrinsic layer was fully depleted. In 2007, the same group reported another PIN diode with an intrinsic layer of $Al_{057}Ga_{0.43}N$ (225 nm), showing 185 V breakdown voltage resulting in a critical electric field of 8.1 MV cm^{-1}. The maximum BFOM was shown with 30% of Al composition because of the tradeoff between breakdown voltage and on-state resistance and is twice as high as that for GaN-based diodes, showing promise for high-power operation in AlGaN-based devices [214].

In 2016, MOVPE-grown $Al_{0.3}Ga_{0.7}N$ quasi-vertical PN diodes on a non-conductive sapphire substrate were reported where a remarkably low reverse leakage current of <3 nA was achieved. The breakdown voltage for this diode was 1600 V with an estimated critical electric field of 5.9 MV cm^{-1} (figures 12(c) and (d)). As a comparison, an ideal planar GaN PN diode with the same breakdown would require a ∼7 μm-thick drift region with a background carrier concentration of $<2.4\times10^{16}$ cm^{-3} [237]. A specific on-resistance of 16 m$\Omega\cdot$cm^2 was reported at a current density of 1.5 mA cm^{-2}. The relatively high resistance was a consequence of the n-type contact layer in the front-contacted device geometry, but comparable with 14 m$\Omega\cdot$cm^2 reported for a GaN PN diode grown on sapphire [238].

3.3.1.2. HEMTs

In power electronics, vertical device structures are typically favored for areal efficiency and elimination of surface state effects. Nonetheless, lateral device structures in U/WBG materials are still important, as seen in GaN-channel HEMTs, due to the advantage of higher channel mobility. Previously, the role of AlGaN in AlGaN/GaN HEMTs was introduced. Here, only fully $Al_xGa_{1-x}N$ structures will be discussed. Both lateral and vertical AlGaN device structures are still in their infancy, but lateral devices are more readily achievable due to existing bulk growth limitations. The growth and device optimization of AlGaN channel HEMTs have been reported in several studies. A HEMT structure of $Al_{0.53}Ga_{0.47}N/Al_{0.38}Ga_{0.62}N$ achieved a maximum breakdown voltage of 1650 V with a gate to drain distance of 10 μm [215]. In 2010, an AlGaN-channel

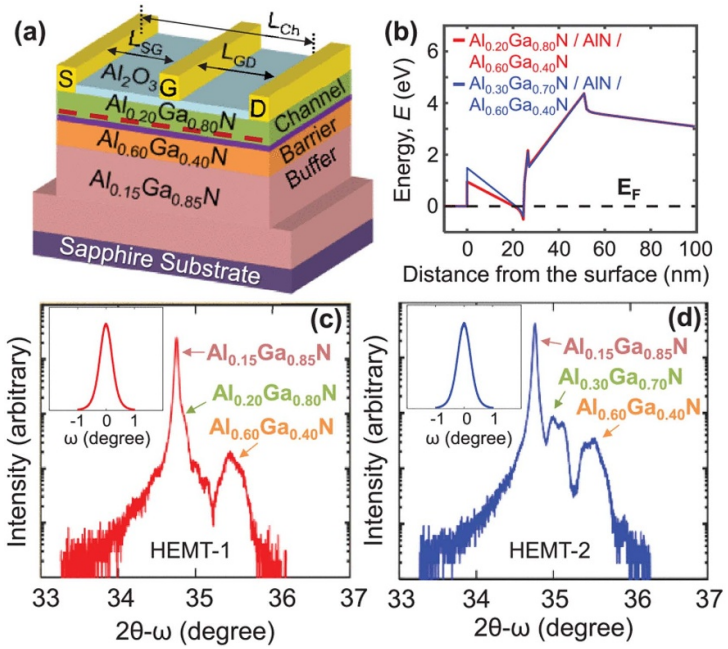

Figure 13. (a) Schematic of all-AlGaN N-polar HEMT device with an $Al_{0.20}Ga_{0.80}N$ channel layer and an $Al_{0.30}Ga_{0.70}N$ channel layer; (b) the simulated band diagrams of $Al_{0.20}Ga_{0.80}N$ channel and $Al_{0.30}Ga_{0.70}N$ channel HEMTs. (c), (d) XRD spectra (2θ-ω scan of (002) plane) of these structures, confirming the stoichiometries of all-AlGaN HEMT structures [189].

HEMT with a high Al composition of over 0.5 ($Al_{0.51}Ga_{0.49}N$) was first reported. The HEMT structure was grown on a free-standing AlN substrate to improve crystalline quality, and the fabricated device exhibited a maximum drain current of 25.2 mA mm^{-1} and a breakdown voltage of 1800 V [239]. A metal stack, composed of Zr/Al/Mo/Au, was found to show low contact resistivity for source and drain ohmic contacts for AlN/AlGaN HEMT with AlN as a barrier layer. This HEMT also demonstrated low degradation of drain current at temperatures from 300 K to 573 K showing stable high-temperature operation [240]. An $Al_{0.85}Ga_{0.15}N$ channel HEMT was demonstrated in 2016 showing a very low off-state leakage current of 10^{-7} mA mm^{-1}. The device's reported breakdown was 810 V, which corresponds to an average field of 0.81 MV cm^{-1}. This is only a fraction of the predicted critical electric field in $Al_{0.85}Ga_{0.15}N$ (13 MV cm^{-1}), due to the immature state of the material [216]. Although most of the reported efforts discuss the investigation of metal polar AlGaN channel based HEMT structures, very recently MOCVD-based growth of N-polar AlGaN channel HEMT structures with varying Al mole fractions in the $Al_xGa_{1-x}N$ channel has been demonstrated [241]. The N-polar all-AlGaN HEMT with 0.2 Al in the channel and 3 μm channel length offered a drive current of 375 mA mm^{-1} while maintaining a low on-state leakage current of ∼0.5 nA mm^{-1} and >400 V breakdown voltage [189], promising for high power electronic applications (figure 13).

3.3.2. RF HEMTs

AlGaN channel based HEMT structures as high-frequency devices have shown significant advancement in the last decade. Raman *et al* demonstrated a low Al composition $Al_{0.06}Ga_{0.94}N$ channel HEMT, which showed an f_T of 13.2 GHz and f_{max} of 41 GHz. At 4 GHz, the output power was 4.5 W mm^{-1} demonstrating the potential of AlGaN channel HEMTs for high-voltage switching and microwave power applications [242]. Bajaj *et al* demonstrated nearly constant f_T and f_{max} profiles in a scaled graded-AlGaN (0%–30% Al) channel with an f_T of 52 GHz and an associated f_{max} of 67 GHz, and the demonstrated flat f_T and f_{max} profiles could help to improve the linearity performance of devices [243]. With a linearly graded AlGaN channel polarization doped field effect transistor (PolFET), X-band power and linearity performance were reported for the first time in 2018 with a third-order output intercept (OIP3) of 33 dBm, and OIP3/P_{DC} (DC power consumption) of 3.4 dB [244]. In 2020, Xue *et al* reported an $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ HEMT with a current density of 900 mA mm^{-1}, f_T of 20 GHz, and f_{max} of 36 MHz. The off-state breakdown voltage in these devices was 80 V with 1 μm gate to drain separation and a gate length of 100 nm [217]. The same group demonstrated an exceptionally low gate leakage current density of 1.4×10^{-8} mA mm^{-1} even at a high forward gate bias of V_{GS} of 12 V, and a current on/off ratio $>10^{10}$ was achieved simultaneously. Small signal measurement showed that the device has an f_T of 3.8 GHz and f_{max} of 4.5 GHz for the same Al compositions [245].

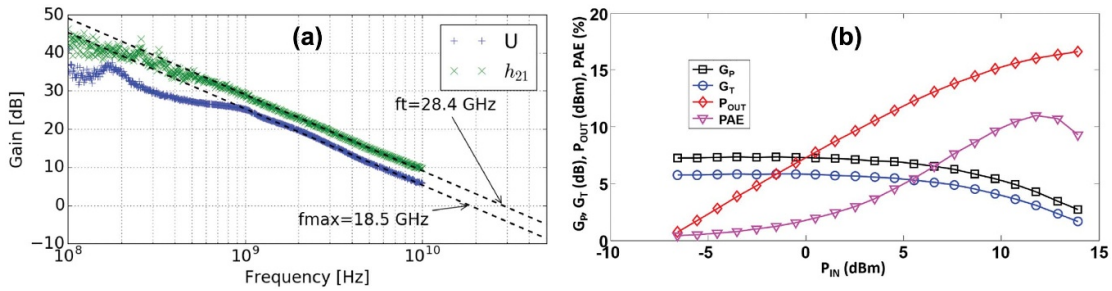

Figure 14. RF performances of a HEMT with an 80 nm gate with both source-to-gate and gate-to-drain spacings of 500 nm: (a) the small-signal gain performance at $V_{GS} = 2.75$ V and $V_{DS} = 20$ V; (b) the 3 GHz class A power sweep for a 2×50 μm^2 HEMT biased with $V_{GS} = 3.75$ V and $V_{DS} = 20$ V [248]. Here, the power gain (G_p), transducer gain, output power, and power-added efficiencies are plotted as a function of input power.

The RF operation of AlGaN channel transistor with Al-composition above 80% was first reported in 2018 demonstrating an impressive current density of 265 mA mm^{-1} for a gate length of 0.8 μm. The reported f_T/f_{max} were 5.4/14.2 GHz respectively [246]. An $Al_{0.75}Ga_{0.25}N/Al_{0.6}Ga_{0.4}N$ HEMT was also reported with a drain current density ($I_{D,\,max}$) of 460 mA mm^{-1} for a gate length of 130 nm. The small signal measurement showed a current/power gain cutoff frequency (f_T/f_{max}) of 40 GHz/58 GHz [247]. Also, $Al_{0.85}Ga_{0.15}N/Al_{0.7}Ga_{0.3}N$ HEMT with 80 nm gate was reported to display a maximum current of 160 mA mm^{-1} with f_T of 28.4 GHz and f_{max} of 18.5 GHz (figure 14) [248].

3.4. AlN devices and applications

3.4.1. High power devices

3.4.1.1. Schottky barrier and PN diodes

In 2015, thick n-type AlN layers were homoepitaxially grown by HVPE on AlN (0001) seed substrates, and a SBD was fabricated using Ni/Au Schottky contacts. High rectification with a turn-on voltage of approximately 2.2 V was observed along with a reverse breakdown voltage of >550 V [249]. Maeda *et al* reported an AlN quasi–vertical SBD fabricated on an AlN bulk substrate. An undoped AlN layer, a Si-doped $Al_{0.9}Ga_{0.1}N$ current spreading layer, and an AlN buffer layer were grown by plasma-enhanced MBE. This device was reported to withstand at least 100 V reverse breakdown voltage; however, the on-resistance was high (1.8 $\Omega \cdot cm^2$) [250]. In 2017, Fu *et al* were the first to demonstrate 1 kV-class AlN SBDs on sapphire substrates grown by MOCVD. The device showed a low turn-on voltage of 1.2 V, a relatively high on/off ratio of $\sim 10^5$, and a low reverse leakage current <1 nA. The devices also exhibited excellent thermal stability over 500 K and a breakdown voltage of ~1 kV without any use of additional edge termination methods (figures 15(a) and (b)) [251]. Researchers have demonstrated few AlN-based PIN diodes as the challenge of growing thick AlN layers remains a primary obstacle in addition to difficulties in doping. Recently, however, an AlN PN diode with a nearly ideal turn-on voltage of ~6 V was demonstrated with a hole concentration of 3.1×10^{18} cm^{-3} and an electron concentration of 6×10^{18} cm^{-3} [235].

3.4.1.2. Metal–semiconductor field effect transistors (MESFETs)

In 2022, Hiroki *et al* reported the first AlN MESFET with epitaxially grown n-type AlN channel layers and achieved an off-state breakdown voltage of 1.72 kV with a 16 μm channel gate to drain distance. This result was attributed to the growth of comparatively low defect AlN using a high-temperature MOCVD with a uniquely designed reactor. To achieve good ohmic contacts, a graded AlGaN layer between AlN and metal electrodes was used. With increasing temperature from room temperature to 500 °C, both on-current and transconductance increased while maintaining a small reverse leakage current of 1.6×10^{-11} A mm^{-1}, leading to a large on/off ratio of $\sim 10^5$ even at 500 °C. The results indicate that AlN MESFETs with epitaxially grown n-type AlN channel layers are promising for high-voltage applications at high temperatures (figures 15(c)–(e)) [233].

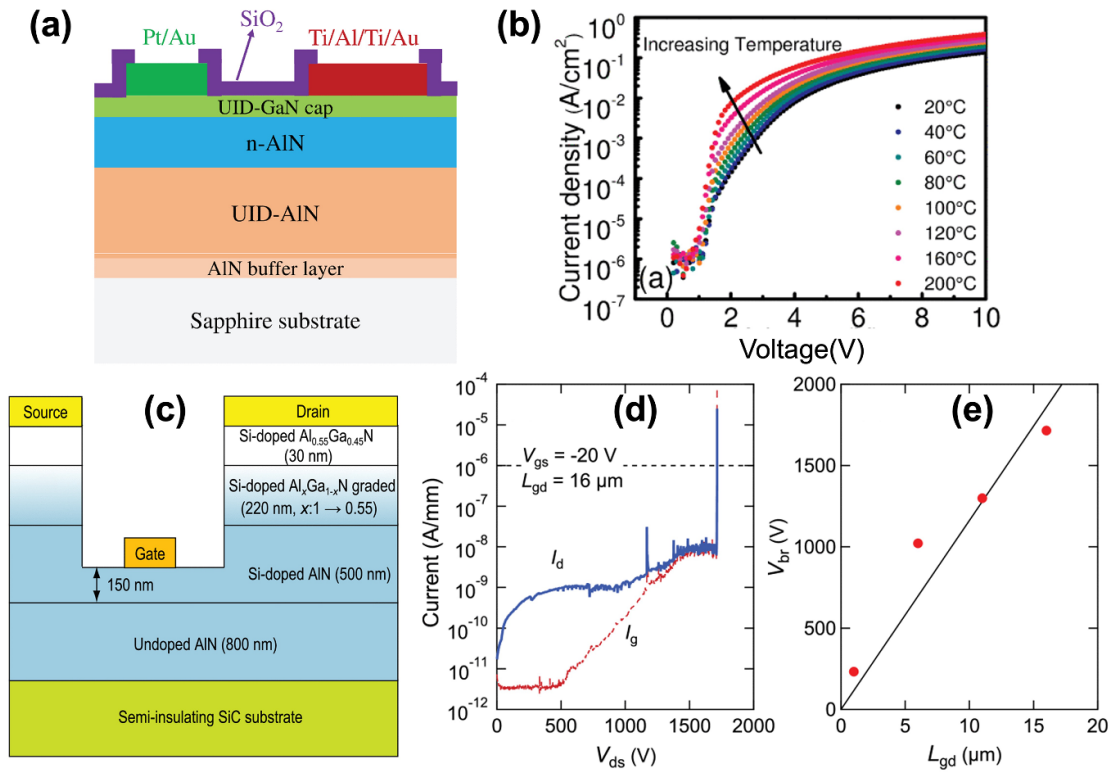

Figure 15. (a) The schematic view of the AlN SBD grown on sapphire by MOCVD and (b) the forward I–V characteristics at different temperatures, which demonstrated 1 kV breakdown voltage [251]; (c) schematic view of the first demonstrated AlN metal–semiconductor field-effect-transistor, (d) the breakdown characteristics for a 16 μm gate-drain length device, and (e) the breakdown voltage as a function of gate to drain length [233].

4. Diamond

4.1. Material properties

As depicted in figure 1(a), diamond has outstanding properties across the board for power and high frequency electronics. Diamond has an indirect band gap of 5.47 eV with an expected ultra-high critical field of >10 MV cm^{-1} at which point it would theoretically breakdown by the avalanche phenomenon [252, 253]. Indicators for avalanche breakdown have been observed by Ohmagari *et al* in PIN diodes which exhibited positive temperature coefficients [254]; however, the observation has not been widely reproduced and further studies are required to better understand the phenomenon.

While high critical field values are expected in all UWBG materials, diamond is unique in that it has both high electron and hole bulk mobilities, unlike in GaN and Ga_2O_3. Using time-of-flight experiments, low field drift mobilities of 3500–4500 cm^2 (V·s)$^{-1}$ and 2600–3800 cm^2 (V·s)$^{-1}$ were extracted for electrons and holes, respectively, and carrier lifetimes were estimated to be >2 μs. The high mobilities were attributed to the high-quality growth of homoepitaxial CVD diamond [255]. These values have been pushed even higher by the extrapolation of time-resolved cyclotron resonance measurements of ultrapure diamond to room temperature. This yielded record high mobilities of 7300 and 5300 cm^2 (V·s)$^{-1}$ for electrons and holes [256]. While spectacularly high values have been reported, the average Hall hole mobility measured in boron doped diamond decreases with increasing doping density and temperature. With boron doping concentrations on the order of 10^{15}–10^{17} cm^{-3}, simulated hole mobilities are ~2000 cm^2 (V·s)$^{-1}$, and experimental values fall between 1000 and 2000 cm^2 (V·s)$^{-1}$. From 10^{18}–10^{20} cm^{-3}, the mobility decreases from 1000 to 30 cm^2 (V·s)$^{-1}$ [257]. In n-type diamond, phosphorous doped diamond from 10^{15}–10^{17} cm^{-3} is simulated to have mobilities ~1000–200 cm^2 (V·s)$^{-1}$ and decreases to below 30 cm^2 (V·s)$^{-1}$ above 10^{18} cm^{-3} [258]. The velocity field curves for electrons and holes were shown to be similar at room temperature [259] with the saturation velocity of electrons and holes to be on the order of 1.4–2 × 10^7 cm s^{-1} at an electric field of 10^5 V cm^{-1} [260, 261].

Moreover, diamond's extremely high TC makes it stand out among other UWBG materials. Due to diamond's strong covalent C–C bonding yielding a bond length of only 1.54 Å, heat is effectively dissipated through lattice vibrations with low phonon scattering. As a result, diamond has one of the highest thermal conductivities of semiconductors and insulators, >2200 W (m·K)$^{-1}$, which is 5 times greater than even that

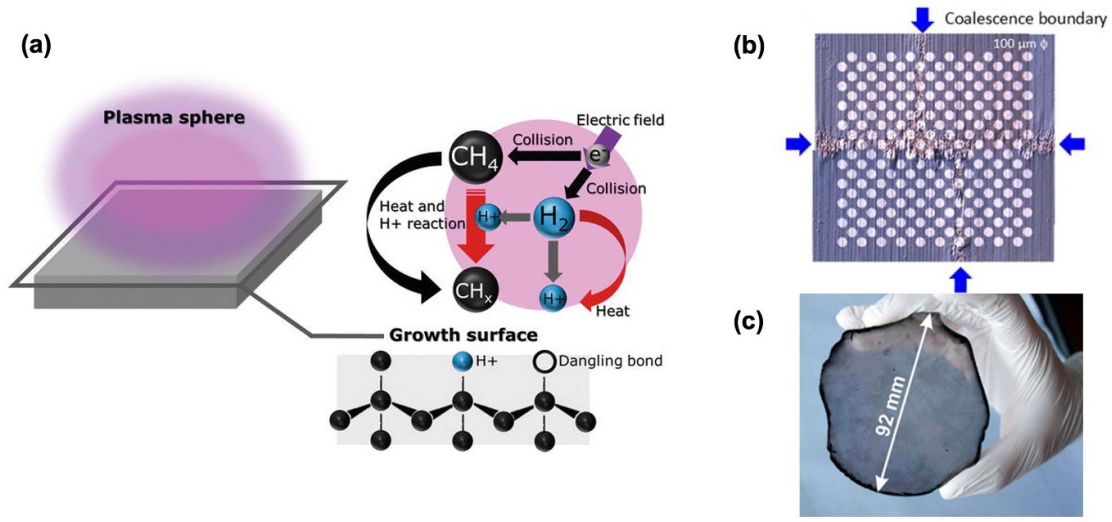

Figure 16. (a) General growth chemistry of MPCVD diamond growth using primarily CH_4 gas and H_2 plasma [263]; (b) Schottky barrier diodes fabricated on a mosaic diamond substrate [254]; (c) the largest diamond substrate to date grown by heteroepitaxial methods [266].

of copper, a common heat sink material. Isotopically enriched (using $^{13}CH_4$ or $^{12}CH_4$) diamond has shown thermal conductivities up to 3300 W $(m{\cdot}K)^{-1}$ [262].

4.2. Growth and doping

4.2.1. Single crystalline bulk substrate growth

While the superior properties of diamond make it an attractive candidate for future high power and frequency device platforms, manufacturing large-diameter, high-quality diamond substrate remains a challenge. The high-pressure high-temperature technique can be employed to synthesize low defect density diamond crystals; however, this method is inherently limited to <1 cm^2 diamond sizes. Alternatively, microwave plasma chemical vapor deposition (MPCVD) methods are prominently used to enlarge seed crystals by outward or lateral growth. Activated atomic hydrogen from the H_2 gas precursor reacts with the hydrogen-terminated surface of a diamond seed to provide a reaction site for carbon radicals to bond to. The CH_3^+ carbon radicals are supplied from CH_4 gas and generated using a plasma or high temperature environment in the chamber [263]. By this chemistry, monolayers of carbon are progressively deposited on the surface, as illustrated in figure 16(a). Unfortunately, this growth process is limited by the formation of PC diamond at the rim which can lead to further stress and cracking of the substrate [264]. Researchers have explored methods to suppress PC diamond formation, such as with modified pocket holders, different diamond seed geometries, and varying growth parameters. These efforts have produced substrates still on the order of 1 cm in diameter [265]. 2 inch substrates were realized by Yamada *et al* (figure 16(b)) by homoepitaxially growing diamond by CVD on a mosaic of smaller clone substrates grown from the same seed crystal, however high defect densities were present at the coalescence boundaries [252]. More recently, Ohmagari *et al* demonstrated the benefit of a W buffering layer in mitigating threading dislocations for mosaic diamond substrates [253] and showed very similar performance to Schottky diodes fabricated on and off the boundaries [254]. Finally, another method to achieve larger area diamond substrates is by heteroepitaxial growth of diamond on materials with readily available substrates. Schreck *et al* demonstrated heteroepitaxial diamond growth on an Ir/YSZ/Si (001) substrate producing a 1.6 mm thick diamond layer with a diameter of 92 mm as pictured in figure 16(c) [266]. The use of negative voltages during the bias-enhanced nucleation process and selection of Ir as the substrate, were key in enabling single-crystalline diamond formation. While the diamond substrates grown in this and other more novel methods have shown immense progress, the quality is certainly still lacking. Thus, continued progress in developing larger-scale diamond growth is critical for the practical widespread adaption of diamond as a semiconductor material.

4.2.2. Doping

In diamond, p-type doping using boron dopants can be readily achieved during bulk MPCVD diamond growth. For boron dopant concentrations up to 10^{18} cm^{-3}, boron has a relatively large activation energy of 0.37 eV, which decreases to ~0.06 eV when boron concentration exceeds 10^{20} cm^{-3} according to Pearson and Bardeen's model. Furthermore, at concentrations $>10^{19}$ cm^{-3}, hopping conduction, between ionized

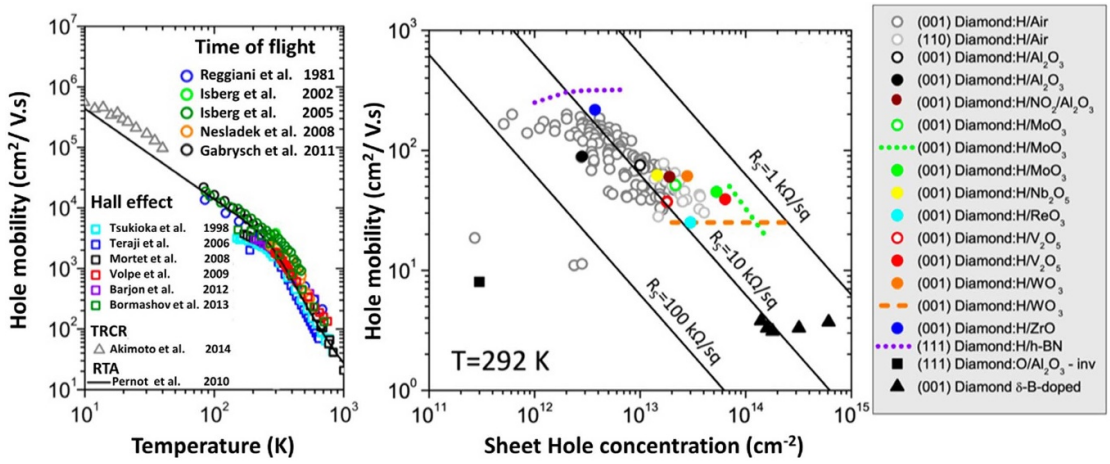

Figure 17. (a) Theoretical and experimental bulk hole mobility using various measurement methods; (b) 2DHG hole mobilities measured from various diamond orientations and passivation materials [280] (and references therein).

and neutral acceptors, dominates the conduction mechanism [267]. Thus, incomplete ionization and varying conduction mechanisms must be considered when designing devices.

On the other hand, n-type doping in diamond has been more difficult to achieve. Successful phosphorous doping with n-type conductivity was first measured in 1996 by Koizumi *et al* using phosphine as the dopant source during MPCVD growth [268]. Follow up growth optimizations yielded n-type diamond thin films grown on (111) Ib substrates with a maximum mobility of 240 cm^2 $(V{\cdot}s)^{-1}$ and an activation energy of ∼0.6 eV [269]. Due to the relatively high activation energy, phosphorous is not readily ionized at room temperature, with ionization levels of only 10^{-5}–10^{-6} [270]. To realize lower resistance n-type diamond, on the order of 70 Ω·cm, heavy phosphorous doping of diamond $>10^{20}$ cm^{-3} is required to lower the activation energy through hopping conduction [271]. On the other side of the spectrum, fine n-type doping control was shown with phosphorous concentrations $<3 \times 10^{17}$ cm^{-3}. The study reported n-type conductivity of the lowly doped films (2×10^{15} cm^{-3}) with high RT mobility of 1060 cm^2 $(V{\cdot}s)^{-1}$ [272].

While phosphorous is most readily incorporated into substitutional sites in (111) diamond, 2–3 orders higher than in (100), the high defect density formed during growth creates issues in device performance. More recently, the (113) orientation was also found to be a stable plane for phosphorous doped epilayer growth in addition to boron doped. In the study, the homoepitaxial layers reached up to 4.5×10^{19} cm^{-3} phosphorous content, greater than that of (100) and less than that of (111), proving to be a promising avenue for phosphorous doping in the future [273].

4.2.3. Surface transfer doping by hydrogen termination

While p-type boron doping is accessible in diamond, the high activation energy allows only a small fraction of dopants to ionize, making it difficult to engineer highly conducting channels in devices [274]. It was discovered that when hydrogen-terminated diamond, which has a negative electron affinity, is exposed to air containing atmospheric adsorbates, a two-dimensional hole gas (2DHG) forms near the surface. This p-type surface hole accumulation layer typically has a sheet charge density of 10^{12}–10^{13} cm^{-2} and hole mobility of 20–200 cm^2 $(V{\cdot}s)^{-1}$ [274]. In efforts to identify the key molecule responsible for forming the 2DHG, it was found that exposing the diamond to increasing levels of NO_2 led to an increased hole concentration, up to 2.3×10^{14} cm^{-2}, and conductivity [275]. At high temperatures above 300 °C, the 2DHG formed from just atmospheric adsorbates was discovered to be unstable, so researchers employed an Al_2O_3 passivation layer to stabilize the 2DHG at temperatures up to 500 °C [276]. Since then, other dielectric materials have been studied to passivate H-terminated diamond as well. More recently, transition metal oxides (TMO), particularly MoO_3 [277] and V_2O_5 [278, 279] have shown superior hole carrier concentrations on the order of 10^{14} cm^{-2}. With its high carrier density, the 2DHG has become a pathway for the most prominent diamond transistor, the H-terminated FET. However, an inverse relationship between hole sheet density and mobility has been repeatedly shown (figure 17), and thus a significant increase in conductivity may be limited. Charged surface acceptors and disorder related to the C–H surface dipoles have been proposed as mobility-limiting mechanisms [274], but more research is critical to determine whether the mobility limitations can be overcome to produce higher-performing devices.

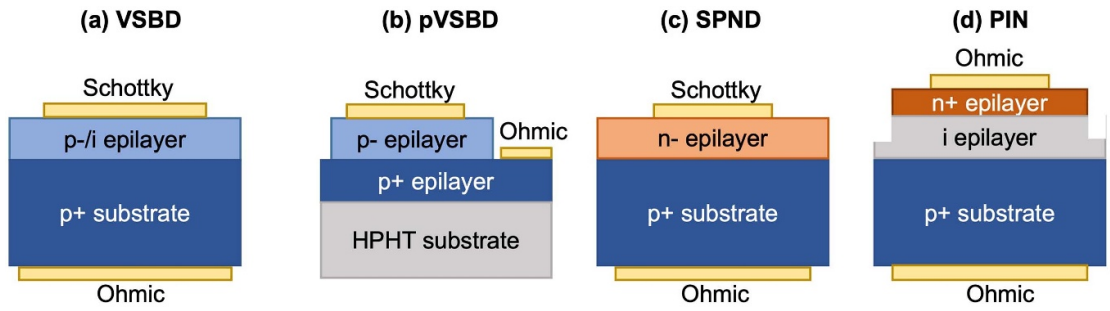

Figure 18. The cross-section schematic of vertical diode structures in diamond: the (a) vertical Schottky (VSBD); (b) pseudo-vertical Schottky (pVSBD); (c) Schottky PN; (d) PIN diode.

4.3. Diamond devices and applications

4.3.1. High power devices

4.3.1.1. Schottky and PN diodes

As diamond lacks a reliable n-type dopant, the p-type SBD is the most mature diamond diode device. Prior to the wider availability of low resistance diamond substrates, pseudo-vertical Schottky diodes were primarily fabricated on doped epilayers with an insulating substrate (figure 18(b)). With the development of highly boron doped substrates, true vertical Schottky diodes are now commonly reported as well (figure 18(a)). The Schottky barrier height can be varied in diamond diodes by utilizing different Schottky contact metals. It was shown that diodes with greater barrier heights can yield lower leakage [281], which comes with a cost of increased on-resistance. Diodes using Schottky contact metals of Al [281, 282], Ni [282, 283], Mo [281], Pt [281], Au [282, 284, 285], Ag [283], WC [286], Zr [287], etc have demonstrated Schottky barrier heights to diamond ranging from <1 to 3.4 eV. Various surface terminations techniques can vary the Schottky barrier height as well. In the case of a hydrogen-terminated diamond surface, the p-type conductivity at the surface must be removed to prevent a leakage path from forming. With oxygen-terminated surfaces, on the other hand, the metal contact becomes rectifying. Thus, increased oxygen termination at the surface was found to increase the Schottky barrier, reduce reverse leakage, and increase breakdown [284, 288, 289]. Diamond surfaces are commonly oxidized by boiling in strong acid mixtures and/or by ultraviolet (UV)/ozone treatment during Schottky diode fabrication [290]. The oxygen content on the diamond may be varied by the wet chemical acids, treatment time, and temperature as well as the ozone concentration and treatment time for UV/ozone [282].

Diamond Schottky diodes have primarily reported breakdown electric fields of <4 MV cm^{-1} even with field termination structures such as field plates. Select works have shown a breakdown field of 7.7 MV cm^{-1}, the record in diamond devices. Traoré *et al* reported results measured from pseudo-vertical Schottky diodes with oxidized Zr Schottky contacts that resulted in a record 244 MW cm^{-2} BFOM [287]. Volpe *et al* demonstrated the high breakdown voltage capability of diamond using Au Schottky contacts to a 13.6 μm p-epilayer (3×10^{16} cm^{-2} boron doped), and set a record breakdown voltage of 10 kV [285]. In recent works, pseudo-vertical Schottky diodes have also been demonstrated on (113) orientated surfaces, with similar performance to that of (100) [291]. The (113) orientation is of interest as it has shown less surface roughness than (111), thus providing better interface qualities while being relatively favorable for both boron and phosphorous doping.

In 2009, Makino *et al* demonstrated an alternative unipolar diode, the Schottky PN diode (SPND). In this configuration, the Schottky metal contacts a lightly phosphorous doped n-type layer on a p+ layer (figure 18(c)) [292]. As a result, the n-type layer is fully depleted in the forward and reverse modes, and the diode conducts like a p-type Schottky diode in the forward bias region, enabling fast switching speeds. In the reverse bias region, the maximum electric field is primarily blocked by the n-region (figure 19). This theoretically enables a more highly doped p-type region, thus increasing the forward current density while maintaining a sufficiently thick space charge region to block high voltages in the reverse region due to the n-type region. Using the SPND structure, a record low on-resistance of 0.03 mΩ·cm^2 was achieved with a breakdown field of 3.4 MV cm^{-1} and a breakdown voltage of 55 V yielding $\sim$100 MW cm^{-2} BFOM [293]. A >1 kV SPIND was later demonstrated by Dutta *et al* [294] and an ultrahigh forward current density on the order of 10^5 A cm^{-2} by Surdi *et al* [295], showing the overall potential of the SPIND for high power applications.

Furthermore, high temperature measurements in Schottky diodes have been measured up to 1000 °C and showed a rectification ratio of up to 10^4 at 600 °C [283, 288]. As the temperature increases, the forward

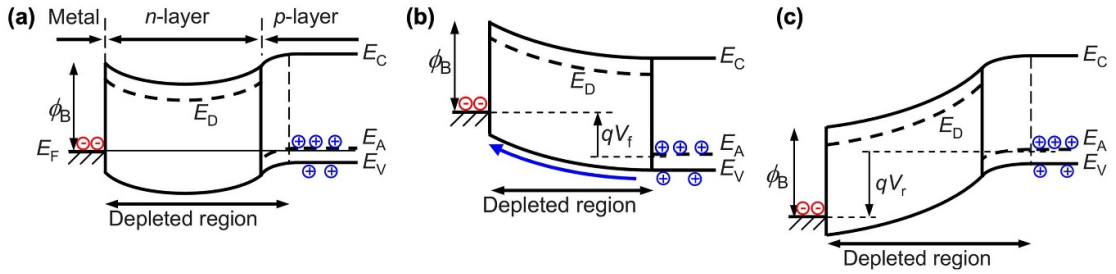

Figure 19. Proposed band diagrams of the SPND at (a) thermal equilibrium, (b) forward bias, and (c) reverse bias based on experimental results [292].

current density increases as the result of boron dopant ionization, which overtakes the decrease in mobility [283, 288, 296]. In high temperature measurements, it is also generally observed that an increase in Schottky barrier height and decrease in ideality factor occurs, indicating barrier inhomogeneity. This has been reported in other WBG materials as well [286], and further supported by conductive AFM measurements which showed that a very small fraction of the contact was active in the lower voltage range of the forward bias region [296].

Due to the challenge of n-type doping, PN diodes are relatively underdeveloped. Several studies have demonstrated PN diodes, with a focus on UV light emission indicating bipolar transport; however, the electronic performance is lacking. Due to the high resistivity of n-type diamond, the on-state current density remains limited, with 140 A cm^{-2} as the highest reported, while a reverse blocking voltage up to 920 V [297] and breakdown field of 3.9 MV cm^{-1} [294] have been achieved.

The current breakdown field values are still far from theoretical predictions in diamond, so efforts to reduce reverse leakage current and premature breakdown are highly relevant. The reverse bias leakage current in Schottky diamond diodes has been fit to the thermionic emission model with image-force lowering at lower fields, and the thermionic field emission model at fields >1 MV cm^{-1} [286, 298]. While this observation has been common in other wide-bandgap semiconductors as well, another prominent source of leakage is the presence of defects formed during growth, which can affect any type of device. These include non-epitaxial crystallites, which have been characterized as killer defects [298], and crystallographic defects like threading dislocations. In a study of PIN diodes, the reverse bias current characteristics, analyzed up to 150 °C, were attributed to hopping conduction and Poole–Frenkel emission through threading dislocations [299]. Furthermore, it was found that as the drift layer increases in thickness, the breakdown field does not proportionally increase in most cases, which indicates poorer epitaxial quality with thicker drift layer growth [300]. While the reduction of defects requires improvement in growth techniques, a common cause for reverse breakdown and increased leakage is field enhancement at the edge of the electrode, a common issue in other materials as well. In response, field-plated Schottky diodes with sputtered Al_2O_3 were studied and found to increase the breakdown voltage appreciably by more than 2 times, from 0.6–0.8 to 1.6–2.0 MV cm^{-1} [301, 302]. While the impact of the field plate has been experimentally shown, more recent studies have not reported similarly effective field plates. Other edge termination structures such as ramped field plates, junction termination, etc have yet to be successfully demonstrated in diamond due to fabrication limitations such as selective doping. Thus, in diamond two-terminal devices, there is still significant room for optimization, improved performance, and reliability studies, which should naturally follow the development of improved growth and doping techniques.

4.3.1.2. MESFETs and MOSFETs

In oxygen terminated diamond, FETs can be fabricated which rely on bulk conduction in the channel as illustrated in figures 20(a)–(c). Due to the large Schottky barrier heights achievable in diamond on oxygen-terminated diamond, MESFETs have been studied with relatively low gate leakage. Umezawa *et al* demonstrated diamond Pt-gated MESFETs with increasing breakdown voltages from 693 V to 1530 V as gate-to-drain distance was increased from 5 to 30 μm [303]. The less-than-ideal breakdown field, approximately 2.15 MV cm^{-1}, can be attributed to electric field spiking at the drain-side edge of the gate electrode. Another FET structure that has been demonstrated is the deep depletion mode MOSFET by Pham *et al* [304, 305]. The structure utilizes an Al_2O_3 dielectric and has achieved a high hole mobility in the conducting channel of 1000 $\pm$ 200 cm^2 $(V{\cdot}s)^{-1}$. This structure has the potential to take advantage of bulk hole mobility while limiting gate leakage which is typically higher in MESFETs.

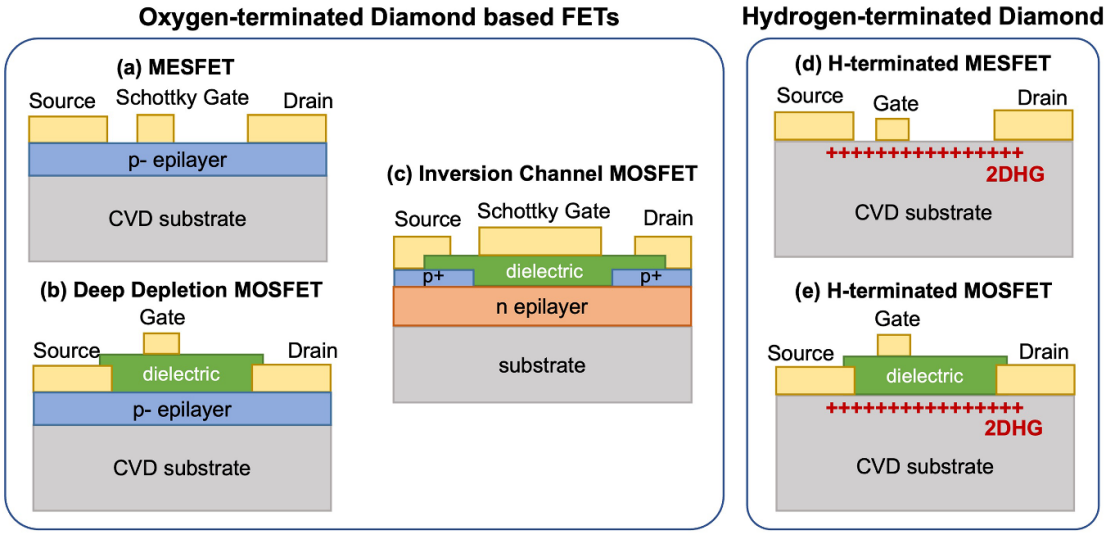

Figure 20. The cross-section schematic of FET structures in diamond categorized into oxygen-terminated diamond FETs and hydrogen-terminated diamond FETs.

While more difficult to achieve due to the challenge of n-type doping and the WBG of diamond, classic inversion channel MOSFETs have been shown due to improvements made in phosphorous doping. Such devices have advantages in gate controllability and threshold voltage tunability [306]. In 2016, Matsumoto *et al* reported the first inversion p-channel diamond MOSFET with normally-off characteristics utilizing a phosphorous-doped n-type body grown on a (111) substrate. A high-quality interface by wet annealing was formed between the Al_2O_3 gate oxide and O-terminated n-type diamond. The devices with a gate length of 5 μm delivered a maximum drain current density of 1.6 mA mm^{-1}, an on/off ratio $>10^{10}$, and a field-effect mobility of 8.0 cm^2 (V·s)$^{-1}$. The low mobility was attributed to high interface defect density, which can be reduced by achieving flatter surfaces [306]. Further studies showed that decreased phosphorous doping density (2×10^{15} cm^{-3}) resulted in greater smoothness and lower interface defect density, and as a result, higher mobility, up to 20 cm^2 (V·s)$^{-1}$ and higher drain current density [307]. Thus, the interface state density between the n-type diamond and the oxide must be further studied and reduced to improve the performance of inversion channel MOSFETs. More recently they also demonstrated an inversion p-channel MOSFET on nitrogen doped diamond, which is much easier to dope albeit has a much larger activation energy, 1.7 eV. Nonetheless, the MOSFET exhibited a drain current density very similar to that of MOSFETs fabricated using a phosphorus n-type diamond body [308].

Hydrogen-terminated (H-term) FETs are the most studied diamond transistor, in which the surface 2DHG formed by hydrogen termination of single-crystalline (SC) or PC diamond generates a conductive channel with a high density of hole carriers (figures 20(d) and (e)). In an H-term MESFET, a Schottky contact, commonly Al, is directly deposited on the diamond as the gate metal. In a MOSFET, Al_2O_3 is often used as the gate oxide since it preserves the 2DHG and stabilizes it for high temperature operation. A NO_2-enhanced H-term MOSFET showed the highest reported breakdown voltage to date, 2.6 kV at a field of 2 MV cm^{-1} [309]. The highest drain current density is reported to be 1.35 A mm^{-1} using NO_2 exposure to increase hole density and Al_2O_3 passivation [310].

Because the 2DHG consists of surface charges formed by hydrogen termination, it is very sensitive to the surface and interface quality. H-term FETs may be depletion or enhancement mode devices based on the surface treatment of diamond and interface defects. To form enhancement mode devices, several strategies have been employed such as selecting low work function gate material [311], partially oxidizing the H-diamond surface [312, 313], and choosing gate oxides with different deposition methods [314–316]. The highest current density for enhancement mode devices, 400 mA mm^{-1}, was recently reported by Zhu *et al* using PC diamond MOSFETs with a heavily boron-doped layer as the source/drain region [315].

While Al_2O_3 is the most popular dielectric used, many others have been studied as well such as HfO_2 and h-BN [314]. Exfoliated single crystalline h-BN is known to have a very flat surface with few charged impurities and no dangling bonds. Thus, it has the potential to form a high-quality interface with diamond. Recently, Sasama *et al* used a h-BN gate insulator which resulted in a >300 cm^2 (V·s)$^{-1}$ channel mobility device [317]. The high mobility was attributed to the low density of defects in h-BN, and follow-up studies

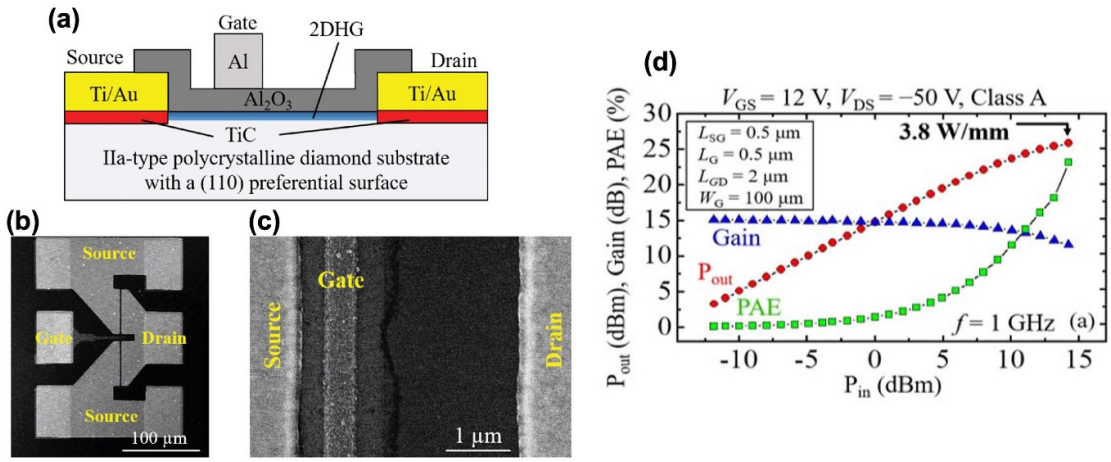

Figure 21. (a)–(c) The schematic and microscope images of an RF diamond H-term MOSFET; (d) large-signal performance of (a) at $V_{DS} = -50$ V [324].

were able to further enhance the mobility to 680 cm^2 $(V{\cdot}s)^{-1}$ by eliminating air exposure between the hydrogen termination and h-BN lamination steps during fabrication [318].

4.3.2. RF hydrogen terminated FETs

Around 2001, researchers first began to report on the high-frequency performance of H-term FETs; however, high-frequency devices in diamond are still very much in the early stages of development. A series of studies from Kasu *et al* culminated in a device (gate length = 0.1 μm, width = 100 μm) yielding 2.1 W mm^{-1} output power density [319]. This relatively high value in diamond was attributed to the high-purity gas used during homoepitaxial layer growth. Later, the group demonstrated a MESFET (gate length = 0.4 μm, width = 1 mm) with a record 23.2 dB maximum power gain and 56.3% PAE [320] measured at 1 GHz and drain-to-source voltage (V_{DS}) = −20 V. Published in the mid-2000s, these RF measurement values remain difficult to surpass. While SC diamond is typically preferred for more ideal electronic properties, PC diamond is much more accessible, offering lower costs and larger diameters, and is also actively studied for fabricating H-term FETs. MESFETs fabricated on preferentially (110) oriented PC diamond by Ueda *et al* demonstrated a high f_T of 45 GHz and f_{max} of 120 GHz and leakage was not observed in the large grain (100 μm) PC diamond substrate [321].

In 2007, Hirama *et al* measured the RF characteristics of H-term MOSFETs on SC and PC diamond using an alumina gate insulator for the first time [322]. The gate oxide was formed by the oxidation of 3 nm thick Al. The (001) homoepitaxial devices demonstrated a similar output power density to that of Kasu *et al*, with 2.14 W mm^{-1} at 1 GHz. Furthermore, the PC (110) devices yielded higher current density and 1.5 times the f_T than the SC (001) devices. This was attributed to the differing orientations rather than the PC and SC nature of the substrates. Previous reports have shown that H-terminated (110) diamond resulted in higher C–H bond density and thus higher hole densities in the 2DHG.

In recent studies, Yu *et al* reported the highest f_T/f_{max} in diamond MOSFETs of 70/80 GHz, which was attributed to continued scaling of the source-drain distance and thin 6 nm gate oxide [323]. Then in 2019, Imanishi *et al* demonstrated the highest power density at 1 GHz to date, 3.8 W mm^{-1} in a MOSFET diamond device with 100 nm ALD Al_2O_3 on a (110) preferential PC diamond substrate (figure 21) [324]. In 2022, the highest RF power densities were measured at 2, 4, and 10 GHz to date: 4.2, 3.1, and 1.7 W mm^{-1}, respectively, on homoepitaxial (001) single crystalline diamond substrates with 100 nm Al_2O_3 [325]. In both these studies, V_{DS} was pushed to greater than 40 V, which contributed to the record power densities measured in diamond.

4.3.3. Heterogeneous integration of diamond for device-level thermal management

The efficiency and reliability of power and RF devices are not only limited by the electronic properties of the material but also by their thermal management [326], as mentioned in section 2.3.2.1. At the device level, Joule heating occurs in the channel due to increased power density and switching speeds. As a result, device performance can suffer from high temperatures which can eventually result in premature failure. While developing diamond-based devices can be a solution due to diamond's excellent thermal and electronic properties, enormous research efforts and progress are still needed to achieve high-performance devices. On the other hand, heterogeneous integration of diamond can serve as a heat spreader solution for more mature

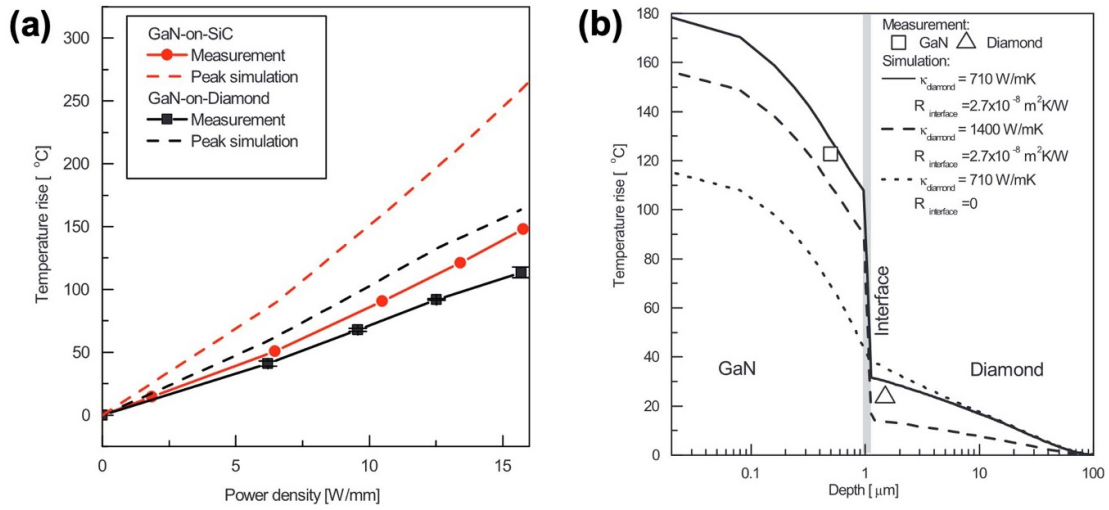

Figure 22. (a) The temperature rise 0.5 μm from the T-gate edge for GaN-on-SiC and GaN-on-Diamond HEMTs measured using Raman thermography and shown to increase with increasing power density; (b) the temperature across GaN, the interface, and diamond were simulated and showed that minimizing the thermal resistance at the interface can more significantly reduce the temperature in GaN than simply increasing the thermal conductivity of diamond [329].

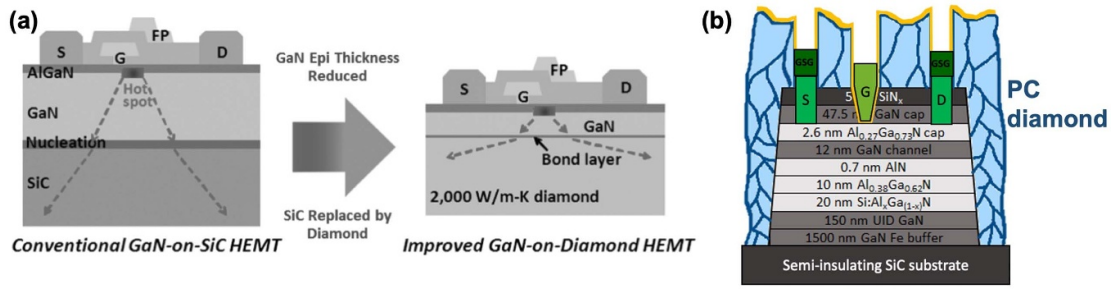

Figure 23. (a) Backside approach for diamond integration to GaN. The SiC and nucleation layer are removed, and the GaN epilayer is thinned before bonding to diamond [330]; (b) topside/all-around PC diamond integration by MPCVD diamond growth above the substrate [331].

material technologies like GaN as well as other emerging UWBG materials such as Ga_2O_3 and AlGaN which have inferior thermal properties [327, 328]. GaN technology, more specifically AlGaN/GaN HEMTs at its current stage, has already penetrated the high-frequency, high-power device market for power amplifiers. Thus, there is particularly high interest in device-level cooling for these structures to enhance their power output. Due to silicon carbide's relatively high TC, GaN-on-SiC technology is customarily used for power RF devices. As diamond possesses a significantly higher TC, Pomeroy *et al* demonstrated that GaN-on-diamond could yield a 40% decrease in peak channel temperature in comparison to GaN-on-SiC AlGaN/GaN HEMTs based on a combination of Raman thermography measurements and thermal modeling (figure 22) [329]. To implement such a diamond-based thermal management strategy, there are two primary approaches as illustrated in figure 23: backside diamond substrate bonding and PC CVD heteroepitaxial diamond growth.

Several works have shown the feasibility of GaN to diamond bonding at lower annealing temperatures of 150 °C–180 °C using 15–40 nm thick undisclosed/Si-based adhesion interlayers [330, 332]. However, the thermal boundary resistance (TBR) of the GaN/diamond interface including the adhesion layer can become a dominating source of thermal resistance as displayed in figure 22(b) [329]. To take full advantage of a diamond heat spreader, a low diamond to substrate TBR is required in addition to a high diamond TC. More recently, the process of surface-activated bonding (SAB) at room temperature under high vacuum was developed (figure 24) [333]. Using this technique resulted in a relatively low GaN/diamond interface TBR of $\sim$11 $m^2K\ (GW)^{-1}$ with a 4 nm bonding sputtered Si bonding layer [334]. While this method requires a specialized tool, a more recent study has established a low temperature, easy-access method in which no pre-deposited interlayer is needed [335]. In this process, a GaN substrate first underwent HCl chemical treatment and the diamond NH_4OH/H_2O_2 treatment. Then, a 2 h, 200 °C, 1 MPa bonding was sufficient to

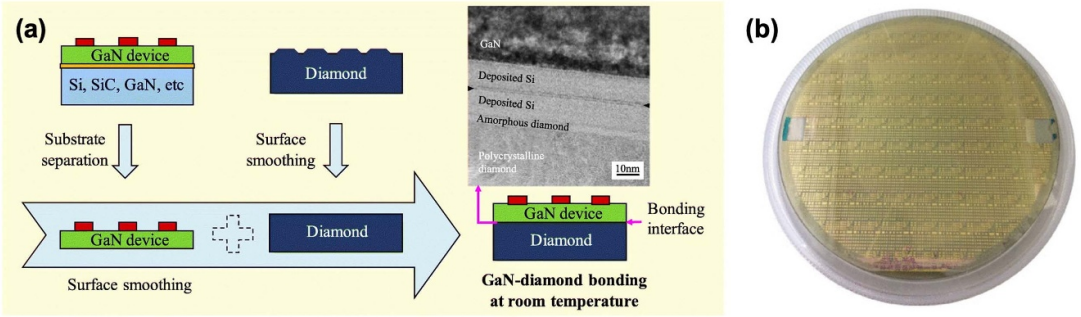

Figure 24. (a) A room temperature surface-activated bonding process assisted by Si nanolayers for GaN/diamond yielding an interface free of nanovoids as shown by TEM imaging [333]; (b) a 3 inch GaN-on-diamond wafer with fabricated HEMTs using low temperature bonding [332].

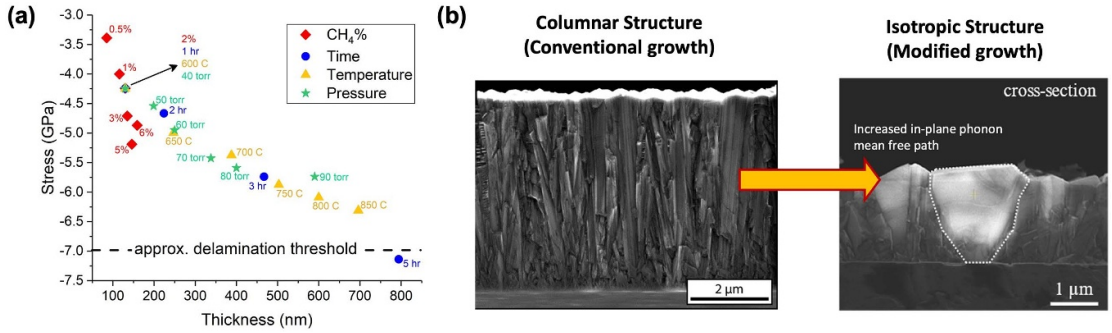

Figure 25. (a) Residual stress as a function of PC diamond film thickness; (b) cross-section schematics and SEM micrographs showing the transformation of diamond grains from a columnar structure to more isotropic [337].

bond the two materials. TEM images showed the formation of a 3 nm amorphous layer, which was predicted to produce a low TBR due to its thinness, although it has not been measured.

In addition to studying diamond thermal management from a material perspective, diamond heat spreading technology must also demonstrate integration without degradation of the device, show an operational temperature decrease, and ultimately enhance device performance and reliability. Using low temperature bonding methods to PC diamond substrates, several groups have shown device-first transfer technology of GaN HEMTs. Chao *et al* maintained a high-performance HEMT with a maximum output power density of 11.0 W mm^{-1} at 10 GHz and a PAE of 51% following the transfer to diamond [330]. Furthermore, IR imaging showed three times higher dissipated power in the same active area of a GaN-on-diamond HEMT in comparison to that of GaN-on-SiC. Liu *et al* later successfully demonstrated 3 inch GaN-on-diamond HEMTs with >80% yield and measured a 50 °C decrease in peak channel temperature (from 241 °C to 191 °C) at 10 W mm^{-1} [332]. With these promising device-level results, similar studies must continue as advancements in the thermal properties of diamond heat spreader technology are made.

Alternatively, a topside PC diamond heat spreader can be advantageous since the diamond can be integrated closer to the channel and more effectively transfer heat away from the channel hot spot. Furthermore, it has increased potential for scalability since it is not limited by the diamond substrate size. To implement this approach, heterogeneous epitaxial growth of diamond must be well-understood. First, to nucleate diamond grains on foreign substrates, a seeding process using diamond nanoparticles is performed. After, the seeded substrate is placed in a hot filament or MPCVD chamber for growth at 400 °C–1000 °C, relying on the same chemistry as that of substrate growth described in section 4.2.1. An important parameter when growing diamond on a foreign substrate is the residual stress due to a coefficient of thermal expansion (CTE) mismatch between the two materials [336]. Since diamond has a very low CTE of $\sim 1.1 \times 10^{-6}$ $K^{-1,}$ it typically contracts less than the substrate while cooling down from growth temperatures, causing compressive stress to form in diamond. The magnitude of stress increases with growth thickness (figure 25(a)), eventually causing the diamond to delaminate from the substrate [337]. This limits the thickness of PC diamond that can be grown on foreign substrates.

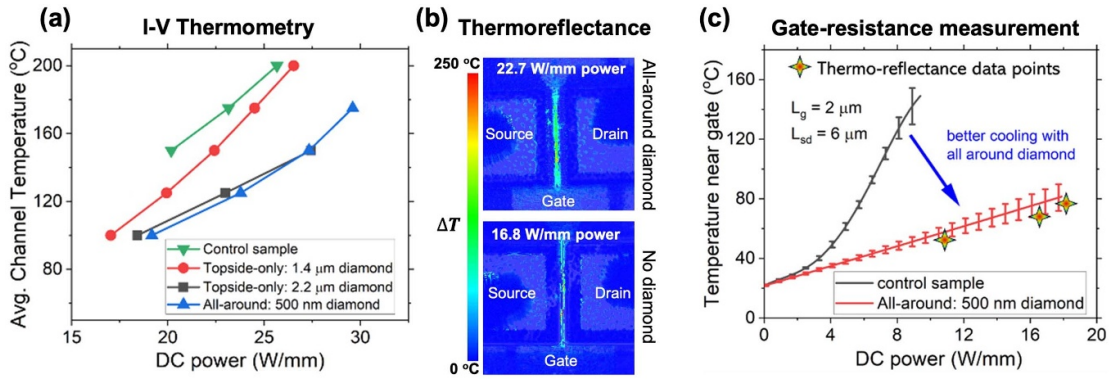

Figure 26. Lower temperature in the channel was measured for all-around diamond devices using multiple methods: (a) I–V thermometry, (b) thermoreflectance imaging, and (c) gate-resistance measurement [331].

Depending on the growth parameters (e.g. gas pressure, plasma power, surface temperature, CH_4%, etc), seeds may grow in the vertical and lateral directions at different rates. Figure 25(b) shows how the change in the growth parameters can transform the columnar structure into a more-isotropic structure [338]. Because one primary drawback of heteroepitaxial PC diamond growth on GaN is the reduced TC in comparison to SC diamond, the formation of large, isotropic diamond grains is crucial. Developing more isotropic growth enhances in-plane phonon transport by reducing scattering sites at the grain boundaries, thus increasing the effective TC and overall capability for device cooling. For example, the more isotropic diamond grains grown by Malakoutian *et al* compared to others resulted in a relatively higher TC of ∼648 W m^{-1} K^{-1} for a 2 μm thick epilayer [338]. Furthermore, there are tremendous efforts in reducing heteroepitaxial diamond-on-GaN TBR for the same reasons highlighted earlier in this section. Zhou *et al* and Yates *et al* showed that using a SiN_x interlayer between diamond and GaN produced an average TBR of 6.5–9.5 m^2K $(GW)^{-1}$, while using an AlN interlayer averaged 15.9–18.2 m^2K $(GW)^{-1}$ [339, 340]. In another work, Malakoutian *et al*, reported the lowest measured TBR between diamond and GaN ∼3.1 m^2K $(GW)^{-1}$ by using a 1 nm SiN_x interlayer [338], indicating that the heat transfer will not be hindered significantly at the interface.

Because typical diamond growth takes place under high temperatures (HT), between 600 °C and 1000 °C, diamond integration with many semiconductor technologies will inevitably damage the device or substrate material. As a result, there have been many efforts to reduce the growth temperature for compatibility with low thermal budget materials and processes. Low temperature (LT) diamond growth has been reported in a temperature range from 100 °C to 500 °C. The growth of a high-quality PC diamond at back end of line compatible temperature, 400 °C, was achieved by modifying the gas chemistry at different nucleation stages. A sharp sp^3 Raman peak (full width at half maximum ≈ 6.5 cm^{-1}) and high phase purity (97.1%), like that of HT-diamond (>98%) were measured in the near-isotropic PC diamond [341]. Furthermore, the LT diamond exhibited a relatively high in-plane and cross-plane TC of ∼300 W $(m{\cdot}K)^{-1}$, and a TBR as small as 5 m^2K $(GW)^{-1}$. The results of these studies highlight the feasibility of diamond integration with various semiconductor technologies and open a path for heat spreading solutions for practical adoption.

By using the LT diamond growth technique, Soman *et al* demonstrated the cooling effect of an integrated all-around PC diamond structure on the topside of a GaN HEMT. The thermal resistance between the device's active region and heat sink was reduced using PC diamond integration, ultimately resulting in a channel temperature decrease of >70 °C at 25 W mm^{-1} power operation shown using I–V thermometry [331]. The thermal benefits were further confirmed using thermoreflectance and gate-resistance measurement techniques illustrated in figure 26. As the inefficiency due to heating is a universal problem in electronics, particularly in high-frequency and high-power switching, continued research in diamond integration for thermal mitigation has the potential to highly impact the field.

Among the emerging UWBG semiconductors, β-Ga_2O_3, discussed later in section 5, has already demonstrated great potential for power device technologies while offering a low-cost method for large-diameter wafer growth. Nonetheless, a notable drawback of this material is its markedly low, anisotropic TC ranging from 11 to 27 W m^{-1} K^{-1}. As a result, there is particularly high interest in employing diamond as a heat spreader for Ga_2O_3. A few key studies have been published that parallel the integration approaches undertaken in GaN. Low-temperature bonding of Ga_2O_3 and diamond was achieved by Matsumae *et al* by first OH terminating both diamond and Ga_2O_3 using H_2SO_4/H_2O_2 and oxygen plasma irradiation, respectively. The contacted materials were then annealed at 250 °C for hydrophilic bonding to

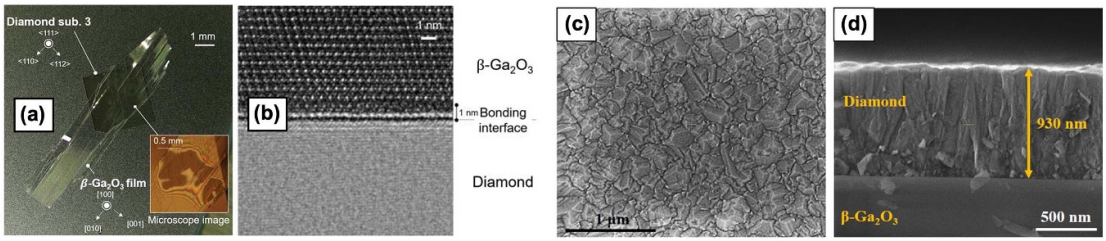

Figure 27. (a), (b) Exfoliated 10 μm β-Ga_2O_3 bonded to diamond and the TEM image of its interface [342]; (c), (d) MPCVD-grown diamond on a 100 nm SiO_2 interlayer on β-Ga_2O_3, yielding an average grain size of 400 nm [327].

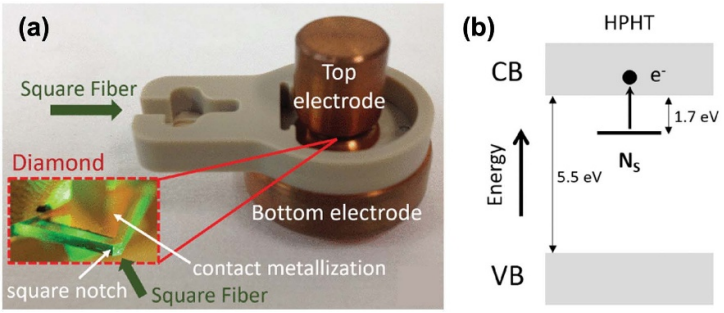

Figure 28. (a) A vertical extrinsic diamond PCSS excited by 532 nm light; (b) the band diagram representation of the mechanism by which electrons are excited from the nitrogen deep donor level in diamond to the conduction band in response to 532 nm light [349].

take place (figures 27(a) and (b)) [342]. Additionally, PC diamond heteroepitaxial growth on β-Ga_2O_3 substrates was shown using a relatively thick SiO_2 protective interlayer that prevented substrate damage and enabled uniform diamond nucleation [327, 343]. As illustrated in figures 27(c) and (d), at lower magnifications, the diamond-on-Ga_2O_3 film exhibits remarkable uniformity, and at high magnification SEMs, dense PC diamond was observed [327]. These results mark a significant step towards device-level thermal management for β-Ga_2O_3.

4.3.4. Photoconductive semiconductor switching

Photoconductive semiconductor switches (PCSS) are optically controlled electronic devices that are desired for their high voltage, high speed, and jitter-free operation [344]. This is achieved by modulating the conductivity of a semiconductor substrate with a light energy source. These devices are especially effective in pulsed power technology, such as radar, particle acceleration, and pulsed high-power lasers. Furthermore, as there are increased efforts toward electrification, developing safer mechanisms for making and breaking high power circuits is a priority. By decoupling the trigger from the circuit with an optical source, the chances of false triggering are reduced and more simple and resilient circuits can be enabled [345]. One of the main issues of photoconductive switches is their short lifespan resulting from voltage and current overloads as well as thermal runaway effects at high-power levels [344]. The use of diamond and other UWBG semiconductors to fabricate PCSS devices could mitigate some of these issues owing to their superior material properties.

Past studies have shown photoconductivity in intrinsic diamond by UV-band excimers in high electric fields up to 0.7 MV cm^{-1}, >10 kV conditions, and with picosecond to nanosecond response times [346–348]. In contrast to intrinsic PCSSs, which depend on high photon energies above the bandgap (band-to-band excitation), extrinsic PCSS operates with below bandgap photon energies due to the excitation of carriers from dopants and defect levels as illustrated in figure 28(b). This enables PCSS functionality with more accessible sub-bandgap excitation sources in the visible or infrared range while maintaining the desirable properties of diamond. Nitrogen-doped diamond-based PCSSs have shown nanosecond pulsed responses to 532 nm light by exciting an electron from the deep defect level (1.7–2.0 eV) of nitrogen into the conduction band [345, 349]. Since diamond's nitrogen dopants are largely inactivated at room temperature, making ohmic contacts is challenging for PCSS devices. However, Woo *et al* showed that the contact resistivity is reduced when the electrodes are under illumination which enabled a high I_{on}/I_{off} ratio ($>10^{11}$ at 33 kV cm^{-1} in response to 0.8 mJ, 10 ns pulsed, 532 nm light). The responsivity of nitrogen-doped diamond to 532 nm light was found to be less than that of diamond UV light, but

comparable to the responsivity of SiC and GaN extrinsic PCSSs [349]. On the other hand, boron doped diamond was found to be responsive to both 532 and 1064 nm light due to its lower activation energy (0.37 eV). While its large off-state conductivity renders it a poor candidate as a switch on its own [345], photoexcitation of boron dopants may still lend itself to other optically triggered electronic devices. Further studies to increase the quantum efficiency of the PCSS and explore the use of other defect states will greatly contribute to the practicality of light-triggered devices in diamond.

5. Beta-gallium oxide (β-Ga_2O_3)

5.1. Material properties

Five types of Ga_2O_3 polymorphs were reported in 1952, denoted as α, β, γ, δ, and ε, respectively. However, recent high-resolution structural characterizations revealed that a transient κ-phase polymorph could form an ordered subgroup in the ε-phase, and an ε/κ phase could coexist instead of a pure-phase Ga_2O_3 polymorph [350, 351]. Among all the five polymorphs, β-Ga_2O_3 is the only thermodynamically stable phase and therefore, the most extensively studied. In this review, the discussions will only focus on the material properties and device applications of β-Ga_2O_3.

The most attractive merit of β-Ga_2O_3 is its high critical field due to its large bandgap of 4.9 eV. Based on the empirical relationship between the critical field and the material's bandgap, a critical field as high as 8 MV cm^{-1} was predicted for β-Ga_2O_3 theoretically [3, 352]. However, almost all the experimental results demonstrated a premature destructive breakdown for β-Ga_2O_3 devices due to the field crowding at the edge of the gate dielectric or the anode electrode. The highest average critical field reported was around 6 MV cm^{-1} in vertical SBDs [353, 354], and no avalanche was reliably observed in a β-Ga_2O_3 device.

The electron mobility at room temperature for the doping range of 10^{15}–10^{16} cm^{-3} is reported to be around 150–200 cm^2 $(V{\cdot}s)^{-1}$ [355–357], and is mainly limited by the longitudinal optical phonons in the β-Ga_2O_3 [358]. The saturation velocity of electrons in β-Ga_2O_3 was calculated to be around $1–2 \times 10^7$ cm s^{-1} [359], which is sufficient for many high-frequency applications. Unfortunately, due to the flat valence band maximum in β-Ga_2O_3, leading to a heavy hole effective mass, the mobility of holes is expected to be very low and nearly no measured values have been reported.

Another one of the main drawbacks of β-Ga_2O_3 is its low TC, posing another challenge for its high-power applications. The extracted TC of β-Ga_2O_3 is 0.27 W $(m{\cdot}K)^{-1}$ along the [010] direction and 0.11 W $(m{\cdot}K)^{-1}$ along the [99] direction [360]. Since these values are only 1/10 of the values for SiC and GaN, more efficient thermal management for Ga_2O_3 devices is demanded.

5.2. Growth and doping

5.2.1. Bulk substrate growth

One of the distinctive features of β-Ga_2O_3 among U/WBG materials is that its native substrates can be grown via the melt growth method. Consequently, mass production of β-Ga_2O_3 substrates with large wafer sizes, high structural quality, and low manufacturing costs is more feasible. The β-Ga_2O_3 substrates can be grown from various melt growth methods: float zone [361–363], Czochralski [364, 365], vertical Bridgman, and edge-defined film-fed growth (EFG) [366], pictured in figure 29. Among these methods, the EFG growth method shows great potential in offering large-diameter β-Ga_2O_3 substrates. 4 inch single-crystalline β-Ga_2O_3 substrates have been successfully grown via the EFG method with a low dislocation density of 10^3–10^4 cm^{-2} and a surface roughness of 0.1 nm [367]. To date, 2 inch β-Ga_2O_3 substrates are commercially available to the public.

5.2.2. Epitaxial layer growth

Like other compound materials in this review, several familiar techniques: MBE, HVPE, and MOCVD are often used for the epitaxial growth of Ga_2O_3. MBE, which can offer high-purity growth with precise control of thickness, has been the most commonly used technique for thin film Ga_2O_3 growth at the beginning of its research and development [370–372]. The growth typically occurs by oxidizing the supplied Ga atoms using ozone or oxygen radicals [373, 374]. Intentional dopants, such as Si, Sn, and Ge can be incorporated during MBE growth. However, it is difficult to achieve a doping density on the order of 10^{16} cm^{-3} or less due to the oxidization of the dopant source by background O species during the growth [375].

HVPE growth of Ga_2O_3 was demonstrated in 2014 by using GaCl and O_2 as precursors [376]. Like HVPE growth of GaN, the GaCl is formed by the reaction of gallium metal source and Cl_2 gas at 850 °C in a source zone first and then transported to the growth zone and reacted with O_2. Here, $SiCl_4$ is commonly used as an n-type dopant source. The growth rate of HVPE can reach up to 20 μm per hour without degrading the film

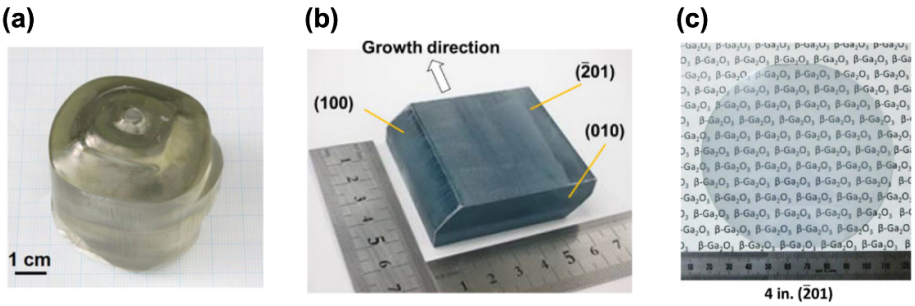

Figure 29. Bulk β-Ga_2O_3 crystals grown by (a) the Czochralski method [368] and (b) the edge-defined film-fed growth (EFG) [369]; (c) a 4 inch β-Ga_2O_3 substrate with a surface orientation of [2¯01] grown by EFG method [369].

quality. A low unintentional doping of 10^{13} cm^{-3} has been achieved by HVPE growth and intentional doping density in the range of 10^{15}–10^{19} cm^{-3} can be accurately controlled by adjusting the flow of $SiCl_4$ [377].

MOCVD is well established in several other compound semiconductors, as mentioned earlier, and can mass produce high-quality epitaxial films. Gallium precursors, such as trimethylgallium (TMGa) and triethylgallium (TEGa), and high-purity O_2 are typically used for MOCVD growth of Ga_2O_3. At the beginning of development, MOCVD growth of Ga_2O_3 faced challenges of low growth rates, high background carrier concentrations, and low electron mobilities [375]. Thanks to the tremendous efforts in optimizing the growth conditions, the structural and electrical properties of Ga_2O_3 film grown by MOCVD have been significantly improved over the recent years [378–382]. Another unique advantage of MOCVD growth is its ability to produce a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure [375, 383, 384], which constitutes an important architecture in Ga_2O_3-based RF applications.

While the aforementioned growth methods are currently the leading techniques and attract significant research interest in Ga_2O_3 epitaxy, additional growth methods, including low pressure chemical vapor deposition (LPCVD) [385–388], mist chemical vapor deposition (Mist-CVD) [389–391], liquid injection metalorganic chemical vapor deposition (LI-MOCVD) [351, 392], and pulsed laser deposition (PLD) [393, 394], have offered epitaxial Ga_2O_3 films of comparable film qualities with the benefits of relatively low deposition temperatures, large carrier concentration ranges, high deposition rates and relatively inexpensive deposition equipment. Lastly, heteroepitaxy of Ga_2O_3 device structures on more thermally conductive foreign substrates for heat mitigation employs epitaxial growth methods described in this section. However, more specific works are further described in section 5.3.3.

5.2.3. Doping

Silicon (Si), Tin (Sn), and Germanium (Ge) are commonly used as donors in β-Ga_2O_3 [395]. At room temperature, the donors show a high activation ratio due to the shallow donor states, typically around 30 meV below the conduction band [396–400]. These dopants can be incorporated into the β-Ga_2O_3 through *in-situ* growth, ion implantation, or diffusion method. The conductivity of the n-type β-Ga_2O_3 can be well modulated by controlling the donor concentration, within the range of 10^{15}–10^{20} cm^{-3}.

In contrast to the ease and success in achieving n-type doping in β-Ga_2O_3, p-type doping in β-Ga_2O_3 has evaded researchers and has become a primary limitation in the rapid development of various β-Ga_2O_3 devices [3, 375]. Several elements, including Mg, and N, were reported to serve as deep acceptors in β-Ga_2O_3, though with an activation energy larger than 1 eV [401, 402]. Besides, the first principle calculations predict a very flat valence band, leading to a large hole effective mass and low mobility [403, 404]. Moreover, self-trapping of holes limits the free hole conduction in β-Ga_2O_3 due to the local lattice distortion [405–407]. The combination of these factors contributes to the difficult nature of achieving well-behaved hole conduction. Recently, Chikoidze *et al*, reported that undoped β-Ga_2O_3 after an oxygen anneal exhibited p-type nature above 500 °C. A free hole concentration of around 10^{17} cm^{-3} (mobility $\sim$0.4 cm^2 $(V{\cdot}s)^{-1}$) was measured and attributed to the large formation energy of the oxygen donor vacancies [408, 409]. These findings help the community understand the mechanism behind the carrier formation and potentially shed light on achieving better p-type conductivity suitable for practical use in Ga_2O_3.

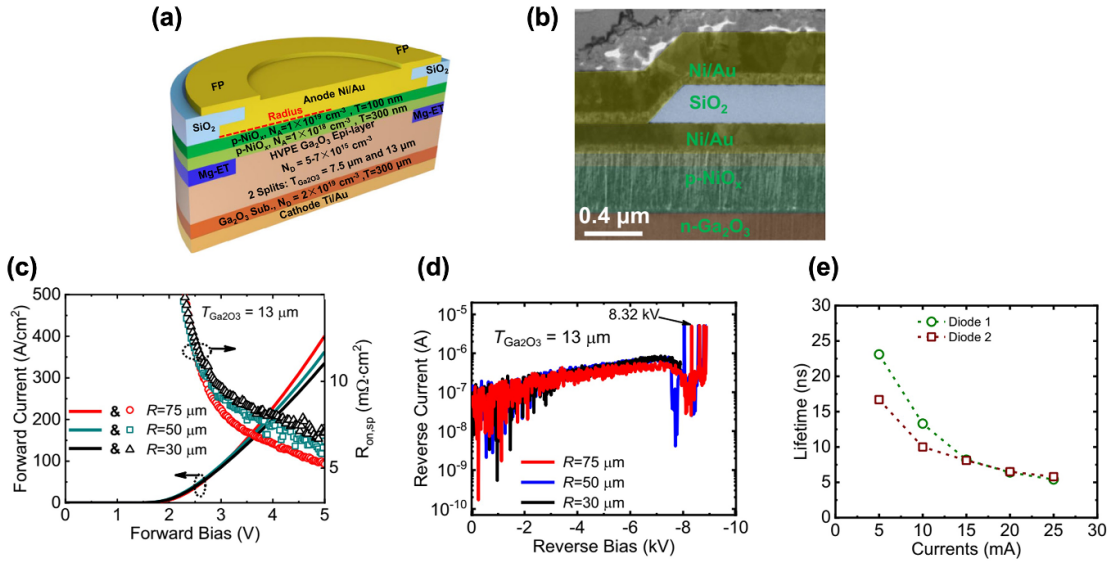

Figure 30. (a) Schematics of the fabricated NiO/Ga_2O_3 heterogeneous PN diodes; (b) SEM image of the cross-sectional anode field plate region; (c) radius-dependent forward current-voltage-resistance curves for a drift layer thickness of 13 μm; (d) radius-dependent reverse breakdown curves for a drift layer thickness of 13 μm; (e) hole lifetime dependence on the forward injection current, measured in reverse recovery transient behavior [354].

5.3. β-Ga_2O_3 device and applications

5.3.1. High power devices

5.3.1.1. SBDs

Ga_2O_3 SBDs were first demonstrated on native n-type Ga_2O_3 substrates, due to the absence of suitable epitaxial growth methods for thick n-drift layers on Ga_2O_3 substrates. In 2013, a Ga_2O_3 SBD fabricated on a bulk (010) substrate grown by the float zone method was reported [410]. A Schottky barrier height of 1.3–1.5 eV was extracted for the Pt contact, and the SBD exhibited a near-unity ideality factor, indicating high crystal quality and good Schottky contact properties. The diodes showed a 150 V breakdown voltage and a high on-resistance of 7.85 mΩ·cm^2, which was attributed to the low conductivity of the bulk substrates. Later, with the advancement of HVPE growth, a 7 μm-thick Si doped drift layer with doping concentration around 2 × 10^{16} cm^{-3} was grown on highly Sn-doped (2.5 × 10^{18} cm^{-3}) (001) native Ga_2O_3 substrates. The fabricated SBDs showed a breakdown voltage of 500 V with an improved on-resistance of 3 mΩ·cm^2 [411]. Catastrophic breakdown occurred in the devices due to the electric-field concentration at the edge of the anode, requiring efficient edge termination to suppress the peak electric field and reduce the leakage current. Several approaches, such as field plating [412–414], junction termination extensions [415–417], and trench metal–insulator–semiconductor (MIS) structures [418, 419], have been proposed and prototyped in Ga_2O_3 SBDs. By deploying a self-aligned field plate with a deep trench filled with thick SiO_2, a 6 kV SBD with a specific on-resistance of 3.4 mΩ·cm^2 was successfully fabricated. This device offered a high BFOM of 10.6 GW cm^{-2} [353] and exceeded the 1D unipolar limit of SiC and GaN.

5.3.1.2. Heterogeneous PN diodes

Though effective p-type β-Ga_2O_3 is still under development, the use of heterogeneous PN structures that employ NiO as the p-type material establishes another route for achieving high voltage diodes [420–425]. The high turn-on voltage, which leads to conduction losses, is characteristic of homogeneous PN structures in WBG materials. However, the band offset of NiO can reduce the threshold voltage, partially resolving this issue [354]. Recently, Zhang *et al* reported a NiO/Ga_2O_3 heterogeneous PN diode by combining Mg implantation termination and field plating architectures with schematics and SEM cross-sections shown in figures 30(a) and (b). These devices produced an 8.32 kV breakdown voltage and the highest BFOM of 13.2 GW cm^{-2} among all UWBG power diodes to date [354]. The reverse recovery behavior of the fabricated heterogeneous PN diodes was measured, and the hole lifetime was determined to be 5.4–23.1 ns (figure 30(e)), yielding a mobility of 1.9–8.3 cm^2 (V·s)$^{-1}$. Despite the difficulties in observing free hole conduction in Ga_2O_3 as discussed in section 5.2.3, this result indicates that holes can be manufactured in Ga_2O_3 via hole injection, and their presence is not limited by the self-trapping effect.

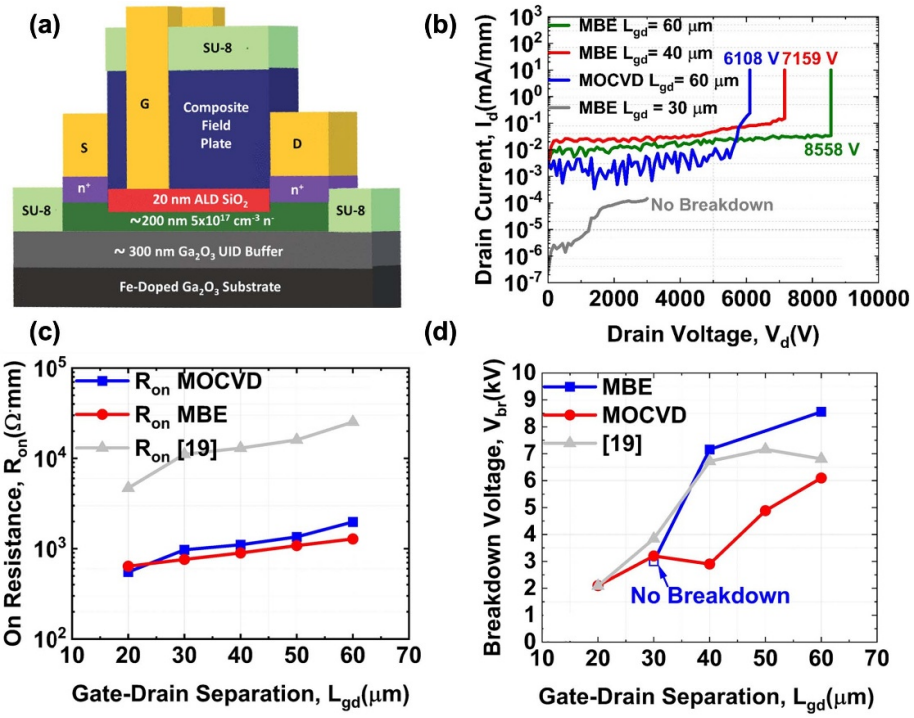

Figure 31. (a) Schematical view of lateral Ga_2O_3 MOSFET based on vacuum annealing with a composite field plate and SU-8 encapsulation layer; (b) breakdown characteristics for the device, the highest breakdown voltage was 8558 V for a 60 μm channel length grown by MBE; (c) comparison of the on-state resistance with vacuum annealing for the channel grown by MOCVD (blue line) and grown by MBE (red line), and without vacuum annealing grown by MBE (gray line); (d) comparison of the breakdown voltage with vacuum annealing for the channel grown by MBE (blue line) and MOCVD (red line), and without vacuum annealing grown by MBE (gray line) [434].

5.3.1.3. MESFETs and lateral MOSFETs

MESFETs were successfully fabricated on Mg-doped semi-insulating Ga_2O_3 substrates in 2011 [352]. A 300 nm thick Sn-doped channel layer was grown by MBE and a Pt/Ti/Au metal stack was deposited as the Schottky gate. The device showed an on–off ratio of 10^4 and a decent three-terminal breakdown voltage of 250 V. However, the unpassivated surface led to a small gate leakage, and the devices suffered from low on-state current due to the high contact resistance of the source/drain electrodes. Later usage of Si ion implantation or diffusion at the source/drain electrode significantly reduced the contact resistance to the order of 10^{-5} $\Omega\cdot cm^2$ [426, 427] and thus resolved a significant limitation of the on-state current for Ga_2O_3 transistors.

MOSFETs have been studied to improve the performance of Ga_2O_3 transistors. Depletion-mode Ga_2O_3 MOSFETs have been demonstrated with an ALD Al_2O_3 layer as the gate dielectric as well as the surface passivation layer to reduce surface leakage [428]. On the other hand, a SiO_2 dielectric/Ga_2O_3 interface was reported to have a large conduction band offset and low interface state density [429], offering an enhancement-mode Ga_2O_3 MOSFET using a Pt gate [430]. These devices showed a breakdown voltage of 400 V without a field plate structure, and the integration of field plate structures enabled a much higher breakdown up to 8 kV [431–433]. Figure 31(a) depicts the device schematic of a lateral Ga_2O_3 MOSFET with a composite field plate design, offering a record-high breakdown voltage of 8.56 kV [434]. The authors reported that vacuum annealing significantly reduced the on-resistance by recovering the surface damage caused by a reactive-ion etching process during fabrication. The on-resistance was reduced by one-order of magnitude while excellent blocking capability was maintained.

5.3.1.4. Vertical transistors

Vertical Ga_2O_3 transistors are favorable in power applications due to their high volume utilization and high power density. Using a fin-shaped channel in vertical transistors (FinFET), as pictured in figure 32(a), removes the need for a p-type material. This structure can also avoid the low effective channel mobility caused by etching damage and interface states in MOSFETs. The demonstration of a 2.6 kV transistor with an on-resistance of 25.2 $m\Omega\cdot cm^2$ [435] promoted continued interest and development of FinFET technology in Ga_2O_3. Although FinFETs have exhibited a high breakdown voltage in Ga_2O_3, the complicated and costly fabrication process with potentially low device yield is a concern for the technology.

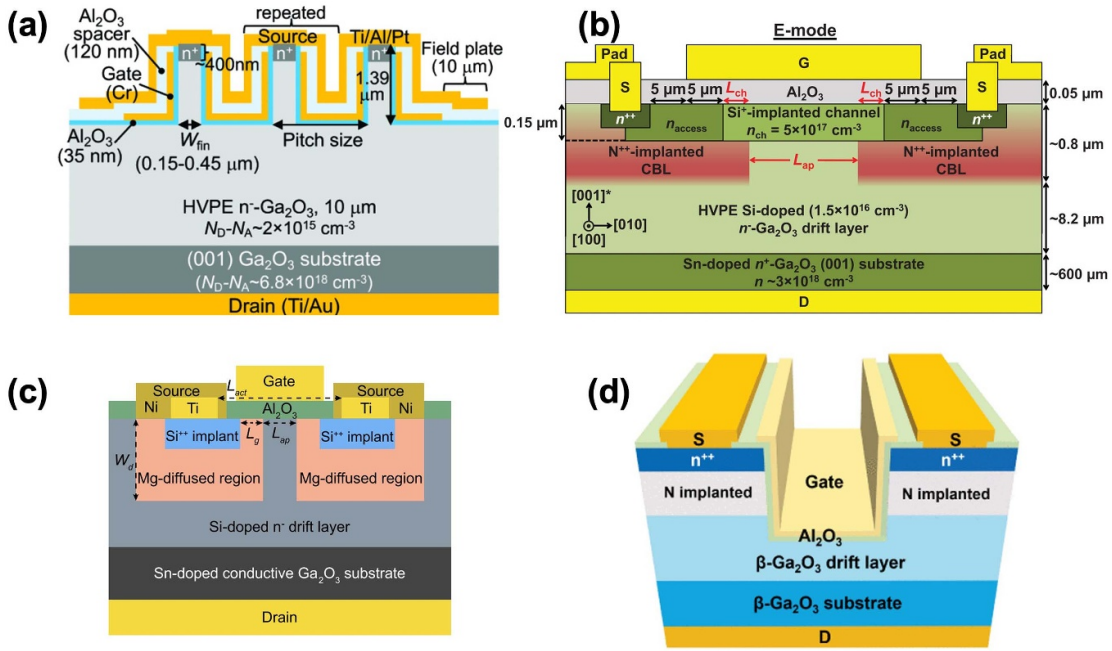

Figure 32. Schematical view of different architectures of vertical Ga_2O_3 transistors: (a) FinFET [435]; (b) current aperture vertical MOSFETs with nitrogen implanted blocker layer [438]; (c) vertical transistor with a diffused barrier (VDBFET) [441]; (d) U-shape trench gate MOSFET with nitrogen ion implantation [442].

Though p-type Ga_2O_3 remains a challenge for the whole community, n-type conductive Ga_2O_3 can be converted to insulating materials by oxygen annealing [436, 437] or by Mg/N implantation or diffusion [438–440]. This can be useful for forming effective current blocking layers in developing vertical transistors. Wong *et al* reported the first Ga_2O_3 CAVET (figure 32(b)) with a Mg implanted blocking layer [439]. However, the devices showed relatively high leakage and poor gate modulation. A possible reason was the diffusion of Mg caused by high temperature annealing used to repair crystal damage after implantation. Later, the same group reported on an N implantation based Ga_2O_3 CAVET [438], demonstrating a breakdown voltage of 253 V with a decent on–off ratio of 10^7, but a large specific resistance of 135 mΩ·cm^2. In contrast to the use of implantation technology, Zeng *et al* utilized an Mg-diffusion process (figure 32(c)) to form a current blocking layer [441], thus avoiding unwanted Mg diffusion during the post-annealing process. The prototype exhibited normally-off operation and a high on–off ratio of 10^8. Though the breakdown voltage was limited to 73 V, this novel diffusion doping method opens an alternative route toward developing vertical Ga_2O_3 transistors.

Similar to SiC and GaN, the U-shaped trench MOSFET (UMOSFET) (figure 32(d)) has also attracted great research interest and was successfully fabricated based on oxygen-annealed and N-implanted channel layers [442, 443]. The nature of the MOSFET made it easy to achieve normally-off operation. Recently, a UMOSFET with a N-implanted current blocking layer exhibited a breakdown voltage of 455 V with a low on-resistance of 10.4 mΩ·cm^2 [442].

5.3.2. RF devices

Green *et al* reported the first RF measurement data in Ga_2O_3 employing a lateral MOSFET architecture with a 180 nm MOVPE-grown Si-doped epitaxial layer on semi-insulating Ga_2O_3 substrates. A gate recess was utilized to reduce the channel thickness to 90 nm [444]. Their devices delivered an f_T of 3.3 GHz and a f_{max} of 12.9 GHz, as well as a continuous wave mode output power of 0.23 W mm^{-1} and PAE of 6.3% measured at a drain voltage of 25 V at 800 MHz. Later, Singh *et al* proved that self-heating was a dominant factor limiting the performance of Ga_2O_3 RF devices [445]. By adopting a pulsed mode measurement method, the device produced 0.13 W mm^{-1} at 1 GHz with a higher PAE of 12%. This finding urges more effective thermal management strategies to address the low TC issue for Ga_2O_3. In addition, the pulsed IV measurements indicated that drain-dispersion, likely caused by traps located either at the surface of the gate dielectric or gate-oxide–semiconductor interface, limited the RF output power as well [446].

Gate length scaling can boost the frequency of RF devices; however, it is limited by the thickness of the channel. A high gate-channel aspect ratio (gate length over gate-to-channel distance) needs to be maintained to suppress the short-channel effect. By growing a 65 nm thick channel layer with a carrier concentration of

2×10^{18} cm^{-3} and decent mobility of 90 cm^2 $(V{\cdot}s)^{-1}$, Chabak *et al* further scaled down the gate length to 140 nm, achieving an f_T/f_{max} of 5.1/17.1 GHz [447]. Kamimura *et al* utilized shallow Si implantation to define a thin channel to maintain the high aspect ratio. Their devices offered a high f_T/f_{max} of 10/27 GHz [448]. Similarly, the growth of a delta-doped Si layer is another way to achieve high sheet charge density and better confinement in the channel, thus enabling an f_T/f_{max} of 27/16 GHz [449]. The $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure is an alternative architecture that can achieve better carrier confinement and reduced effective channel thickness [450, 451]. High carrier densities between 10^{12} and 10^{13} cm^{-2} have been reported in $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ modulation-doped transistors (MODFET) with enhanced carrier mobilities [452–456]. A record-high f_T/f_{max} of 30/37 GHz has recently been reported in $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFETs [457].

5.3.3. Thermal management for Ga_2O_3 devices

Ga_2O_3 is notorious for its low TC and will especially suffer from self-heating. Self-heating not only degrades the reliability and lifetime of a device but also limits its electrical performance. Several cooling strategies have been reported for thermal management at the device level in Ga_2O_3, including heteroepitaxial channel grown on foreign substrates with high TC, wafer bonding to high-thermal-conductivity substrates, and integration of heat spreading layers in close proximity to the active device areas. Details regarding diamond-based thermal management for β-Ga_2O_3 were discussed in section 4.3.2.

Various studies have reported thin Ga_2O_3 epitaxial growth on SiC [458, 459], AlN [460], and diamond substrates [461, 462] due to their much higher thermal conductivities. The TC of an 81 nm thick β-Ga_2O_3 grown on 4H–SiC substrate was measured to be 3.1 ± 0.5 W $(m{\cdot}K)^{-1}$ and the thermal boundary conductance between β-Ga_2O_3/SiC interface was 140 ± 60 MW $(m^2{\cdot}K)^{-1}$ [459]. Despite the promising results shown by thermal characterization and device simulation, experimental demonstration of an active device of Ga_2O_3 on foreign substrates without degrading the electrical performance is yet to be shown.

Besides the direct growth of Ga_2O_3 on foreign substrates, the integration of β-Ga_2O_3 with highly thermally conductive substrates has also been reported through ion cutting [463, 464] and fusion bonding processes [465]. A thermal boundary conductance of 60–130 MW $(m^2{\cdot}K)^{-1}$ between the β-Ga_2O_3/SiC interface formed via the ion cutting process was reported [464]. Minimizing the thermal boundary resistance and Ga_2O_3 substrate thinning is key in facilitating efficient heat removal. A Ga_2O_3 SBD on a thinned-down, 100 μm-thick bulk substrate showed a significant reduction in junction-to-case thermal resistance by 30% compared to the reference device on 250 μm-thick substrates [466], and further substrate thinning to less than 50 μm with the integration of a backside heat sink are predicted to offer further improvements of heat transfer [467].

6. Conclusion

Over the course of recent decades, GaN-based electronics have undergone extensive exploration for various applications, including optoelectronics, high-power devices, and high-frequency electronics. This surge in interest can be attributed to GaN's exceptional material properties. Substantial progress has been achieved in pushing the boundaries of device performance, encompassing both fundamental research and advancements in industrial processes. This continuous improvement in the fields of physics, materials science, and manufacturing processes has expanded the horizons for WBG materials, ushering in new possibilities and catalyzing numerous research breakthroughs, particularly in the realm of UWBG technology. To quantify the progress achieved in the domain of U/WBG materials, figure 33 has been plotted as a benchmark, utilizing Baliga's figure of merit, specifically the relationship between R_{on} and breakdown voltage, as a measure of performance for power devices. Remarkable advances have been made by researchers, resulting in the development of kilovolt-class diodes and transistors across all the materials discussed within this review. This accomplishment underscores the immense potential of these U/WBGs for high-power applications.

In the field of RF applications, GaN HEMTs have demonstrated outstanding performance metrics and have successfully transitioned into commercialization for applications within the X-Ka band. Conversely, the landscape for UWBG materials is still in its nascent stages of development, as depicted in figures 34(a) and (b). These figures vividly illustrate that the state-of-the-art power and RF performance across various UWBG materials significantly lags behind that of GaN.

In the final part of this review article, we are choosing a few common research directions that will significantly impact the WBG to UWBG transition.

Substrates serve as the fundamental building blocks for semiconductor technology, forming the critical foundation upon which it is constructed. The issue of scalable substrates is a pervasive challenge across all the materials under discussion here. Bulk GaN devices have garnered significant research interest due to their potential for higher performance and enhanced reliability. However, the availability of suitable substrates

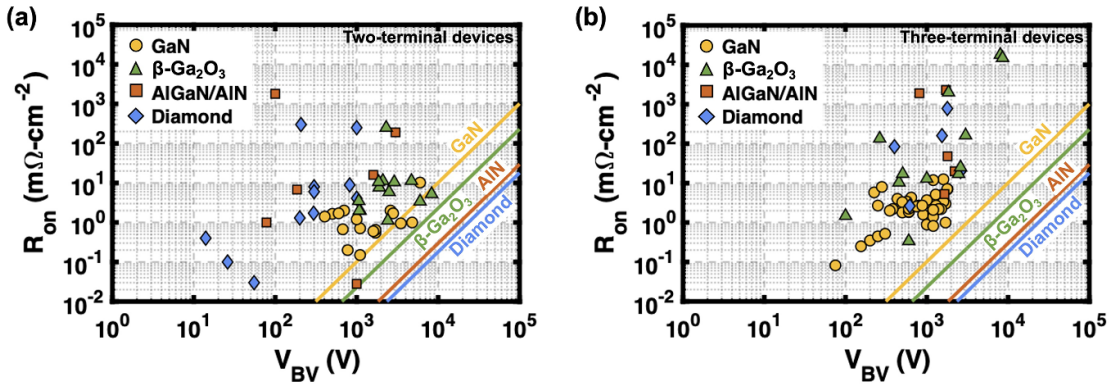

Figure 33. BFOM unipolar limit and experimental data for (a) two-terminal and (b) three-terminal devices. References for (a) GaN SBDs: [61, 67, 69, 72, 73, 468, 469]; GaN PNDs: [79–82, 89, 90, 470]; GaN JBS, SJs: [92, 93, 95]; AlGaN/AlN: [214, 236, 237, 250, 251, 471]; diamond: [281, 287, 292–294, 302, 472–475]; Ga_2O_3 SBDs: [353, 412, 413, 415, 417–419, 476]; Ga_2O_3/NiO PNDs: [354, 421, 423, 424, 477] and (b) lateral GaN: [114, 120, 128, 478, 479] and references therein [480], and references therein; vertical GaN: [131, 134, 135, 139, 141, 145, 147, 481]; AlGaN: [215, 216, 233, 239, 482]; diamond: [309, 312, 483–485]; lateral Ga_2O_3: [432–434, 486, 487] Ga_2O_3 vertical [435, 438, 442, 443, 488, 489].

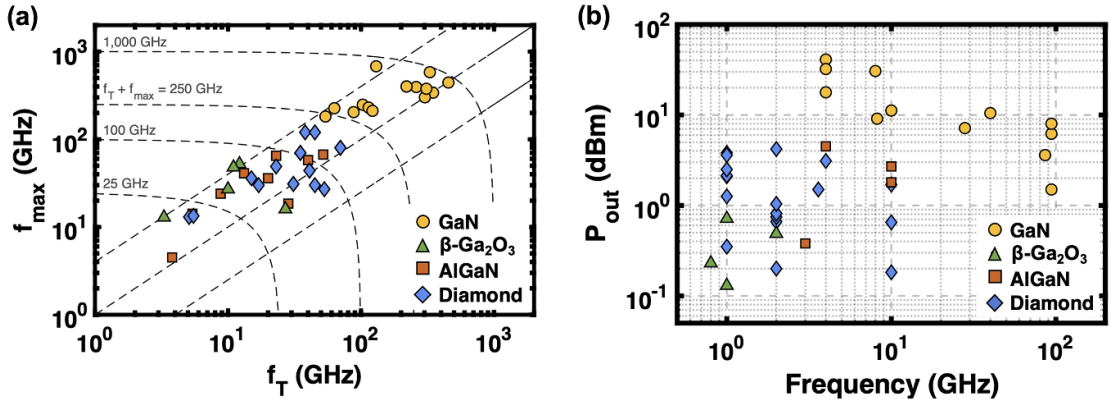

Figure 34. State-of-the-art RF performance: (a) f_{max} vs f_T and (b) P_{out} vs frequency of U/WBG transistors. References for (a) GaN HEMTs: [490–501]; AlGaN: [217, 242–248, 502]; diamond: [321–324, 503–510]; Ga_2O_3: [444, 448, 449, 511] and (b) GaN HEMTs: [157, 159, 160, 164–166, 171, 176, 178, 490, 512]; AlGaN: [217, 242, 247, 248]; diamond: [319, 320, 322, 324, 503–508, 325,513,514]; Ga_2O_3 [444–446].

remains constrained by both size and cost limitations. For instance, the cost of a 2 inch bulk GaN substrate remains prohibitively high, and the commercial availability of substrates larger than 4 inches remains a formidable challenge as of the present date. The development of electrically conducting and optically transparent AlGaN substrates is still in its infancy, and in the case of diamond substrates, typical MPCVD growth methods limit their size to less than 1 cm. Although ongoing efforts in the realm of novel growth methods have resulted in the production of larger substrates, the demonstration of large-diameter bulk GaN, AlN, AlGaN, and diamond substrates with both low defect densities and affordable manufacturing costs remains a formidable hurdle for researchers to overcome.

While it is widely recognized that achieving improved doping control and faster growth rates is imperative for all the materials under discussion, we believe that a pivotal area of research lies in selective area doping within UWBG materials. Selective area doping has the potential to yield remarkable advancements in many device concepts. Generally, due to the substantial bandgap in UWBG materials, the activation of dopants to attain high carrier densities has presented a persistent challenge. The overall proficiency of doping through innovative techniques such as light-assisted doping and selective area regrowth methods holds the promise of facilitating more effective device technology. To date, the absence of reliable n-type and n+ doping methods in diamond, coupled with the scarcity of p-type and p+ doping techniques in AlGaN and the absence of an effective p-type doping method in Ga_2O_3, hinders the creation of properly designed PN junctions, the implementation of effective field termination techniques, and the formation of robust ohmic contacts.

The success of ion-implantation can streamline various processes, offering simplifications with significant implications. For instance, in devices like CAVET, the need for a complex regrowth step could

potentially be reduced or entirely eliminated if ion-implantation can be consistently and effectively achieved. Similarly, the creation of a deep p-well column, essential for fabricating superjunction structures, could become a more practical manufacturing process if ion-implanted dopants could be reliably activated. Therefore, it is imperative to continue researching doping techniques and alternative methods, some of which have been discussed in this review.

For power electronics applications, achieving a robust and uniform avalanche effect in devices is of paramount importance for safeguarding devices against the extreme conditions encountered in real-world scenarios. This capability not only reduces the need for excessive over-design but also permits device operation close to its material limits. While the avalanche phenomenon has been more consistently realized in GaN PN diodes fabricated on native bulk GaN substrates, further data is necessary to fully comprehend the mechanisms and harness their potential in practical applications. However, in UWBG materials, the reliable observation and generation of the avalanche phenomenon remain elusive. This challenge can be attributed in part to the immaturity of the materials and limitations in device architecture, underscoring the need for the development of the physics governing avalanche in UWBGs.

High-k dielectric materials occupy a pivotal role in addressing the requirements of UWBG device technologies. Gate dielectrics with superior electrical strength compared to the semiconductor channel are essential for effective gate technology. These dielectrics must exhibit a very high critical electric field while also providing substantial band offsets to minimize gate leakage. Given the limited space (in thickness) available for the dielectric layer under the gate, the pursuit of high-k value materials becomes crucial. An ideal dielectric should possess a large band offset, a high dielectric constant, low gate leakage, and minimal interface traps to ensure the functionality and reliability of device technology. Insufficiently engineered dielectric layers can significantly impact and even limit a device's performance. Additionally, the emerging branch of nitride ferroelectric gate stacks [515, 516], not discussed in this article, is poised to acquire substantial research interest in the coming decade.

Lastly, the concept of electro-thermal co-design is gaining prominence, particularly in GaN RF devices. Elevated channel temperatures can degrade the mobility of the 2DEG and jeopardize device reliability under high-power operation. Traditional thermal management techniques, such as heat sinks and appropriate thermal interface materials at the package level, remain important. However, the heterogeneous integration of PC diamond with other WBG materials and even silicon technology as a heat-spreading layer presents an alternative approach to device-level cooling. Effective thermal management is essential for UWBG devices, as they are expected to operate at higher voltages and significantly higher power densities, rendering them more susceptible to thermal-related issues.

In summary, U/WBGs represent a highly fascinating and rapidly advancing domain, offering the scientific community a vast array of research prospects in both materials science and device physics. The anticipated range of applications is equally promising, following the path set by SiC and GaN.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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References

[1] Dogmus E, Chiu P and Ayari T (Yole Intelligence) 2022 SiC and GaN: an industry driven by different engines *EE TIMES 50th Anniversary Special Edition: The Next Silicon Frontier*

[2] Ghorbel A, Dogmus E and Chiu P (Yole Intelligence) 2023 RF GaN market broadens its appeal with an appetite for GaN-on-silicon *Microw. J.* **66** 72–82
[3] Tsao J Y *et al* 2018 Ultrawide-bandgap semiconductors: research opportunities and challenges *Adv. Electron. Mater.* **4** 1
[4] Hudgins J L, Simin G S, Santi E and Khan M A 2003 An assessment of wide bandgap semiconductors for power devices *IEEE Trans. Power Electron.* **18** 3
[5] She X, Huang A Q, Lucía Ó and Ozpineci B 2017 Review of silicon carbide power devices and their applications *IEEE Trans. Ind. Electron.* **64** 8193–205
[6] Papanasam E, Prashanth Kumar B, Chanthini B, Manikandan E and Agarwal L 2022 A comprehensive review of recent progress, prospect and challenges of silicon carbide and its applications *Silicon* **14** 12887–900
[7] Mnatsakanov T T, Levinshtein M E, Pomortseva L I, Yurkov S N, Simin G S and Asif Khan M 2003 Carrier mobility model for GaN *Solid-State Electron.* **47** 111–5
[8] Gaska R, Yang J W, Osinsky A, Chen Q, Khan M A, Orlov A O, Snider G L and Shur M S 1998 Electron transport in AlGaN–GaN heterostructures grown on 6H–SiC substrates *Appl. Phys. Lett.* **72** 707–9
[9] Bhapkar U V and Shur M S 1997 Monte Carlo calculation of velocity-field characteristics of wurtzite GaN *J. Appl. Phys.* **82** 1649–55
[10] Ardaravičius L, Matulionis A, Liberis J, Kiprijanovic O, Ramonas M, Eastman L F, Shealy J R and Vertiatchikh A 2003 Electron drift velocity in AlGaN/GaN channel at high electric fields *Appl. Phys. Lett.* **83** 4038–40
[11] Ji D, Ercan B and Chowdhury S 2019 Experimental determination of hole impact ionization coefficient and saturation velocity in GaN *2019 Compound Semiconductor Week (CSW)* pp 1–2
[12] Ji D, Ercan B and Chowdhury S 2020 Experimental determination of velocity-field characteristic of holes in GaN *IEEE Electron Device Lett.* **41** 23–25
[13] Cao L, Wang J, Harden G, Ye H, Stillwell R, Hoffman A J and Fay P 2018 Experimental characterization of impact ionization coefficients for electrons and holes in GaN grown on bulk GaN substrates *Appl. Phys. Lett.* **112** 262103
[14] Ji D, Ercan B and Chowdhury S 2019 Experimental determination of impact ionization coefficients of electrons and holes in gallium nitride using homojunction structures *Appl. Phys. Lett.* **115** 073503
[15] Maeda T, Narita T, Ueda H, Kanechika M, Uesugi T, Kachi T, Kimoto T, Horita M and Suda J 2019 Measurement of avalanche multiplication utilizing Franz-Keldysh effect in GaN p-n junction diodes with double-side-depleted shallow bevel termination *Appl. Phys. Lett.* **115** 142101
[16] Ji D and Chowdhury S 2020 On impact ionization and avalanche in gallium nitride *Appl. Phys. Lett.* **117** 252107
[17] Jeżowski A, Danilchenko B A, Boćkowski M, Grzegory I, Krukowski S, Suski T and Paszkiewicz T 2003 Thermal conductivity of GaN crystals in 4.2–300 K range *Solid State Commun.* **128** 69–73
[18] Zou J, Kotchetkov D, Balandin A A, Florescu D I and Pollak F H 2002 Thermal conductivity of GaN films: effects of impurities and dislocations *J. Appl. Phys.* **92** 2534–9
[19] Utsumi W, Saitoh H, Kaneko H, Watanuki T, Aoki K and Shimomura O 2003 Congruent melting of gallium nitride at 6 GPa and its application to single-crystal growth *Nat. Mater.* **2** 735–8
[20] Dwiliński R, Doradziński R, Garczyński J, Sierzputowski L, Kucharski R, Zając M, Rudziński M, Kudrawiec R, Strupiński W and Misiewicz J 2011 Ammonothermal GaN substrates: growth accomplishments and applications *Phys. Status Solidi* a **208** 1489–93
[21] Mori Y, Imade M, Maruyama M, Yoshimura M, Kawamura F and Kawamura T 2015 *Handbook of Crystal Growth: Bulk Crystal Growth: Basic Techniques* 2nd edn, ed P Rudolph (Elsevier) p 505
[22] Bockowski M, Iwinska M, Amilusik M, Fijalkowski M, Lucznik B and Sochacki T 2016 Challenges and future perspectives in HVPE-GaN growth on ammonothermal GaN seeds *Semicond. Sci. Technol.* **31** 093002
[23] Dwiliński R, Doradziński R, Garczyński J, Sierzputowski L, Baranowski J M and Kamińska M 1997 Exciton photo-luminescence of GaN bulk crystals grown by the AMMONO method *Mater. Sci. Eng.* B **50** 46–49
[24] Xu K, Wang J-F and Ren G-Q 2015 Progress in bulk GaN growth* *Chin. Phys.* B **24** 066105
[25] Hashimoto T, Fujito K, Saito M, Speck J S and Nakamura S 2005 Ammonothermal growth of GaN on an over-1-inch seed crystal *Jpn. J. Appl. Phys.* **44** L1570
[26] Wang B, Callahan M J, Rakes K D, Bouthillette L O, Wang S-Q, Bliss D F and Kolis J W 2006 Ammonothermal growth of GaN crystals in alkaline solutions *J. Cryst. Growth* **287** 376–80
[27] Aoki M, Yamane H, Shimada M, Sarayama S and DiSalvo F J 2002 GaN single crystal growth using high-purity Na as a flux *J. Cryst. Growth* **242** 70–76
[28] Kawamura F, Iwahashi T, Morishita M, Omae K, Yoshimura M, Mori Y and Sasaki T 2003 Growth of transparent, large size GaN single crystal with low dislocations using Ca-Na flux system *Jpn. J. Appl. Phys.* **42** L729
[29] Morishita M, Kawamura F, Kawahara M, Yoshimura M, Mori Y and Sasaki T 2005 Promoted nitrogen dissolution due to the addition of Li or Ca to Ga-Na melt; some effects of additives on the growth of GaN single crystals using the sodium flux method *J. Cryst. Growth* **284** 91–99
[30] Kawamura F, Morishita M, Omae K, Yoshimura M, Mori Y and Sasaki T 2005 The effects of Na and some additives on nitrogen dissolution in the Ga-Na system: a growth mechanism of GaN in the Na flux method *J. Mater. Sci., Mater. Electron.* **16** 29–34
[31] Mori Y, Imanishi M, Murakami K and Yoshimura M 2019 Recent progress of Na-flux method for GaN crystal growth *Jpn. J. Appl. Phys.* **58** SC0803
[32] Imade M, Hirabayashi Y, Konishi Y, Ukegawa H, Miyoshi N, Yoshimura M, Sasaki T, Kitaoka Y and Mori Y 2010 Growth of large GaN single crystals on high-quality GaN seed by carbon-added Na flux method *Appl. Phys. Express* **3** 075501
[33] Fujito K, Kubo S, Nagaoka H, Mochizuki T, Namita H and Nagao S 2009 Bulk GaN crystals grown by HVPE *J. Cryst. Growth* **311** 3011–4
[34] Kucharski R, Sochacki T, Lucznik B and Bockowski M 2020 Growth of bulk GaN crystals *J. Appl. Phys.* **128** 050902
[35] Ilegems M and Montgomery H C 1973 Electrical properties of n-type vapor-grown gallium nitride *J. Phys. Chem. Solids* **34** 885–95
[36] Usui A, Sunakawa H, Sakai A and Yamaguchi A A 1997 Thick GaN epitaxial growth with low dislocation density by hydride vapor phase epitaxy *Jpn. J. Appl. Phys.* **36** L899
[37] Götz W, Romano L T, Walker J, Johnson N M and Molnar R J 1998 Hall-effect analysis of GaN films grown by hydride vapor phase epitaxy *Appl. Phys. Lett.* **72** 1214–6
[38] Fujikura H, Konno T, Yoshida T and Horikiri F 2017 Hydride-vapor-phase epitaxial growth of highly pure GaN layers with smooth as-grown surfaces on freestanding GaN substrates *Jpn. J. Appl. Phys.* **56** 085503
[39] Moustakas T D, Lei T and Molnar R J 1993 Growth of GaN by ECR-assisted MBE *Physica* B **185** 36–49

[40] Molnar R J and Moustakas T D 1994 Growth of gallium nitride by electron-cyclotron resonance plasma-assisted molecular-beam epitaxy: the role of charged species *J. Appl. Phys.* **76** 4587–95
[41] Hughes W C, Rowland W H, Johnson M A L, Fujita S, Cook J W, Schetzina J F, Ren J and Edmond J A 1995 Molecular beam epitaxy growth and properties of GaN films on GaN/SiC substrates *J. Vac. Sci. Technol.* B **13** 1571–7
[42] Heinke H, Kirchner V, Einfeldt S and Hommel D 2000 X-ray diffraction analysis of the defect structure in epitaxial GaN *Appl. Phys. Lett.* **77** 2145–7
[43] Matloubian M and Gershenzon M 1985 MOCVD epitaxial growth of single crystal GaN, AlN and $Al_xGa_{1-x}N$ *J. Electron. Mater.* **14** 633–44
[44] Miskys C R, Kelly M K, Ambacher O and Stutzmann M 1999 MOCVD-epitaxy on free-standing HVPE-GaN substrates *Phys. Status Solidi* a **176** 443–6
[45] Pandey A, Yadav B S, Rao D V S, Kaur D and Kapoor A K 2016 Dislocation density investigation on MOCVD-grown GaN epitaxial layers using wet and dry defect selective etching *Appl. Phys.* A **122** 614
[46] Amano H, Sawaki N, Akasaki I and Toyoda Y 1986 Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer *Appl. Phys. Lett.* **48** 353–5
[47] Flack T J, Pushpakaran B N and Bayne S B 2016 GaN technology for power electronic applications: a review *J. Electron. Mater.* **45** 2673–82
[48] Sheu J K and Chi G C 2002 The doping process and dopant characteristics of GaN *J. Phys.* **14** R657
[49] Nakamura S, Takashi Mukai T M and Masayuki Senoh M S 1992 Si- and Ge-doped GaN films grown with GaN buffer layers *Jpn. J. Appl. Phys.* **31** 2883
[50] Murakami H, Asahi T, Amano H, Hiramatsu K, Sawaki N and Akasaki I 1991 Growth of Si-doped $Al_xGa_{1-x}N$ on (0001) sapphire substrate by metalorganic vapor phase epitaxy *J. Cryst. Growth* **115** 648–51
[51] Wickenden A E, Rowland L B, Doverspike K, Gaskill D K, Freitas J A, Simons D S and Chi P H 1995 Doping of gallium nitride using disilane *J. Electron. Mater.* **24** 1547–50
[52] Götz W, Johnson N M, Chen C, Liu H, Kuo C and Imler W 1996 Activation energies of Si donors in GaN *Appl. Phys. Lett.* **68** 3144–6
[53] Perlin P *et al* 1995 Towards the identification of the dominant donor in GaN *Phys. Rev. Lett.* **75** 296–9
[54] Zhang G Y, Tong Y Z, Yang Z J, Jin S X, Li J and Gan Z Z 1997 Relationship of background carrier concentration and defects in GaN grown by metalorganic vapor phase epitaxy *Appl. Phys. Lett.* **71** 3376–8
[55] Nakamura S, Mukai T, Masayuki Senoh M S and Naruhito Iwasa N I 1992 Thermal annealing effects on P-type Mg-doped GaN films *Jpn. J. Appl. Phys.* **31** L139
[56] Yasuo Ohba Y O and Ako Hatano A H 1994 H-atom incorporation in Mg-doped GaN grown by metalorganic chemical vapor deposition *Jpn. J. Appl. Phys.* **33** L1367
[57] Amano H, Kito M, Hiramatsu K and Akasaki I 1989 P-type conduction in Mg-doped GaN treated with low-energy electron beam irradiation (LEEBI) *Jpn. J. Appl. Phys.* **28** L2112
[58] Tanaka T, Watanabe A, Amano H, Kobayashi Y, Akasaki I, Yamazaki S and Koike M 1994 p-type conduction in Mg-doped GaN and $Al_{0.08}Ga_{0.92}N$ grown by metalorganic vapor phase epitaxy *Appl. Phys. Lett.* **65** 593–4
[59] Huang J W, Kuech T F, Lu H and Bhat I 1996 Electrical characterization of Mg-doped GaN grown by metalorganic vapor phase epitaxy *Appl. Phys. Lett.* **68** 2392–4
[60] Johnson C, Lin J Y, Jiang H X, Khan M A and Sun C J 1996 Metastability and persistent photoconductivity in Mg-doped p-type GaN *Appl. Phys. Lett.* **68** 1808–10
[61] Saitoh Y, Sumiyoshi K, Okada M, Horii T, Miyazaki T, Shiomi H, Ueno M, Katayama K, Kiyama M and Nakamura T 2010 Extremely low on-resistance and high breakdown voltage observed in vertical GaN Schottky barrier diodes with high-mobility drift layers on low-dislocation-density GaN substrates *Appl. Phys. Express* **3** 081001
[62] Tanaka N, Hasegawa K, Yasunishi K, Murakami N and Oka T 2015 50 A vertical GaN Schottky barrier diode on a free-standing GaN substrate with blocking voltage of 790 V *Appl. Phys. Express* **8** 071001
[63] Ozbek A M and Baliga B J 2011 Planar nearly ideal edge-termination technique for GaN devices *IEEE Electron Device Lett.* **32** 300–2
[64] Ozbek A M and Baliga B J 2011 Finite-zone argon implant edge termination for high-voltage GaN Schottky rectifiers *IEEE Electron Device Lett.* **32** 1361–3
[65] Wang M J, Yuan L, Cheng C C, Beling C D and Chen K J 2009 Defect formation and annealing behaviors of fluorine-implanted GaN layers revealed by positron annihilation spectroscopy *Appl. Phys. Lett.* **94** 061910
[66] Wang M J, Yuan L, Chen K J, Xu F J and Shen B 2009 Diffusion mechanism and the thermal stability of fluorine ions in GaN after ion implantation *J. Appl. Phys.* **105** 083519
[67] Liu Z, Wang J, Gu H, Zhang Y, Wang W, Xiong R and Xu K 2019 High-voltage vertical GaN-on-GaN Schottky barrier diode using fluorine ion implantation treatment *AIP Adv.* **9** 055016
[68] Zhang Z, Li B, Qian Q, Tang X, Hua M, Huang B and Chen K J 2017 Revealing the nitridation effects on GaN surface by first-principles calculation and x-ray/ultraviolet photoemission spectroscopy *IEEE Trans. Electron Devices* **64** 4036–43
[69] Han S, Yang S and Sheng K 2018 High-voltage and high-I_{ON}/I_{OFF} vertical GaN-on-GaN Schottky barrier diode with nitridation-based termination *IEEE Electron Device Lett.* **39** 572–5
[70] Mehrotra M and Baliga B J 1995 Trench MOS Barrier Schottky (TMBS) rectifier: a Schottky rectifier with higher than parallel plane breakdown voltage *Solid-State Electron.* **38** 801–6
[71] Hasegawa K, Nishio G, Yasunishi K, Tanaka N, Murakami N and Oka T 2017 Vertical GaN trench MOS barrier Schottky rectifier maintaining low leakage current at 200° C with blocking voltage of 750 V *Appl. Phys. Express* **10** 121002
[72] Jia X, Chen S-W H, Liu Y, Hou X, Zhang Y, Zhang Z-H and Kuo H-C 2020 Design strategies for mesa-type GaN-based Schottky barrier diodes for obtaining high breakdown voltage and low leakage current *IEEE Trans. Electron Devices* **67** 1931–8
[73] Zhang Y *et al* 2016 Novel GaN trench MIS barrier Schottky rectifiers with implanted field rings *2016 IEEE Int. Electron Devices Meeting (IEDM)* pp 10.2.1–4
[74] Li S, Ercan B, Ren C, Ikeda H and Chowdhury S 2022 A study on the impact of dislocation density on leakage current in vertical GaN-on-GaN p-n diodes *IEEE Trans. Electron Devices* **69** 4206–11
[75] Fukushima H, Usami S, Ogura M, Ando Y, Tanaka A, Deki M, Kushimoto M, Nitta S, Honda Y and Amano H 2019 Vertical GaN p–n diode with deeply etched mesa and the capability of avalanche breakdown *Appl. Phys. Express* **12** 026502
[76] Maeda T, Narita T, Ueda H, Kanechika M, Uesugi T, Kachi T, Kimoto T, Horita M and Suda J 2019 Design and fabrication of GaN p-n junction diodes with negative beveled-mesa termination *IEEE Electron Device Lett.* **40** 941–4

[77] Zeng K and Chowdhury S 2020 Designing beveled edge termination in GaN vertical p-i-n diode-bevel angle, doping, and passivation *IEEE Trans. Electron Devices* **67** 2457–62
[78] Zeng K, Chowdhury S, Gunning B, Kaplar R and Anderson T 2021 Study on avalanche uniformity in 1.2 KV GaN vertical PIN diode with bevel edge-termination *2021 IEEE Int. Reliability Physics Symp. (IRPS)* pp 1–4
[79] Nomoto K, Song B, Hu Z, Zhu M, Qi M, Kaneda N, Mishima T, Nakamura T, Jena D and Xing H G 2016 1.7-kV and 0.55-mΩ. cm^2 GaN p-n diodes on bulk GaN substrates with avalanche capability *IEEE Electron Device Lett.* **37** 161–4
[80] Nomoto K *et al* 2015 GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ-cm^2: a record high figure-of-merit of 12.8 GW/cm^2 *2015 IEEE Int. Electron Devices Meeting (IEDM)* pp 9.7.1–4
[81] Ohta H, Asai N, Horikiri F, Narita Y, Yoshida T and Mishima T 2020 Two-step mesa structure GaN p-n diodes with low ON-resistance, high breakdown voltage, and excellent avalanche capabilities *IEEE Electron Device Lett.* **41** 123–6
[82] Yates L *et al* 2022 Demonstration of >6.0-kV breakdown voltage in large area vertical GaN p-n diodes with step-etched junction termination extensions *IEEE Trans. Electron Devices* **69** 1931–7
[83] Ji D, Li S, Ercan B, Ren C and Chowdhury S 2020 Design and fabrication of ion-implanted moat etch termination resulting in 0.7 mΩ.cm^2/1500 V GaN diodes *IEEE Electron Device Lett.* **41** 264–7
[84] Wang J *et al* 2017 High voltage vertical p-n diodes with ion-implanted edge termination and sputtered SiN_x passivation on GaN substrates *2017 IEEE Int. Electron Devices Meeting (IEDM)* pp 9.6.1–4
[85] Cao L, Ye H, Wang J and Fay P 2020 Avalanche multiplication noise in GaN p–n junctions grown on native GaN substrates *Phys. Status Solidi* b **257** 1900373
[86] Fu H *et al* 2019 Implantation-and etching-free high voltage vertical GaN p–n diodes terminated by plasma-hydrogenated p-GaN: revealing the role of thermal annealing *Appl. Phys. Express* **12** 051015
[87] Fu H, Fu K, Huang X, Chen H, Baranowski I, Yang T-H, Montes J and Zhao Y 2018 High performance vertical GaN-on-GaN p-n power diodes with hydrogen-plasma-based edge termination *IEEE Electron Device Lett.* **39** 1018–21
[88] Okamoto Y, Saito M and Oshiyama A 1996 First-principles calculations on Mg impurity and Mg–H complex in GaN *Jpn. J. Appl. Phys.* **35** L807
[89] Fu H *et al* 2020 High voltage vertical GaN p-n diodes with hydrogen-plasma based guard rings *IEEE Electron Device Lett.* **41** 127–30
[90] Bian Z, Zeng K and Chowdhury S 2022 2.8 kV avalanche in vertical GaN PN diode utilizing field plate on hydrogen passivated P-layer *IEEE Electron Device Lett.* **43** 596–9
[91] Koehler A D, Anderson T J, Tadjer M J, Nath A, Feigelson B N, Shahin D I, Hobart K D and Kub F J 2016 Vertical GaN junction barrier Schottky diodes *ECS J. Solid State Sci. Technol.* **6** Q10
[92] Zhang Y *et al* 2017 Vertical GaN junction barrier Schottky rectifiers by selective ion implantation *IEEE Electron Device Lett.* **38** 1097–100
[93] Matys M, Kitagawa K, Narita T, Uesugi T, Suda J and Kachi T 2022 Mg-implanted vertical GaN junction barrier Schottky rectifiers with low on resistance, low turn-on voltage, and nearly ideal nondestructive breakdown voltage *Appl. Phys. Lett.* **121** 203507
[94] Zhou F, Xu W, Ren F, Zhou D, Chen D, Zhang R, Zheng Y, Zhu T and Lu H 2021 Demonstration of avalanche and surge current robustness in GaN junction barrier Schottky diode with 600-V/10-A switching capability *IEEE Trans. Power Electron.* **36** 12163–7
[95] Xiao M *et al* 2022 First demonstration of vertical superjunction diode in GaN *2022 Int. Electron Devices Meeting (IEDM)* pp 35.6.1–4
[96] Ambacher O, Christian B, Yassine M, Baeumler M, Leone S and Quay R 2021 Polarization induced interface and electron sheet charges of pseudomorphic ScAlN/GaN, GaAlN/GaN, InAlN/GaN, and InAlN/InN heterostructures *J. Appl. Phys.* **129** 204501
[97] He X-G, Zhao D-G and Jiang D-S 2015 Formation of two-dimensional electron gas at AlGaN/GaN heterostructure and the derivation of its sheet density expression* *Chin. Phys.* B **24** 067301
[98] Kikkawa T *et al* 2014 600 V JEDEC-qualified highly reliable GaN HEMTs on Si substrates *2014 IEEE Int. Electron Devices Meeting* pp 2.6.1–4
[99] Kikkawa T *et al* 2015 Commercialization and reliability of 600 V GaN power switches *2015 IEEE Int. Reliability Physics Symp.* pp 6C.1.1–6
[100] Haeberlen M, Zhu D, McAleese C, Kappers M J and Humphreys C J 2010 Dislocation reduction in MOVPE grown GaN layers on (111)Si using SiN_x and AlGaN layers *J. Phys.: Conf. Ser.* **209** 012017
[101] Gupta C, Enatsu Y, Gupta G, Keller S and Mishra U K 2016 High breakdown voltage p–n diodes on GaN on sapphire by MOCVD *Phys. Status Solidi* a **213** 878–82
[102] Gmeinwieser N *et al* 2004 Correlation of strain, wing tilt, dislocation density, and photoluminescence in epitaxial lateral overgrown GaN on SiC substrates *J. Appl. Phys.* **96** 3666–72
[103] Christy D, Watanabe A and Egawa T 2014 Influence of strain induced by AlN nucleation layer on the electrical properties of AlGaN/GaN heterostructures on Si(111) substrate *AIP Adv.* **4** 107104
[104] Dadgar A *et al* 2003 MOVPE growth of GaN on Si(111) substrates *J. Cryst. Growth* **248** 556–62
[105] Leung B, Han J and Sun Q 2014 Strain relaxation and dislocation reduction in AlGaN step-graded buffer for crack-free GaN on Si (111) *Phys. Status Solidi* c **11** 437–41
[106] Tajalli A *et al* 2020 High breakdown voltage and low buffer trapping in superlattice GaN-on-silicon heterostructures for high voltage applications *Materials* **13** 4271
[107] Sorrentino G, Melito M, Patti A, Parrino G and Raciti A 2013 GaN HEMT devices: experimental results on normally-on, normally-off and cascode configuration *IECON 2013–39th Annual Conf. IEEE Industrial Electronics Society* pp 816–21
[108] Huang X, Li Q, Liu Z and Lee F C 2014 Analytical loss model of high voltage GaN HEMT in cascode configuration *IEEE Trans. Power Electron.* **29** 2208–19
[109] Huang X, Liu Z, Li Q and Lee F C 2013 Evaluation and application of 600V GaN HEMT in cascode structure *2013 28th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC)* pp 1279–86
[110] Ren J, Tang C W, Feng H, Jiang H, Yang W, Zhou X, Lau K M and Sin J K O 2018 A novel 700 V monolithically integrated Si-GaN cascoded field effect transistor *IEEE Electron Device Lett.* **39** 394–6
[111] Meneghini M *et al* 2021 GaN-based power devices: physics, reliability, and perspectives *J. Appl. Phys.* **130** 181101
[112] He Y, Gao H, Wang C, Zhao Y, Lu X, Zhang C, Zheng X, Guo L, Ma X and Hao Y 2019 Comparative study between partially and fully recessed-gate enhancement-mode AlGaN/GaN MIS HEMT on the breakdown mechanism *Phys. Status Solidi* a **216** 1900115
[113] Shi Y *et al* 2016 Normally OFF GaN-on-Si MIS-HEMTs fabricated with LPCVD-SiN_x passivation and high-temperature gate recess *IEEE Trans. Electron Devices* **63** 614–9

[114] Saito W, Takada Y, Kuraguchi M, Tsuda K and Omura I 2006 Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications *IEEE Trans. Electron Devices* **53** 356–62
[115] Greco G, Giannazzo F, Frazzetto A, Raineri V and Roccaforte F 2011 Near-surface processing on AlGaN/GaN heterostructures: a nanoscale electrical and structural characterization *Nanoscale Res. Lett.* **6** 132
[116] Acurio E, Crupi F, Magnone P, Trojman L and Iucolano F 2017 Impact of AlN layer sandwiched between the GaN and the Al_2O_3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs *Microelectron. Eng.* **178** 42–47
[117] Hosoi T, Watanabe K, Nozaki M, Yamada T, Shimura T and Watanabe H 2019 Mobility enhancement in recessed-gate AlGaN/GaN MOS-HFETs using an AlON gate insulator *Jpn. J. Appl. Phys.* **58** SCCD16
[118] Fiorenza P, Greco G, Giannazzo F, Iucolano F and Roccaforte F 2017 Effects of interface states and near interface traps on the threshold voltage stability of GaN and SiC transistors employing SiO_2 as gate dielectric *J. Vac. Sci. Technol.* B **35** 01A101
[119] He J, Hua M, Zhang Z and Chen K J 2018 Performance and V_{TH} stability in E-mode GaN fully recessed MIS-FETs and partially recessed MIS-HEMTs with LPCVD-SiN_x/PECVD-SiN_x gate dielectric stack *IEEE Trans. Electron Devices* **65** 3185–91
[120] Suh C S, Dora Y, Fichtenbaum N, McCarthy L, Keller S and Mishra U K 2006 High-breakdown enhancement-mode AlGaN/GaN HEMTs with integrated slant field-plate *2006 Int. Electron Devices Meeting* pp 1–3
[121] Cai Y, Zhou Y, Lau K M and Chen K J 2006 Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: from depletion mode to enhancement mode *IEEE Trans. Electron Devices* **53** 2207–15
[122] Cai Y, Zhou Y, Chen K J and Lau K M 2005 High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment *IEEE Electron Device Lett.* **26** 435–7
[123] Kang S C *et al* 2020 Charging effect by fluorine-treatment and recess gate for enhancement-mode on AlGaN/GaN high electron mobility transistors *Nanomaterials* **10** 2116
[124] Chen K J and Zhou C 2011 Enhancement-mode AlGaN/GaN HEMT and MIS-HEMT technology *Phys. Status Solidi* a **208** 434–8
[125] Meneghini M, Hilt O, Wuerfl J and Meneghesso G 2017 Technology and reliability of normally-off GaN HEMTs with p-type gate *Energies* **10** 153
[126] Greco G, Iucolano F, Di Franco S, Bongiorno C, Patti A and Roccaforte F 2016 Effects of annealing treatments on the properties of Al/Ti/p-GaN interfaces for normally OFF p-GaN HEMTs *IEEE Trans. Electron Devices* **63** 2735–41
[127] Bakeroot B, Stockman A, Posthuma N, Stoffels S and Decoutere S 2018 Analytical model for the threshold voltage of p-(Al)GaN high-electron-mobility transistors *IEEE Trans. Electron Devices* **65** 79–86
[128] Uemoto Y, Hikita M, Ueno H, Matsuo H, Ishida H, Yanagihara M, Ueda T, Tanaka T and Ueda D 2007 Gate injection transistor (GIT) normally-off AlGaN/GaN power transistor using conductivity modulation *IEEE Trans. Electron Devices* **54** 3393–9
[129] Kaneko S *et al* 2015 Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain *2015 IEEE 27th Int. Symp. on Power Semiconductor Devices & IC's (ISPSD)* pp 41–44
[130] Otake H, Egami S, Ohta H, Nanishi Y and Takasu H 2007 GaN-based trench gate metal oxide semiconductor field effect transistors with over 100 cm^2/(V.s) channel mobility *Jpn. J. Appl. Phys.* **46** L599
[131] Oka T, Ina T, Ueno Y and Nishii J 2015 1.8 mΩ cm^2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation *Appl. Phys. Express* **8** 054101
[132] Gupta C, Chan S H, Enatsu Y, Agarwal A, Keller S and Mishra U K 2016 OG-FET: an in-situ oxide, GaN interlayer-based vertical trench MOSFET *IEEE Electron Device Lett.* **37** 1601–4
[133] Gupta C, Chan S H, Agarwal A, Hatui N, Keller S and Mishra U K 2017 First demonstration of AlSiO as gate dielectric in GaN FETs; applied to a high performance OG-FET *IEEE Electron Device Lett.* **38** 1575–8
[134] Ji D *et al* 2017 Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices *2017 IEEE Int. Electron Devices Meeting (IEDM)* pp 9.4.1–4
[135] Tanaka R, Takashima S, Ueno K, Matsuyama H and Edo M 2020 Demonstration of 1200 V/1.4 mΩ cm^2 vertical GaN planar MOSFET fabricated by an all ion implantation process *Jpn. J. Appl. Phys.* **59** SGGD02
[136] Chowdhury S, Swenson B L and Mishra U K 2008 Enhancement and depletion mode AlGaN/GaN CAVET with Mg-Ion-implanted GaN as current blocking layer *IEEE Electron Device Lett.* **29** 543–5
[137] Mandal S, Agarwal A, Ahmadi E, Bhat K M, Ji D, Laurent M A, Keller S and Chowdhury S 2017 Dispersion free 450-V p GaN-gated CAVETs with Mg-ion implanted blocking layer *IEEE Electron Device Lett.* **38** 933–6
[138] Ji D, Laurent M A, Agarwal A, Li W, Mandal S, Keller S and Chowdhury S 2017 Normally OFF trench CAVET with active Mg-doped GaN as current blocking layer *IEEE Trans. Electron Devices* **64** 805–8
[139] Nie H, Diduck Q, Alvarez B, Edwards A P, Kayes B M, Zhang M, Ye G, Prunty T, Bour D and Kizilyalli I C 2014 1.5-kV and 2.2-mΩ cm^2 vertical GaN transistors on bulk-GaN substrates *IEEE Electron Device Lett.* **35** 939–41
[140] Gupta C and Pasayat S S 2022 Vertical GaN and vertical Ga_2O_3 power transistors: status and challenges *Phys. Status Solidi* a **219** 2100659
[141] Shibata D *et al* 2016 1.7 kV/1.0 mΩcm^2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure *2016 IEEE Int. Electron Devices Meeting (IEDM)* pp 10.1.1–4
[142] Šichman P *et al* 2020 Semi-insulating GaN for vertical structures: role of substrate selection and growth pressure *Mater. Sci. Semicond. Process.* **118** 105203
[143] Šichman P *et al* 2023 Vertical GaN transistor with semi-insulating channel *Phys. Status Solidi* a **220** 2200776
[144] Sun M, Zhang Y, Gao X and Palacios T 2017 High-performance GaN vertical fin power transistors on bulk GaN substrates *IEEE Electron Device Lett.* **38** 509–12
[145] Zhang Y *et al* 2019 Large-area 1.2-kV GaN vertical power FinFETs with a record switching figure of merit *IEEE Electron Device Lett.* **40** 75–78
[146] Xiao M, Gao X, Palacios T and Zhang Y 2019 Leakage and breakdown mechanisms of GaN vertical power FinFETs *Appl. Phys. Lett.* **114** 163503
[147] Liu J *et al* 2020 1.2 kV vertical GaN Fin JFETs with robust avalanche and fast switching capabilities *2020 IEEE Int. Electron Devices Meeting (IEDM)* pp 23.2.1–23.2.4
[148] Zhang R, Liu J, Li Q, Pidaparthi S, Edwards A, Drowley C and Zhang Y 2022 Robust through-Fin avalanche in vertical GaN Fin-JFET with soft failure mode *IEEE Electron Device Lett.* **43** 366–9
[149] Mishra U K, Shen L, Kazior T E and Wu Y-F 2008 GaN-based RF power devices and amplifiers *Proc. IEEE* **96** 287–305
[150] Nakamura S, Masayuki Senoh M S and Takashi Mukai T M 1993 P-GaN/N-InGaN/N-GaN double-heterostructure blue-light-emitting diodes *Jpn. J. Appl. Phys.* **32** L8
[151] Sheppard S T *et al* 2000 Technology development for GaN/AlGaN HEMT hybrid and MMIC amplifiers on semi-insulating SiC substrates *Proc. 2000 IEEE/ Cornell Conf. on High Performance Devices (Cat. No.00CH37122)* pp 232–6

[152] Chini A, Buttari D, Coffie R, Heikman S, Keller S and Mishra U K 2004 12 W/mm power density AlGaN/GaN HEMTs on sapphire substrate *Electron. Lett.* **40** 73–74
[153] Runton D W, Trabert B, Shealy J B and Vetury R 2013 History of GaN: high-power RF gallium nitride (GaN) from infancy to manufacturable process and beyond *IEEE Microw. Mag.* **14** 82–93
[154] Khan M A, Shur M S, Chen Q C and Kuznia J N 1994 Current/voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias *Electron. Lett.* **30** 2175–6
[155] Binari S C, Ikossi K, Roussos J A, Kruppa W, Park D, Dietrich H B, Koleske D D, Wickenden A E and Henry R L 2001 Trapping effects and microwave power performance in AlGaN/GaN HEMTs *IEEE Trans. Electron Devices* **48** 465–71
[156] Green B M, Chu K K, Chumbes E M, Smart J A, Shealy J R and Eastman L F 2000 The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs *IEEE Electron Device Lett.* **21** 268–70
[157] Shealy J R *et al* 2002 An AlGaN/GaN high-electron-mobility transistor with an AlN sub-buffer layer *J. Phys.* **14** 3499
[158] Ando Y, Okamoto Y, Miyamoto H, Nakayama T, Inoue T and Kuzuhara M 2003 10-W/mm AlGaN-GaN HFET with a field modulating plate *IEEE Electron Device Lett.* **24** 289–91
[159] Wu Y-F, Saxler A, Moore M, Smith R P, Sheppard S, Chavarkar P M, Wisleder T, Mishra U K and Parikh P 2004 30-W/mm GaN HEMTs by field plate optimization *IEEE Electron Device Lett.* **25** 117–9
[160] Wu Y-F, Moore M, Saxler A, Wisleder T and Parikh P 2006 40-W/mm double field-plated GaN HEMTs *2006 64th Device Research Conf.* pp 151–2
[161] Coffie R, Buttari D, Heikman S, Keller S, Chini A, Shen L and Mishra U K 2002 p-capped GaN-AlGaN-GaN high-electron mobility transistors (HEMTs) *IEEE Electron Device Lett.* **23** 588–90
[162] Jimnez A *et al* 2002 Effect of p-doped overlayer thickness on RF-dispersion in GaN junction FETs *IEEE Electron Device Lett.* **23** 306–8
[163] Shen L, Coffie R, Buttari D, Heikman S, Chakraborty A, Chini A, Keller S, DenBaars S P and Mishra U K 2004 High-power polarization-engineered GaN/AlGaN/GaN HEMTs without surface passivation *IEEE Electron Device Lett.* **25** 7–9
[164] Shen L, Palacios T, Poblenz C, Corrion A, Chakraborty A, Fichtenbaum N, Keller S, Denbaars S P, Speck J S and Mishra U K 2006 Unpassivated high power deeply recessed GaN HEMTs with fluorine-plasma surface treatment *IEEE Electron Device Lett.* **27** 214–6
[165] Liu W, Romanczyk B, Guidry M, Hatui N, Wurm C, Li W, Shrestha P, Zheng X, Keller S and Mishra U K 2021 6.2 W/Mm and record 33.8% PAE at 94 GHz from N-polar GaN deep recess MIS-HEMTs with ALD Ru gates *IEEE Microw. Wirel. Compon. Lett.* **31** 748–51
[166] Palacios T, Chakraborty A, Rajan S, Poblenz C, Keller S, DenBaars S P, Speck J S and Mishra U K 2005 High-power AlGaN/GaN HEMTs for Ka-band applications *IEEE Electron Device Lett.* **26** 781–3
[167] Zhang Z *et al* 2017 AlGaN/GaN MIS-HEMTs of very-low V_{th} hysteresis and current collapse with in-situ pre-deposition plasma nitridation and LPCVD-Si_3N_4 gate insulator *IEEE Electron Device Lett.* **38** 236–9
[168] Van Hove M, Boulay S, Bahl S R, Stoffels S, Kang X, Wellekens D, Geens K, Delabie A and Decoutere S 2012 CMOS process-compatible high-power low-leakage AlGaN/GaN MISHEMT on silicon *IEEE Electron Device Lett.* **33** 667–9
[169] Zhang S *et al* 2021 7.05 W/mm power density millimeter-wave GaN MIS-HEMT with plasma enhanced atomic layer deposition SiN dielectric layer *IEEE Electron Device Lett.* **42** 1436–9
[170] Huang S *et al* 2014 High-temperature low-damage gate recess technique and ozone-assisted ALD-grown Al_2O_3 gate dielectric for high-performance normally-off GaN MIS-HEMTs *2014 IEEE Int. Electron Devices Meeting* pp 17.4.1–4
[171] Zhang S *et al* 2021 Suppression of gate leakage current in Ka-band AlGaN/GaN HEMT WITH 5-nm SiN gate dielectric grown by plasma-enhanced ALD *IEEE Trans. Electron Devices* **68** 49–52
[172] Hao Y, Ma X, Mi M and Yang L-A 2021 Research on GaN-based RF devices: high-frequency gate structure design, submicrometer-length gate fabrication, suppressed SCE, low parasitic resistance, minimized current collapse, and lower gate leakage *IEEE Microw. Mag.* **22** 34–48
[173] Higashiwaki M, Mimura T and Matsui T 2008 AlGaN/GaN heterostructure field-effect transistors on 4H-SiC substrates with current-gain cutoff frequency of 190 GHz *Appl. Phys. Express* **1** 021103
[174] Yue Y *et al* 2012 InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz *IEEE Electron Device Lett.* **33** 988–90
[175] Shinohara K *et al* 2013 Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications *IEEE Trans. Electron Devices* **60** 2982–96
[176] Brown D F *et al* 2011 W-band power performance of AlGaN/GaN DHFETs with regrown n+ GaN ohmic contacts by MBE *2011 Int. Electron Devices Meeting* pp 19.3.1–4
[177] Niida Y *et al* 2016 3.6 W/mm high power density W-band InAlGaN/GaN HEMT MMIC power amplifier *2016 IEEE Topical Conf. on Power Amplifiers for Wireless and Radio Applications (PAWR)* pp 24–26
[178] Romanczyk B, Wienecke S, Guidry M, Li H, Ahmadi E, Zheng X, Keller S and Mishra U K 2018 Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave N-polar GaN MISHEMTs *IEEE Trans. Electron Devices* **65** 45–50
[179] Li W *et al* 2023 Record RF power performance at 94 GHz from millimeter-wave N-polar GaN-on-sapphire deep-recess HEMTs *IEEE Trans. Electron Devices* **70** 2075–80
[180] Ji D, Ercan B, Zhuang J, Gu L, Rivas-Davila J and Chowdhury S 2020 Demonstration of GaN impact ionization avalanche transit-time (IMPATT) diode *2020 Device Research Conf. (DRC)* pp 1–2
[181] Kawasaki S, Ando Y, Deki M, Watanabe H, Tanaka A, Nitta S, Honda Y, Arai M and Amano H 2021 Experimental demonstration of GaN IMPATT diode at X-band *Appl. Phys. Express* **14** 046501
[182] Kawasaki S, Kumabe T, Ando Y, Deki M, Watanabe H, Tanaka A, Honda Y, Arai M and Amano H 2023 Junction diameter dependence of oscillation frequency of GaN IMPATT diode up to 21 GHz *IEEE Electron Device Lett.* **44** 1328–31
[183] Nishikawa A, Kumakura K, Akasaka T and Makimoto T 2006 Critical electric fields of AlGaN in AlGaN-based vertical conducting diodes on n-SiC substrates *Superlattices Microstruct.* **40** 332–7
[184] Zhang A P, Dang G, Ren F, Han J, Polyakov A Y, Smirnov N B, Govorkov A V, Redwing J M, Cao X A and Pearton S J 2000 Al composition dependence of breakdown voltage in $Al_xGa_{1-x}N$ Schottky rectifiers *Appl. Phys. Lett.* **76** 1767–9
[185] Kaplar R J, Allerman A A, Armstrong A M, Crawford M H, Dickerson J R, Fischer A J, Baca A G and Douglas E A 2017 Review—ultra-wide-bandgap AlGaN power electronic devices *ECS J. Solid State Sci. Technol.* **6** Q3061
[186] Cheng Z *et al* 2020 Experimental observation of high intrinsic thermal conductivity of AlN *Phys. Rev. Mater.* **4** 044602
[187] Nanjo T, Takeuchi M, Suita M, Abe Y, Oishi T, Tokuda Y and Aoyagi Y 2007 First operation of AlGaN channel high electron mobility transistors *Appl. Phys. Express* **1** 011101

[188] Nanjo T, Imai A, Suzuki Y, Abe Y, Oishi T, Suita M, Yagyu E and Tokuda Y 2013 AlGaN channel HEMT with extremely high breakdown voltage *IEEE Trans. Electron Devices* **60** 1046–53
[189] Noshin M, Soman R and Chowdhury S 2023 Demonstration of N-polar all-AlGaN high electron mobility transistors with 375 mA/mm drive current *IEEE Electron Device Lett.* **44** 1072–5
[190] Taniyasu Y, Kasu M and Makimoto T 2006 Increased electron mobility in n-type Si-doped AlN by reducing dislocation density *Appl. Phys. Lett.* **89** 182112
[191] Werdecker W and Aldinger F 1984 Aluminum nitride-an alternative ceramic substrate for high power applications in microcircuits *IEEE Trans. Compon. Hybrids Manuf. Technol.* **7** 399–404
[192] Nomura T, Okumura K, Miyake H, Hiramatsu K, Eryu O and Yamada Y 2012 AlN homoepitaxial growth on sublimation-AlN substrate by low-pressure HVPE *J. Cryst. Growth* **350** 69–71
[193] Dalmau R *et al* 2011 Growth and characterization of AlN and AlGaN epitaxial films on AlN single crystal substrates *J. Electrochem. Soc.* **158** H530
[194] Makarov Y N *et al* 2008 Experimental and theoretical analysis of sublimation growth of AlN bulk crystals *J. Cryst. Growth* **310** 881–6
[195] Volkova A A, Ivantsov V A and Leung L 2011 Hydride vapor phase epitaxy of high structural perfection thick AlN layers on off-axis 6H-SiC *J. Cryst. Growth* **314** 113–8
[196] Kumagai Y, Goto K, Nagashima T, Yamamoto R, Boćkowski M and Kotani J 2022 Influence of growth rate on homoepitaxial growth of AlN at 1450 °C by hydride vapor phase epitaxy *Appl. Phys. Express* **15** 115501
[197] Chemekova T Y *et al* 2008 Sublimation growth of 2 inch diameter bulk AlN crystals *Phys. Status Solidi* c **5** 1612–4
[198] Nagai I *et al* 2010 AlN bulk single crystal growth on SiC and AlN substrates by sublimation method *Conf. Proc.—Int. Conf. on Indium Phosphide and Related Materials* pp 1–4
[199] Hartmann C, Dittmar A, Wollweber J and Bickermann M 2014 Bulk AlN growth by physical vapour transport *Semicond. Sci. Technol.* **29** 084002
[200] Hartmann C, Wollweber J, Dittmar A, Irmscher K, Kwasniewski A, Langhans F, Neugut T and Bickermann M 2013 Preparation of bulk AlN seeds by spontaneous nucleation of freestanding crystals *Jpn. J. Appl. Phys.* **52** 08JA06
[201] Epelbaum B M, Nagata S, Bickermann M, Heimann P and Winnacker A 2007 Development of natural habit of large free-nucleated AlN single crystals *Phys. Status Solidi* b **244** 1780–3
[202] Hu W, Guo L, Guo Y and Wang W 2020 Growing AlN crystals on SiC seeds: effects of growth temperature and seed orientation *J. Cryst. Growth* **541** 125654
[203] Chen W-H *et al* 2019 The physical vapor transport method for bulk AlN crystal growth *Molecules* **24** 1562
[204] Hagedorn S, Knauer A, Brunner F, Mogilatenko A, Zeimer U and Weyers M 2017 High-quality AlN grown on a thermally decomposed sapphire surface *J. Cryst. Growth* **479** 16–21
[205] Demir I, Li H, Robin Y, McClintock R, Elagoz S and Razeghi M 2018 Sandwich method to grow high quality AlN by MOCVD *J. Phys. D: Appl. Phys.* **51** 085104
[206] Long H *et al* 2019 High quality 10.6 μm AlN grown on pyramidal patterned sapphire substrate by MOCVD *Appl. Phys. Lett.* **114** 042101
[207] Mino T, Hirayama H, Takano T, Tsubaki K and Sugiyama M 2012 Characteristics of epitaxial lateral overgrowth AlN templates on (111)Si substrates for AlGaN deep-UV LEDs fabricated on different direction stripe patterns *Phys. Status Solidi* c **9** 802–5
[208] Mansurov V, Nikitin A Y, Galitsyn Y G, Svitasheva S N, Zhuravlev K S, Osvath Z, Dobos L, Horvath Z E and Pecz B 2007 AlN growth on sapphire substrate by ammonia MBE *J. Cryst. Growth* **300** 145–50
[209] Yin X, Zhang Q and Zhao S 2021 Molecular beam epitaxial growth of AlN thin films on Si through exploiting low Al adatom migration and the nitrogen-rich environment on a nanowire template *Cryst. Growth Des.* **21** 3645–9
[210] Bellucci A *et al* 2021 Aluminum (Oxy)nitride thin films grown by fs-PLD as electron emitters for thermionic applications *AIP Conf. Proc.* **2416** 020004
[211] Wang W, Yang W, Liu Z, Wang H, Wen L and Li G 2015 Interfacial reaction control and its mechanism of AlN epitaxial films grown on Si(111) substrates by pulsed laser deposition *Sci. Rep.* **5** 11480
[212] Yang H, Wang W, Liu Z, Yang W and Li G 2014 Epitaxial growth mechanism of pulsed laser deposited AlN films on Si (111) substrates *CrystEngComm* **16** 3148–54
[213] Vashaei Z, Aikawa T, Ohtsuka M, Kobatake H, Fukuyama H, Ikeda S and Takada K 2009 Influence of sputtering parameters on the crystallinity and crystal orientation of AlN layers deposited by RF sputtering using the AlN target *J. Cryst. Growth* **311** 459–62
[214] Nishikawa A, Kumakura K and Makimoto T 2007 High critical electric field exceeding 8 MV/cm measured using an AlGaN p–i–n vertical conducting diode on n-SiC substrate *Jpn. J. Appl. Phys.* **46** 2316
[215] Nanjo T, Takeuchi M, Suita M, Oishi T, Abe Y, Tokuda Y and Aoyagi Y 2008 Remarkable breakdown voltage enhancement in AlGaN channel high electron mobility transistors *Appl. Phys. Lett.* **92** 263502
[216] Baca A G, Armstrong A M, Allerman A A, Douglas E A, Sanchez C A, King M P, Coltrin M E, Fortune T R and Kaplar R J 2016 An AlN/$Al_{0.85}Ga_{0.15}N$ high electron mobility transistor *Appl. Phys. Lett.* **109** 3
[217] Xue H, Hussain K, Razzak T, Gaevski M, Sohel S H, Mollah S, Talesara V, Khan A, Rajan S and Lu W 2020 $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ micro-channel heterojunction field effect transistors with current density over 900 mA/mm *IEEE Electron Device Lett.* **41** 677–80
[218] Yoshida S, Misawa S and Gonda S 1982 Properties of $Al_xGa_{1-x}N$ films prepared by reactive molecular beam epitaxy *J. Appl. Phys.* **53** 6844–8
[219] Khan M A, Skogman R A, Schulze R G and Gershenzon M 1983 Properties and ion implantation of $Al_xGa_{1-x}N$ epitaxial single crystal films prepared by low pressure metalorganic chemical vapor deposition *Appl. Phys. Lett.* **43** 492–4
[220] Han J, Waldrip K E, Lee S R, Figiel J J, Hearne S J, Petersen G A and Myers S M 2001 Control and elimination of cracking of AlGaN using low-temperature AlGaN interlayers *Appl. Phys. Lett.* **78** 67–69
[221] Hatui N, Collins H, Kayede E, Pasayat S S, Li W, Keller S and Mishra U K 2022 Fully relaxed, crack-free AlGaN with upto 50% Al composition grown on porous GaN pseudo-substrate *Crystals* **12** 989
[222] Armstrong A M and Allerman A A 2016 Polarization-induced electrical conductivity in ultra-wide band gap AlGaN alloys *Appl. Phys. Lett.* **109** 222101
[223] Tang L, Tang B, Zhang H and Yuan Y 2020 Review—review of research on AlGaN MOCVD growth *ECS J. Solid State Sci. Technol.* **9** 024009
[224] Tasi C-T, Wang W-K, Ou S-L, Huang S-Y, Horng R-H and Wuu D-S 2018 Structural and stress properties of AlGaN epilayers grown on AlN-nanopatterned sapphire templates by hydride vapor phase epitaxy *Nanomaterials* **8** 704

[225] Fujikura H, Konno T and Kimura T 2022 Hydride vapor phase epitaxial growth of AlGaN *Appl. Phys. Express* **15** 085504
[226] Lee K, Page R, Protasenko V, Schowalter L J, Toita M, Xing H G and Jena D 2021 MBE growth and donor doping of coherent ultrawide bandgap AlGaN alloy layers on single-crystal AlN substrates *Appl. Phys. Lett.* **118** 092101
[227] Martens M *et al* 2016 Low absorption loss p-AlGaN superlattice cladding layer for current-injection deep ultraviolet laser diodes *Appl. Phys. Lett.* **108** 151108
[228] Bayram C, Pau J L, McClintock R and Razeghi M 2008 Delta-doping optimization for high quality p-type GaN *J. Appl. Phys.* **104** 083512
[229] Li J, Yang W, Li S, Chen H, Liu D and Kang J 2009 Enhancement of p-type conductivity by modifying the internal electric field in Mg- and Si-δ-codoped $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ superlattices *Appl. Phys. Lett.* **95** 151113
[230] Qiu X, Chen Y, Han E, Lv Z, Song Z and Jiang H 2020 High doping efficiency in p-type Al-rich AlGaN by modifying the Mg doping planes *Mater. Adv.* **1** 77–85
[231] Sarkar B *et al* 2018 N- and P-type doping in Al-rich AlGaN and AlN *ECS Trans.* **86** 25
[232] Taniyasu Y, Kasu M and Makimoto T 2006 An aluminium nitride light-emitting diode with a wavelength of 210 nanometres *Nature* **441** 325–8
[233] Hiroki M, Taniyasu Y and Kumakura K 2022 High-temperature performance of AlN MESFETs with epitaxially grown n-type AlN channel layers *IEEE Electron Device Lett.* **43** 350–3
[234] Harris J S, Baker J N, Gaddy B E, Bryan I, Bryan Z, Mirrielees K J, Reddy P, Collazo R, Sitar Z and Irving D L 2018 On compensation in Si-doped AlN *Appl. Phys. Lett.* **112** 152101
[235] Ahmad H, Engel Z, Matthews C M, Lee S and Doolittle W A 2022 Realization of homojunction PN AlN diodes *J. Appl. Phys.* **131** 175701
[236] Nishikawa A, Kumakura K, Akasaka T and Makimoto T 2006 High critical electric field of $Al_xGa_{1-x}N$ p-i-n vertical conducting diodes on n-SiC substrates *Appl. Phys. Lett.* **88** 173508
[237] Allerman A A, Armstrong A M, Fischer A J, Dickerson J R, Crawford M H, King M P, Moseley M W, Wierer J J and Kaplar R J 2016 $Al_{0.3}Ga_{0.7}N$ PN diode with breakdown voltage >1600 V *Electron. Lett.* **52** 1319–21
[238] Yoshizumi Y, Hashimoto S, Tanabe T and Kiyama M 2007 High-breakdown-voltage pn-junction diodes on GaN substrates *J. Cryst. Growth* **298** 875–8
[239] Tokuda H, Hatano M, Yafune N, Hashimoto S, Akita K, Yamamoto Y and Kuzuhara M 2010 High Al composition AlGaN-channel high-electron-mobility transistor on AlN substrate *Appl. Phys. Express* **3** 121003
[240] Yafune N, Hashimoto S, Akita K, Yamamoto Y, Tokuda H and Kuzuhara M 2014 AlN/AlGaN HEMTs on AlN substrate for stable high-temperature operation *Electron. Lett.* **50** 211–2
[241] Noshin M, Wen X, Soman R, Xu X and Chowdhury S 2023 Growth and mobility characterization of N-polar AlGaN channel high electron mobility transistors *Appl. Phys. Lett.* **123** 062103
[242] Raman A, Dasgupta S, Rajan S, Speck J S and Mishra U K 2008 AlGaN channel high electron mobility transistors: device performance and power-switching figure of merit *Jpn. J. Appl. Phys.* **47** 3359
[243] Bajaj S, Yang Z, Akyol F, Park P S, Zhang Y, Price A L, Krishnamoorthy S, Meyer D J and Rajan S 2017 Graded AlGaN channel transistors for improved current and power gain linearity *IEEE Trans. Electron Devices* **64** 3114–9
[244] Sohel S H *et al* 2018 X-band power and linearity performance of compositionally graded AlGaN channel transistors *IEEE Electron Device Lett.* **39** 1884–7
[245] Xue H, Hussain K, Talesara V, Razzak T, Gaevski M, Mollah S, Rajan S, Khan A and Lu W 2021 High-current-density enhancement-mode ultrawide-bandgap AlGaN channel metal–insulator–semiconductor heterojunction field-effect transistors with a threshold voltage of 5 V *Phys. Status Solidi* **15** 2000576
[246] Razzak T *et al* 2018 RF operation in graded $Al_xGa_{1-x}N$ (x = 0.65 to 0.82) channel transistors *Electron. Lett.* **54** 1351–3
[247] Xue H, Lee C H, Hussian K, Razzak T, Abdullah M, Xia Z, Sohel S H, Khan A, Rajan S and Lu W 2019 $Al_{0.75}Ga_{0.25}N/Al_{0.6}Ga_{0.4}N$ heterojunction field effect transistor with f_T of 40 GHz *Appl. Phys. Express* **12** 066502
[248] Baca A G *et al* 2019 RF performance of $Al_{0.85}Ga_{0.15}N/Al_{0.70}Ga_{0.30}N$ high electron mobility transistors with 80 nm gates *IEEE Electron Device Lett.* **40** 17–20
[249] Kinoshita T *et al* 2015 Fabrication of vertical Schottky barrier diodes on n-type freestanding AlN substrates grown by hydride vapor phase epitaxy *Appl. Phys. Express* **8** 061003
[250] Maeda T, Page R, Nomoto K, Toita M, Xing H G and Jena D 2022 AlN quasi–vertical Schottky barrier diode on AlN bulk substrate using $Al_{0.9}Ga_{0.1}N$ current spreading layer *Appl. Phys. Express* **15** 061007
[251] Fu H, Baranowski I, Huang X, Chen H, Lu Z, Montes J, Zhang X and Zhao Y 2017 Demonstration of AlN Schottky barrier diodes with blocking voltage over 1 kV *IEEE Electron Device Lett.* **38** 1286–9
[252] Yamada H, Chayahara A, Mokuno Y, Kato Y and Shikata S 2014 A 2-in. mosaic wafer made of a single-crystal diamond *Appl. Phys. Lett.* **104** 102110
[253] Ohmagari S, Yamada H, Tsubouchi N, Umezawa H, Chayahara A, Tanaka S and Mokuno Y 2018 Large reduction of threading dislocations in diamond by hot-filament chemical vapor deposition accompanying W incorporations *Appl. Phys. Lett.* **113** 032108
[254] Ohmagari S, Yamada H, Tsubouchi N, Umezawa H, Chayahara A, Seki A, Kawaii F, Saitoh H and Mokuno Y 2019 Schottky barrier diodes fabricated on diamond mosaic wafers: dislocation reduction to mitigate the effect of coalescence boundaries *Appl. Phys. Lett.* **114** 082104
[255] Isberg J, Hammersberg J, Johansson E, Wikström T, Twitchen D J, Whitehead A J, Coe S E and Scarsbrook G A 2002 High carrier mobility in single-crystal plasma-deposited diamond *Science* **297** 1670–2
[256] Akimoto I, Handa Y, Fukai K and Naka N 2014 High carrier mobility in ultrapure diamond measured by time-resolved cyclotron resonance *Appl. Phys. Lett.* **105** 032102
[257] Pernot J, Volpe P N, Omnès F, Muret P, Mortet V, Haenen K and Teraji T 2010 Hall hole mobility in boron-doped homoepitaxial diamond *Phys. Rev.* B **81** 205203
[258] Pernot J and Koizumi S 2008 Electron mobility in phosphorous doped {111} homoepitaxial diamond *Appl. Phys. Lett.* **93** 052105
[259] Gabrysch M, Majdi S, Twitchen D J and Isberg J 2011 Electron and hole drift velocity in chemical vapor deposition diamond *J. Appl. Phys.* **109** 063719
[260] Reggiani L, Bosi S, Canali C, Nava F and Kozlov S F 1981 Hole-drift velocity in natural diamond *Phys. Rev.* B **23** 3050–7
[261] Pomorski M, Berdermann E, Caragheorgheopol A, Ciobanu M, Kiš M, Martemiyanov A, Nebel C and Moritz P 2006 Development of single-crystal CVD-diamond detectors for spectroscopy and timing *Phys. Status Solidi* a **203** 3152–60
[262] Anthony T R, Banholzer W F, Fleischer J F, Wei L, Kuo P K, Thomas R L and Pryor R W 1990 Thermal diffusivity of isotopically enriched ^{12}C diamond *Phys. Rev.* B **42** 1104–11

[263] da Silva Neto J V, Fraga M A and Trava-Airoldi V J 2019 Development, properties, and applications of CVD diamond-based heat sinks *Some Aspects of Diamonds in Scientific Research and High Technology* ed E Lipatov (IntechOpen) ch 4 (https://doi.org/10.5772/intechopen.85349)
[264] Nad S, Gu Y and Asmussen J 2015 Growth strategies for large and high quality single crystal diamond substrates *Diam. Relat. Mater.* **60** 26–34
[265] Cao W, Ma Z, Gao D, Fu Q and Zhao H 2022 Homoepitaxial lateral growth of single-crystal diamond with eliminating PCD rim and enlarging surface area *Vacuum* **197** 110820
[266] Schreck M, Gsell S, Brescia R and Fischer M 2017 Ion bombardment induced buried lateral growth: the key mechanism for the synthesis of single crystal diamond wafers *Sci. Rep.* **7** 44462
[267] Lagrange J-P, Deneuville A and Gheeraert E 1998 Activation energy in low compensated homoepitaxial boron-doped diamond films *Diam. Relat. Mater.* **7** 1390–3
[268] Koizumi S, Kamo M, Sato Y, Ozaki H and Inuzuka T 1997 Growth and characterization of phosphorous doped {111} homoepitaxial diamond thin films *Appl. Phys. Lett.* **71** 1065–7
[269] Koizumi S, Teraji T and Kanda H 2000 Phosphorus-doped chemical vapor deposition of diamond *Diam. Relat. Mater.* **9** 935–40
[270] Grotjohn T A, Tran D T, Yaran M K, Demlow S N and Schuelke T 2014 Heavy phosphorus doping by epitaxial growth on the (111) diamond surface *Diam. Relat. Mater.* **44** 129–33
[271] Kato H, Takeuchi D, Tokuda N, Umezawa H, Okushi H and Yamasaki S 2009 Characterization of specific contact resistance on heavily phosphorus-doped diamond films *Diam. Relat. Mater.* **18** 782–5
[272] Kato H, Yamasaki S and Okushi H 2005 n-type doping of (001)-oriented single-crystalline diamond by phosphorus *Appl. Phys. Lett.* **86** 222111
[273] Pinault-Thaury M A, Temgoua S, Gillet R, Bensalah H, Stenger I, Jomard F, Issaoui R and Barjon J 2019 Phosphorus-doped (113) CVD diamond: a breakthrough towards bipolar diamond devices *Appl. Phys. Lett.* **114** 112106
[274] Peterson R, Malakoutian M, Xu X, Chapin C, Chowdhury S and Senesky D G 2020 Analysis of mobility-limiting mechanisms of the two-dimensional hole gas on hydrogen-terminated diamond *Phys. Rev.* B **102** 075303
[275] Kubovic M, Kasu M, Kageshima H and Maeda F 2010 Electronic and surface properties of H-terminated diamond surface affected by NO_2 gas *Diam. Relat. Mater.* **19** 889–93
[276] Daicho A, Saito T, Kurihara S, Hiraiwa A and Kawarada H 2014 High-reliability passivation of hydrogen-terminated diamond surface by atomic layer deposition of Al_2O_3 *J. Appl. Phys.* **115** 223711
[277] Tordjman M, Saguy C, Bolker A and Kalish R 2014 Superior surface transfer doping of diamond with MoO_3 *Adv. Mater. Interfaces* **1** 1300155
[278] Xing K, Zhang S, Tsai A, Xiao H, Creedon D L, Yianni S A, McCallum J C, Pakes C I and Qi D-C 2020 High-electron-affinity oxide V_2O_5 enhances surface transfer doping on hydrogen-terminated diamond *Diam. Relat. Mater.* **108** 107865
[279] Crawford K G, Cao L, Qi D, Tallaire A, Limiti E, Verona C, Wee A T S and Moran D A J 2016 Enhanced surface transfer doping of diamond by V_2O_5 with improved thermal stability *Appl. Phys. Lett.* **108** 042103
[280] Donato N, Rouger N, Pernot J, Longobardi G and Udrea F 2020 Diamond power devices: state of the art, modelling, figures of merit and future perspective *J. Phys. D: Appl. Phys.* **53** 093001
[281] Umezawa H, Ikeda K, Kumaresan R, Tatsumi N and Shikata S I 2009 Increase in reverse operation limit by barrier height control of diamond Schottky barrier diode *IEEE Electron Device Lett.* **30** 960–2
[282] Doneddu D, Guy O J, Twitchen D, Tajani A, Schwitters M and Igi P 2006 Schottky contacts on single-crystal CVD diamond
[283] Ueda K, Kawamoto K, Soumiya T and Asano H 2013 High-temperature characteristics of Ag and Ni/diamond Schottky diodes *Diam. Relat. Mater.* **38** 41–44
[284] Teraji T, Garino Y, Koide Y and Ito T 2009 Low-leakage p-type diamond Schottky diodes prepared using vacuum ultraviolet light/ozone treatment *J. Appl. Phys.* **105** 126109
[285] Volpe P-N *et al* 2010 Extreme dielectric strength in boron doped homoepitaxial diamond *Appl. Phys. Lett.* **97** 223501
[286] Teraji T, Fiori A, Kiritani N, Tanimoto S, Gheeraert E and Koide Y 2017 Mechanism of reverse current increase of vertical-type diamond Schottky diodes *J. Appl. Phys.* **122** 135304
[287] Traoré A, Muret P, Fiori A, Eon D, Gheeraert E and Pernot J 2014 Zr/oxidized diamond interface for high power Schottky diodes *Appl. Phys. Lett.* **104** 052105
[288] Vescan A, Daumiller I, Gluche P, Ebert W and Kohn E 1997 Very high temperature operation of diamond Schottky diode **18** 556–8
[289] Baumann P K and Nemanich R J 1998 Electron affinity and Schottky barrier height of metal-diamond (100), (111), and (110) interfaces *J. Appl. Phys.* **83** 2072–82
[290] Sakai T, Song K-S, Kanazawa H, Nakamura Y, Umezawa H, Tachiki M and Kawarada H 2003 Ozone-treated channel diamond field-effect transistors *Diam. Relat. Mater.* **12** 1971–5
[291] Hazdra P, Laposa A, Šobáň Z, Taylor A, Lambert N, Povolný V, Kroutil J, Gedeonová Z, Hubík P and Mortet V 2022 Pseudo-vertical Mo/Au Schottky diodes on {113} oriented boron doped homoepitaxial diamond layers *Diam. Relat. Mater.* **126** 109088
[292] Makino T *et al* 2009 Diamond Schottky-pn diode with high forward current density and fast switching operation *Appl. Phys. Lett.* **94** 262101
[293] Makino T, Kato H, Tokuda N, Ogura M, Takeuchi D, Oyama K, Tanimoto S, Okushi H and Yamasaki S 2010 Diamond Schottky-pn diode without trade-off relationship between on-resistance and blocking voltage *Phys. Status Solidi* a **207** 2105–9
[294] Dutta M, Koeck F A M, Li W, Nemanich R J and Chowdhury S 2017 High voltage diodes in diamond using (100)- and (111)-substrates *IEEE Electron Device Lett.* **38** 600–3
[295] Surdi H, Koeck F A M, Ahmad M F, Thornton T J, Nemanich R J and Goodnick S M 2022 Demonstration and analysis of ultrahigh forward current density diamond diodes *IEEE Trans. Electron Devices* **69** 254–61
[296] Malakoutian M, Benipal M, Koeck F A, Nemanich R J and Chowdhury S 2020 Schottky barrier height analysis of diamond SPIND using high temperature operation up to 873 K *IEEE J. Electron Devices Soc.* **8** 614–8
[297] Suzuki M, Sakai T, Makino T, Kato H, Takeuchi D, Ogura M, Okushi H and Yamasaki S 2013 Electrical characterization of diamond PiN diodes for high voltage applications: electrical characterization of diamond PiN diodes *Phys. Status Solidi* a **210** 2035–9
[298] Umezawa H, Saito T, Tokuda N, Ogura M, Ri S-G, Yoshikawa H and Shikata S-I 2007 Leakage current analysis of diamond Schottky barrier diode *Appl. Phys. Lett.* **90** 073506
[299] Saremi M, Hathwar R, Dutta M, Koeck F A M, Nemanich R J, Chowdhury S and Goodnick S M 2017 Analysis of the reverse I-V characteristics of diamond-based PIN diodes *Appl. Phys. Lett.* **111** 043507

[300] Zhao D, Hu C, Liu Z, Wang H X, Wang W and Zhang J 2017 Diamond MIP structure Schottky diode with different drift layer thickness *Diam. Relat. Mater.* **73** 15–18
[301] Ikeda K, Umezawa H, Tatsumi N, Ramanujam K and Shikata S 2009 Fabrication of a field plate structure for diamond Schottky barrier diodes *Diam. Relat. Mater.* **18** 292–5
[302] Umezawa H, Nagase M, Kato Y and Shikata S I 2012 High temperature application of diamond power device *Diam. Relat. Mater.* **24** 201–5
[303] Umezawa H, Matsumoto T and Shikata S-I 2014 Diamond metal–semiconductor field-effect transistor with breakdown voltage over 1.5 kV *IEEE Electron Device Lett.* **35** 1112–4
[304] Pham T T, Rouger N, Masante C, Chicot G, Udrea F, Eon D, Gheeraert E and Pernot J 2017 Deep depletion concept for diamond MOSFET *Appl. Phys. Lett.* **111** 173503
[305] Masante C, Rouger N and Pernot J 2021 Recent progress in deep-depletion diamond metal–oxide–semiconductor field-effect transistors *J. Appl. Phys.* **54** 233002
[306] Matsumoto T, Kato H, Oyama K, Makino T, Ogura M, Takeuchi D, Inokuma T, Tokuda N and Yamasaki S 2016 Inversion channel diamond metal-oxide-semiconductor field-effect transistor with normally off characteristics *Sci. Rep.* **6** 31585
[307] Matsumoto T, Kato H, Makino T, Ogura M, Takeuchi D, Yamasaki S, Inokuma T and Tokuda N 2019 Inversion channel mobility and interface state density of diamond MOSFET using N-type body with various phosphorus concentrations *Appl. Phys. Lett.* **114** 242101
[308] Matsumoto T, Yamakawa T, Kato H, Makino T, Ogura M, Zhang X, Inokuma T, Yamasaki S and Tokuda N 2021 Fabrication of inversion p-channel MOSFET with a nitrogen-doped diamond body *Appl. Phys. Lett.* **119** 242105
[309] Saha N C, Kim S W, Oishi T, Kawamata Y, Koyama K and Kasu M 2021 345-MW/cm^2 2608-V NO p-type doped diamond MOSFETs with an AlO passivation overlayer on heteroepitaxial diamond *IEEE Electron Device Lett.* **42** 903–6
[310] Kasu M and Oishi T 2014 Diamond RF power transistors: present status and challenges *European Microwave Week 2014: "Connecting the Future", EuMW 2014—Conference Proc.; EuMIC 2014: 9th European Microwave Integrated Circuits Conf.* (Institute of Electrical and Electronics Engineers Inc.) pp 146–8
[311] Wang W, Wang Y, Zhang M, Wang R, Chen G, Chang X, Lin F, Wen F, Jia K and Wang H-X 2020 An enhancement-mode hydrogen-terminated diamond field-effect transistor with lanthanum hexaboride gate material *IEEE Electron Device Lett.* **41** 585–8
[312] Kitabayashi Y *et al* 2017 Normally-off C–H diamond MOSFETs with partial C–O channel achieving 2-kV breakdown voltage *IEEE Electron Device Lett.* **38** 363–6
[313] Ren Z, Chen W, Zhang J, Zhang J, Zhang C, Yuan G, Su K, Lin Z and Hao Y 2019 High performance single crystalline diamond normally-off field effect transistors *IEEE J. Electron Devices Soc.* **7** 82–87
[314] Liu J W, Liao M Y, Imura M and Koide Y 2013 Normally-off HfO_2-gated diamond field effect transistors *Appl. Phys. Lett.* **103** 092905
[315] Zhu X *et al* 2022 −400 mA mm^{-1} drain current density normally-off polycrystalline diamond MOSFETs *IEEE Electron Device Lett.* **43** 789–92
[316] Wang Y-F *et al* 2019 Hydrogen-terminated diamond field-effect transistor with AlO_x dielectric layer formed by autoxidation *Sci. Rep.* **9** 5192
[317] Sasama Y, Komatsu K, Moriyama S, Imura M, Teraji T, Watanabe K, Taniguchi T, Uchihashi T and Takahide Y 2018 High-mobility diamond field effect transistor with a monocrystalline h-BN gate dielectric *APL Mater.* **6** 111105
[318] Sasama Y, Kageura T, Imura M, Watanabe K, Taniguchi T, Uchihashi T and Takahide Y 2021 High-mobility p-channel wide-bandgap transistors based on hydrogen-terminated diamond/hexagonal boron nitride heterostructures *Nat. Electron.* **5** 37–44
[319] Kasu M, Ueda K, Ye H, Yamauchi Y, Sasaki S and Makimoto T 2005 2 W/mm output power density at 1 GHz for diamond FETs *Electron. Lett.* **41** 1249
[320] Kasu M, Ueda K, Ye H, Yamauchi Y, Sasaki S and Makimoto T 2006 High RF output power for H-terminated diamond FETs *Diam. Relat. Mater.* **15** 783–6
[321] Ueda K, Kasu M, Yamauchi Y, Makimoto T, Schwitters M, Twitchen D J, Scarsbrook G A and Coe S E 2006 Diamond FET using high-quality polycrystalline diamond with f_T of 45 GHz and f_{max} of 120 GHz *IEEE Electron Device Lett.* **27** 570–2
[322] Hirama K, Takayanagi H, Yamauchi S, Jingu Y, Umezawa H and Kawarada H 2007 High-performance p-channel diamond MOSFETs with alumina gate insulator *2007 IEEE Int. Electron Devices Meeting*, (IEEE) pp 873–6
[323] Yu X, Zhou J, Qi C, Cao Z, Kong Y and Chen T 2018 A high frequency hydrogen-terminated diamond MISFET with f_T/f_{max} of 70/80 GHz *IEEE Electron Device Lett.* **39** 1373–6
[324] Imanishi S, Horikawa K, Oi N, Okubo S, Kageura T, Hiraiwa A and Kawarada H 2019 3.8 W/mm RF power density for ALD Al_2O_3-based two-dimensional hole gas diamond MOSFET operating at saturation velocity *IEEE Electron Device Lett.* **40** 279–82
[325] Yu C, Zhou C, Guo J, He Z, Ma M, Yu H, Song X, Bu A and Feng Z 2022 Hydrogen-terminated diamond MOSFETs on (0 0 1) single crystal diamond with state of the art high RF power density *Funct. Diam.* **2** 64–70
[326] Zhou X, Malakoutian M, Soman R, Bian Z, Martinez R P and Chowdhury S 2022 Impact of diamond passivation on f_T and f_{max} of mm-wave N-polar GaN HEMTs *IEEE Trans. Electron Devices* **69** 6650–5
[327] Malakoutian M *et al* 2021 Polycrystalline diamond growth on β-Ga_2O_3 for thermal management *Appl. Phys. Express* **14** 055502
[328] Choi S, Graham S, Chowdhury S, Heller E R, Tadjer M J, Moreno G and Narumanchi S 2021 A perspective on the electro-thermal co-design of ultra-wide bandgap lateral devices *Appl. Phys. Lett.* **119** 170501
[329] Pomeroy J W, Bernardoni M, Dumka D C, Fanning D M and Kuball M 2014 Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping *Appl. Phys. Lett.* **104** 083513
[330] Chao P-C, Chu K, Creamer C, Diaz J, Yurovchak T, Shur M, Kallaher R, McGray C, Via G D and Blevins J D 2015 Low-temperature bonded GaN-on-diamond HEMTs with 11 W/mm output power at 10 GHz *IEEE Trans. Electron Devices* **62** 3658–64
[331] Soman R *et al* 2022 Novel all-around diamond integration with GaN HEMTs demonstrating highly efficient device cooling *2022 Int. Electron Devices Meeting (IEDM)* (IEEE) pp 30.8.1–30.8.4
[332] Liu T, Kong Y, Wu L, Guo H, Zhou J, Kong C and Chen T 2017 3-inch GaN-on-diamond HEMTs with device-first transfer technology *IEEE Electron Device Lett.* **38** 1417–20
[333] Mu F, He R and Suga T 2018 Room temperature GaN-diamond bonding for high-power GaN-on-diamond devices *Scr. Mater.* **150** 148–51

[334] Cheng Z, Mu F, Yates L, Suga T and Graham S 2020 Interfacial thermal conductance across room-temperature-bonded GaN/diamond interfaces for GaN-on-diamond devices *ACS Appl. Mater. Interfaces* **12** 8376–84

[335] Matsumae T, Okita S, Fukumoto S, Hayase M, Kurashima Y and Takagi H 2023 Simple low-temperature GaN/diamond bonding process with an atomically thin intermediate layer *ACS Appl. Nano Mater.* **6** 14076–82

[336] Wei C and Chen C-H 2008 The effect of thermal and plastic mismatch on stress distribution in diamond like carbon film under different interlayer/substrate system *Diam. Relat. Mater.* **17** 1534–40

[337] Malakoutian L and Chowdhury S 2019 A study on the growth window of polycrystalline diamond on Si_3N_4-coated N-polar GaN *Crystals* **9** 498

[338] Malakoutian M, Field D E, Hines N J, Pasayat S, Graham S, Kuball M and Chowdhury S 2021 Record-low thermal boundary resistance between diamond and GaN-on-SiC for enabling radiofrequency device cooling *ACS Appl. Mater. Interfaces* **13** 60553–60

[339] Zhou Y *et al* 2017 Barrier-layer optimization for enhanced GaN-on-diamond device cooling *ACS Appl. Mater. Interfaces* **9** 34416–22

[340] Yates L *et al* 2018 Low thermal boundary resistance interfaces for GaN-on-diamond devices *ACS Appl. Mater. Interfaces* **10** 24302–9

[341] Malakoutian M, Zheng X, Woo K, Soman R, Kasperovich A, Pomeroy J, Kuball M and Chowdhury S 2022 Low thermal budget growth of near-isotropic diamond grains for heat spreading in semiconductor devices *Adv. Funct. Mater.* **32** 2208997

[342] Matsumae T, Kurashima Y, Umezawa H, Tanaka K, Ito T, Watanabe H and Takagi H 2020 Low-temperature direct bonding of β-Ga_2O_3 and diamond substrates under atmospheric conditions *Appl. Phys. Lett.* **116** 141602

[343] Mandal S, Arts K, Knoops H C M, Cuenca J A, Klemencic G M and Williams O A 2021 Surface zeta potential and diamond growth on gallium oxide single crystal *Carbon* **181** 79–86

[344] Nunnally W C and Hammond R B 1984 Optoelectronic switch for pulsed power *Picosecond Optoelectronic Devices* (Elsevier) pp 373–98

[345] Woo K, Malakoutian M, Reeves B A and Chowdhury S 2022 A study on sub-bandgap photoexcitation in nitrogen- and boron-doped diamond with interdigitated device structure *Appl. Phys. Lett.* **120** 112104

[346] Bharadwaj P K, Code R F, van Driel H M and Walentynowicz E 1983 High voltage optoelectronic switching in diamond *Appl. Phys. Lett.* **43** 207–9

[347] Feng S, Ho P-T and Goldhar J 1990 Photoconductive switching in diamond under high bias field *IEEE Trans. Electron Devices* **37** 2511–6

[348] van Driel H M, Code R F, Moss D J and Bharadwaj P K 1983 Picosecond photoconductive switching in semiconducting and insulating natural diamond *27th Annual Techincal Symp.* ed G A Mourou pp 101–4

[349] Hall D L, Voss L F, Grivickas P, Bora M, Conway A M, Scajev P and Grivickas V 2020 Photoconductive switch with high sub-bandgap responsivity in nitrogen-doped diamond *IEEE Electron Device Lett.* **41** 1070–3

[350] Cora I, Mezzadri F, Boschi F, Bosi M, Čaplovičová M, Calestani G, Dódony I, Pécz B and Fornari R 2017 The real structure of ε-Ga_2O_3 and its relation to κ-phase *CrystEngComm* **19** 1509–16

[351] Dobročka E, Gucmann F, Hušeková K, Nádaždy P, Hrubišák F, Egyenes F, Rosová A, Mikolášek M and Ťapajna M 2022 Structure and thermal stability of ε/κ-Ga_2O_3 films deposited by liquid-injection MOCVD *Materials* **16** 20

[352] Higashiwaki M, Sasaki K, Kuramata A, Masui T and Yamakoshi S 2012 Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates *Appl. Phys. Lett.* **100** 013504

[353] Dong P, Zhang J, Yan Q, Liu Z, Ma P, Zhou H and Hao Y 2022 6 kV/3.4 mΩ·cm^2 vertical β-Ga_2O_3 Schottky barrier diode with $BV^2/R_{on,sp}$ performance exceeding 1D unipolar limit of GaN and SiC *IEEE Electron Device Lett.* **43** 765–8

[354] Zhang J *et al* 2022 Ultra-wide bandgap semiconductor Ga_2O_3 power diodes *Nat. Commun.* **13** 3900

[355] Goto K, Konishi K, Murakami H, Kumagai Y, Monemar B, Higashiwaki M, Kuramata A and Yamakoshi S 2018 Halide vapor phase epitaxy of Si doped β-Ga_2O_3 and its electrical properties *Thin Solid Films* **666** 182–4

[356] Ma N, Tanen N, Verma A, Guo Z, Luo T, Xing H and Jena D 2016 Intrinsic electron mobility limits in β-Ga_2O_3 *Appl. Phys. Lett.* **109** 212101

[357] Ghosh K and Singisetti U 2016 Ab initio calculation of electron–phonon coupling in monoclinic β-Ga_2O_3 crystal *Appl. Phys. Lett.* **109** 072102

[358] Onuma T *et al* 2016 Temperature-dependent exciton resonance energies and their correlation with IR-active optical phonon modes in β-Ga_2O_3 single crystals *Appl. Phys. Lett.* **108** 101904

[359] Ghosh K and Singisetti U 2017 Ab initio velocity-field curves in monoclinic β-Ga_2O_3 *J. Appl. Phys.* **122** 035702

[360] Guo Z, Verma A, Wu X, Sun F, Hickman A, Masui T, Kuramata A, Higashiwaki M, Jena D and Luo T 2015 Anisotropic thermal conductivity in single crystal β-gallium oxide *Appl. Phys. Lett.* **106** 111909

[361] Ueda N, Hosono H, Waseda R and Kawazoe H 1997 Synthesis and control of conductivity of ultraviolet transmitting β-Ga_2O_3 single crystals *Appl. Phys. Lett.* **70** 3561–3

[362] Víllora E G, Shimamura K, Yoshikawa Y, Aoki K and Ichinose N 2004 Large-size β-Ga_2O_3 single crystals and wafers *J. Cryst. Growth* **270** 420–6

[363] Ohira S, Yoshioka M, Sugawara T, Nakajima K and Shishido T 2006 Fabrication of hexagonal GaN on the surface of β-Ga_2O_3 single crystal by nitridation with NH_3 *Thin Solid Films* **496** 53–57

[364] Tomm Y, Reiche P, Klimm D and Fukuda T 2000 Czochralski grown Ga_2O_3 crystals *J. Cryst. Growth* **220** 510–4

[365] Galazka Z *et al* 2014 On the bulk β-Ga_2O_3 single crystals grown by the Czochralski method *J. Cryst. Growth* **404** 184–91

[366] Aida H, Nishiguchi K, Takeda H, Aota N, Sunakawa K and Yaguchi Y 2008 Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method *Jpn. J. Appl. Phys.* **47** 8506

[367] Higashiwaki M, Sasaki K, Murakami H, Kumagai Y, Koukitu A, Kuramata A, Masui T and Yamakoshi S 2016 Recent progress in Ga_2O_3 power devices *Semicond. Sci. Technol.* **31** 034001

[368] Galazka Z, Uecker R, Klimm D, Irmscher K, Naumann M, Pietsch M, Kwasniewski A, Bertram R, Ganschow S and Bickermann M 2016 Scaling-up of bulk β-Ga_2O_3 single crystals by the Czochralski method *ECS J. Solid State Sci. Technol.* **6** Q3007

[369] Kuramata A, Koshi K, Watanabe S, Yamaoka Y, Masui T and Yamakoshi S 2016 High-quality β-Ga_2O_3 single crystals grown by edge-defined film-fed growth *Jpn. J. Appl. Phys.* **55** 1202A2

[370] Víllora E G, Shimamura K, Kitamura K and Aoki K 2006 Rf-plasma-assisted molecular-beam epitaxy of β-Ga_2O_3 *Appl. Phys. Lett.* **88** 031105

[371] Oshima T, Arai N, Suzuki N, Ohira S and Fujita S 2008 Surface morphology of homoepitaxial β-Ga_2O_3 thin films grown by molecular beam epitaxy *Thin Solid Films* **516** 5768–71

[372] Sasaki K, Higashiwaki M, Kuramata A, Masui T and Yamakoshi S 2014 Growth temperature dependences of structural and electrical properties of Ga_2O_3 epitaxial films grown on β-Ga_2O_3 (010) substrates by molecular beam epitaxy *J. Cryst. Growth* **392** 30–33
[373] Okumura H, Kita M, Sasaki K, Kuramata A, Higashiwaki M and Speck J S 2014 Systematic investigation of the growth rate of β-Ga_2O_3(010) by plasma-assisted molecular beam epitaxy *Appl. Phys. Express* **7** 095501
[374] Sasaki K, Kuramata A, Masui T, Víllora E G, Shimamura K and Yamakoshi S 2012 Device-quality β-Ga_2O_3 epitaxial films fabricated by ozone molecular beam epitaxy *Appl. Phys. Express* **5** 035502
[375] Higashiwaki M 2022 β-Ga_2O_3 material properties, growth technologies, and devices: a review *AAPPS Bull.* **32** 3
[376] Nomura K, Goto K, Togashi R, Murakami H, Kumagai Y, Kuramata A, Yamakoshi S and Koukitu A 2014 Thermodynamic study of β-Ga_2O_3 growth by halide vapor phase epitaxy *J. Cryst. Growth* **405** 19–22
[377] Murakami H *et al* 2014 Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy *Appl. Phys. Express* **8** 015503
[378] Alema F, Zhang Y, Osinsky A, Valente N, Mauze A, Itoh T and Speck J S 2019 Low temperature electron mobility exceeding 104 cm^2/V s in MOCVD grown β-Ga_2O_3 *APL Mater.* **7** 121110
[379] Zhang Y, Alema F, Mauze A, Koksaldi O S, Miller R, Osinsky A and Speck J S 2019 MOCVD grown epitaxial β-Ga_2O_3 thin film with an electron mobility of 176 cm^2/V s at room temperature *APL Mater.* **7** 022506
[380] Feng Z, Anhar Uddin Bhuiyan A F M, Karim M R and Zhao H 2019 MOCVD homoepitaxy of Si-doped (010) β-Ga_2O_3 thin films with superior transport properties *Appl. Phys. Lett.* **114** 250601
[381] Tadjer M J *et al* 2020 Characterization of β-Ga_2O_3 homoepitaxial films and MOSFETs grown by MOCVD at high growth rates *J. Appl. Phys.* **54** 034005
[382] Alema F, Zhang Y, Osinsky A, Orishchin N, Valente N, Mauze A and Speck J S 2020 Low 10^{14} cm^{-3} free carrier concentration in epitaxial β-Ga_2O_3 grown by MOCVD *APL Mater.* **8** 021110
[383] Anhar Uddin Bhuiyan A F M, Feng Z, Johnson J M, Chen Z, Huang H-L, Hwang J and Zhao H 2019 MOCVD epitaxy of β-$(Al_xGa_{1-x})_2O_3$ thin films on (010) Ga_2O_3 substrates and N-type doping *Appl. Phys. Lett.* **115** 120602
[384] Ranga P, Bhattacharyya A, Rishinaramangalam A, Ooi Y K, Scarpulla M A, Feezell D and Krishnamoorthy S 2020 Delta-doped β-Ga_2O_3 thin films and β-$(Al_{0.26}Ga_{0.74})_2O_3$/β-$Ga_2O_3$ heterostructures grown by metalorganic vapor-phase epitaxy *Appl. Phys. Express* **13** 045501
[385] Rafique S, Karim M R, Johnson J M, Hwang J and Zhao H 2018 LPCVD homoepitaxy of Si doped β-Ga_2O_3 thin films on (010) and (001) substrates *Appl. Phys. Lett.* **112** 052104
[386] Feng Z, Karim M R and Zhao H 2019 Low pressure chemical vapor deposition of β-Ga_2O_3 thin films: dependence on growth parameters *APL Mater.* **7** 022514
[387] Zhang Y, Feng Z, Karim M R and Zhao H 2020 High-temperature low-pressure chemical vapor deposition of β-Ga_2O_3 *J. Vac. Sci. Technol.* A **38** 050806
[388] Hu J *et al* 2023 Step flow growth of β-Ga_2O_3 films on off-axis 4H-SiC substrates by LPCVD *Surf. Interfaces* **37** 102732
[389] Lee S, Kaneko K and Fujita S 2016 Homoepitaxial growth of beta gallium oxide films by mist chemical vapor deposition *Jpn. J. Appl. Phys.* **55** 1202B8
[390] Nishinaka H, Nagaoka T, Kajita Y and Yoshimoto M 2021 Rapid homoepitaxial growth of (010) β-Ga_2O_3 thin films via mist chemical vapor deposition *Mater. Sci. Semicond. Process.* **128** 105732
[391] Mondal A K, Deivasigamani R, Ping L K, Shazni Mohammad Haniff M A, Goh B T, Horng R H and Mohamed M A 2022 Heteroepitaxial growth of an ultrathin β-Ga_2O_3 film on a sapphire substrate using mist CVD with fluid flow modeling *ACS Omega* **7** 41236–45
[392] Egyenes-Pörsök F, Gucmann F, Hušeková K, Dobročka E, Sobota M, Mikolášek M, Fröhlich K and Ťapajna M 2020 Growth of α- and β-Ga_2O_3 epitaxial layers on sapphire substrates using liquid-injection MOCVD *Semicond. Sci. Technol.* **35** 115002
[393] Leedy K D *et al* 2018 Si content variation and influence of deposition atmosphere in homoepitaxial Si-doped β-Ga_2O_3 films by pulsed laser deposition *APL Mater.* **6** 101102
[394] Leedy K D *et al* 2017 Highly conductive homoepitaxial Si-doped Ga_2O_3 films on (010) β-Ga_2O_3 by pulsed laser deposition *Appl. Phys. Lett.* **111** 012103
[395] Neal A T *et al* 2018 Donors and deep acceptors in β-Ga_2O_3 *Appl. Phys. Lett.* **113** 062101
[396] Irmscher K, Galazka Z, Pietsch M, Uecker R and Fornari R 2011 Electrical properties of β-Ga_2O_3 single crystals grown by the Czochralski method *J. Appl. Phys.* **110** 063720
[397] Parisini A and Fornari R 2016 Analysis of the scattering mechanisms controlling electron mobility in β-Ga_2O_3 crystals *Semicond. Sci. Technol.* **31** 035023
[398] Oishi T, Koga Y, Harada K and Kasu M 2015 High-mobility β-Ga_2O_3($_{201}$) single crystals grown by edge-defined film-fed growth method and their Schottky barrier diodes with Ni contact *Appl. Phys. Express* **8** 031101
[399] Oishi T, Harada K, Koga Y and Kasu M 2016 Conduction mechanism in highly doped β-Ga_2O_3 single crystals grown by edge-defined film-fed growth method and their Schottky barrier diodes *Jpn. J. Appl. Phys.* **55** 030305
[400] Moser N *et al* 2017 Ge-doped β -Ga_2O_3 MOSFETs *IEEE Electron Device Lett.* **38** 775–8
[401] Lyons J L 2018 A survey of acceptor dopants for β-Ga_2O_3 *Semicond. Sci. Technol.* **33** 05LT02
[402] Peelaers H, Lyons J L, Varley J B and Van de Walle C G 2019 Deep acceptors and their diffusion in Ga_2O_3 *APL Mater.* **7** 022519
[403] He H, Orlando R, Blanco M A, Pandey R, Amzallag E, Baraille I and Rérat M 2006 First-principles study of the structural, electronic, and optical properties of Ga_2O_3 in its monoclinic and hexagonal phases *Phys. Rev.* B **74** 195123
[404] Peelaers H and Van de Walle C G 2015 Brillouin zone and band structure of β-Ga_2O_3 *Phys. Status Solidi* b **252** 828–32
[405] Varley J B, Janotti A, Franchini C and Van de Walle C G 2012 Role of self-trapping in luminescence and p-type conductivity of wide-band-gap oxides *Phys. Rev.* B **85** 081109
[406] Deák P, Duy Ho Q, Seemann F, Aradi B, Lorke M and Frauenheim T 2017 Choosing the correct hybrid for defect calculations: a case study on intrinsic carrier trapping in β-Ga_2O_3 *Phys. Rev.* B **95** 075208
[407] Gake T, Kumagai Y and Oba F 2019 First-principles study of self-trapped holes and acceptor impurities in Ga_2O_3 polymorphs *Phys. Rev. Mater.* **3** 044603
[408] Chikoidze E *et al* 2019 Enhancing the intrinsic p-type conductivity of the ultra-wide bandgap Ga_2O_3 semiconductor *J. Mater. Chem.* C **7** 10231–9
[409] Chikoidze E *et al* 2017 P-type β-gallium oxide: a new perspective for power and optoelectronic devices *Mater. Today Phys.* **3** 118–26
[410] Sasaki K, Higashiwaki M, Kuramata A, Masui T and Yamakoshi S 2013 Ga_2O_3 Schottky barrier diodes fabricated by using single-crystal β-Ga_2O_3 (010) substrates *IEEE Electron Device Lett.* **34** 493–5

[411] Higashiwaki M et al 2015 Ga_2O_3 Schottky barrier diodes with n^--Ga_2O_3 drift layers grown by HVPE *2015 73rd Annual Device Research Conf. (DRC)* pp 29–30
[412] Konishi K, Goto K, Murakami H, Kumagai Y, Kuramata A, Yamakoshi S and Higashiwaki M 2017 1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes *Appl. Phys. Lett.* **110** 103506
[413] Allen N, Xiao M, Yan X, Sasaki K, Tadjer M J, Ma J, Zhang R, Wang H and Zhang Y 2019 Vertical Ga_2O_3 Schottky barrier diodes with small-angle beveled field plates: a Baliga's figure-of-merit of 0.6 GW/cm^2 *IEEE Electron Device Lett.* **40** 1399–402
[414] Roy S, Bhattacharyya A, Ranga P, Splawn H, Leach J and Krishnamoorthy S 2021 High-k oxide field-plated vertical (001) β-Ga_2O_3 Schottky barrier diode with Baliga's figure of merit over 1 GW/cm^2 *IEEE Electron Device Lett.* **42** 1140–3
[415] Gong H H et al 2021 β-Ga_2O_3 vertical heterojunction barrier Schottky diodes terminated with p-NiO field limiting rings *Appl. Phys. Lett.* **118** 202102
[416] Lv Y et al 2021 Demonstration of β-Ga_2O_3 junction barrier Schottky diodes with a Baliga's figure of merit of 0.85 GW/cm^2 or a 5A/700 V handling capabilities *IEEE Trans. Power Electron.* **36** 6179–82
[417] Wang B, Xiao M, Spencer J, Qin Y, Sasaki K, Tadjer M J and Zhang Y 2023 2.5 kV vertical Ga_2O_3 Schottky rectifier with graded junction termination extension *IEEE Electron Device Lett.* **44** 221–4
[418] Li W et al 2018 2.44 kV Ga_2O_3 vertical trench Schottky barrier diodes with very low reverse leakage current *2018 IEEE Int. Electron Devices Meeting (IEDM)* pp 8.5.1–4
[419] Li W, Nomoto K, Hu Z, Jena D and Xing H G 2020 Field-plated Ga_2O_3 trench Schottky barrier diodes with a $BV^2/R_{on,sp}$ of up to 0.95 GW/cm^2 *IEEE Electron Device Lett.* **41** 107–10
[420] Kokubun Y, Kubo S and Nakagomi S 2016 All-oxide p–n heterojunction diodes comprising p-type NiO and n-type β-Ga_2O_3 *Appl. Phys. Express* **9** 091101
[421] Lu X, Zhou X, Jiang H, Ng K W, Chen Z, Pei Y, Lau K M and Wang G 2020 1-kV sputtered p-NiO/n-Ga_2O_3 heterojunction diodes with an ultra-low leakage current below \$1 μA/cm^2 *IEEE Electron Device Lett.* **41** 449–52
[422] Wang C et al 2021 Demonstration of the p-NiOx/n-Ga_2O_3 heterojunction Gate FETs and diodes with $BV^2/R_{on,sp}$ figures of merit of 0.39 GW/cm^2 and 1.38 GW/cm^2 *IEEE Electron Device Lett.* **42** 485–8
[423] Wang Y et al 2022 2.41 kV vertical P-Nio/n-Ga_2O_3 heterojunction diodes with a record Baliga's figure-of-merit of 5.18 GW/cm^2 *IEEE Trans. Power Electron.* **37** 3743–6
[424] Gong H H, Chen X H, Xu Y, Ren F-F, Gu S L and Ye J D 2020 A 1.86-kV double-layered NiO/β-Ga_2O_3 vertical p–n heterojunction diode *Appl. Phys. Lett.* **117** 022104
[425] Zhou F et al 2022 1.95-kV beveled-mesa NiO/β-Ga_2O_3 heterojunction diode with 98.5% conversion efficiency and over million-times overvoltage ruggedness *IEEE Trans. Power Electron.* **37** 1223–7
[426] Sasaki K, Higashiwaki M, Kuramata A, Masui T and Yamakoshi S 2013 Si-ion implantation doping in β-Ga_2O_3 and its application to fabrication of low-resistance ohmic contacts *Appl. Phys. Express* **6** 086502
[427] Zeng K, Wallace J S, Heimburger C, Sasaki K, Kuramata A, Masui T, Gardella J A and Singisetti U 2017 Ga_2O_3 MOSFETs using spin-on-glass source/drain doping technology *IEEE Electron Device Lett.* **38** 513–6
[428] Higashiwaki M, Sasaki K, Kamimura T, Hoi Wong M, Krishnamurthy D, Kuramata A, Masui T and Yamakoshi S 2013 Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3 (010) substrates and temperature dependence of their device characteristics *Appl. Phys. Lett.* **103** 123511
[429] Jia Y, Zeng K, Wallace J S, Gardella J A and Singisetti U 2015 Spectroscopic and electrical calculation of band alignment between atomic layer deposited SiO_2 and β-Ga_2O_3 (2^-01) *Appl. Phys. Lett.* **106** 102107
[430] Zeng K, Sasaki K, Kuramata A, Masui T and Singisetti U 2016 Depletion and enhancement mode β-Ga_2O_3 MOSFETs with ALD SiO_2 gate and near 400 V breakdown voltage *2016 74th Annual Device Research Conf. (DRC)* pp 1–2
[431] Wong M H, Sasaki K, Kuramata A, Yamakoshi S and Higashiwaki M 2016 Field-plated Ga_2O_3 MOSFETs with a breakdown voltage of over 750 V *IEEE Electron Device Lett.* **37** 212–5
[432] Zeng K, Vaidya A and Singisetti U 2018 1.85 kV breakdown voltage in lateral field-plated Ga_2O_3 MOSFETs *IEEE Electron Device Lett.* **39** 1385–8
[433] Sharma S, Zeng K, Saha S and Singisetti U 2020 Field-plated lateral Ga_2O_3 MOSFETs with polymer passivation and 8.03 kV breakdown voltage *IEEE Electron Device Lett.* **41** 836–9
[434] Sharma S, Meng L, Bhuiyan A F M A U, Feng Z, Eason D, Zhao H and Singisetti U 2022 Vacuum annealed β-Ga_2O_3 recess channel MOSFETs with 8.56 kV breakdown voltage *IEEE Electron Device Lett.* **43** 2029–32
[435] Li W, Nomoto K, Hu Z, Nakamura T, Jena D and Xing H G 2019 Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV *2019 IEEE Int. Electron Devices Meeting (IEDM)* pp 12.4.1–4
[436] Oshima T, Okuno T, Arai N, Suzuki N, Ohira S and Fujita S 2008 Vertical solar-blind deep-ultraviolet Schottky photodetectors based on β-Ga_2O_3 substrates *Appl. Phys. Express* **1** 011202
[437] Oshima T, Kaminaga K, Mukai A, Sasaki K, Masui T, Kuramata A, Yamakoshi S, Fujita S and Ohtomo A 2013 Formation of semi-insulating layers on semiconducting β-Ga_2O_3 single crystals by thermal oxidation *Jpn. J. Appl. Phys.* **52** 051101
[438] Wong M H, Murakami H, Kumagai Y and Higashiwaki M 2020 Enhancement-mode β-Ga_2O_3 current aperture vertical MOSFETs with N-ion-implanted blocker *IEEE Electron Device Lett.* **41** 296–9
[439] Wong M H, Goto K, Morikawa Y, Kuramata A, Yamakoshi S, Murakami H, Kumagai Y and Higashiwaki M 2018 All-ion-implanted planar-gate current aperture vertical Ga_2O_3 MOSFETs with Mg-doped blocking layer *Appl. Phys. Express* **11** 064102
[440] Wong M H, Goto K, Murakami H, Kumagai Y and Higashiwaki M 2019 Current aperture vertical β-Ga_2O_3 MOSFETs fabricated by N- and Si-ion implantation doping *IEEE Electron Device Lett.* **40** 431–4
[441] Zeng K, Soman R, Bian Z, Jeong S and Chowdhury S 2022 Vertical Ga_2O_3 MOSFET with magnesium diffused current blocking layer *IEEE Electron Device Lett.* **43** 1527–30
[442] Ma Y et al 2023 702.3 A·cm^{-2}/10.4 mΩ·cm^2 vertical β-Ga_2O_3 U-shape trench gate MOSFET with N-ion implantation *IEEE Electron Device Lett.* **44** 384–7
[443] Zhou X, Ma Y, Xu G, Liu Q, Liu J, He Q, Zhao X and Long S 2022 Enhancement-mode β-Ga_2O_3 U-shaped gate trench vertical MOSFET realized by oxygen annealing *Appl. Phys. Lett.* **121** 223501
[444] Green A J et al 2017 β-Ga_2O_3 MOSFETs for radio frequency operation *IEEE Electron Device Lett.* **38** 790–3
[445] Singh M et al 2018 Pulsed large signal RF performance of field-plated Ga_2O_3 MOSFETs *IEEE Electron Device Lett.* **39** 1572–5
[446] Moser N A et al 2020 Pulsed power performance of β-Ga_2O_3 MOSFETs at L-band *IEEE Electron Device Lett.* **41** 989–92
[447] Chabak K D et al 2018 Sub-micron gallium oxide radio frequency field-effect transistors *2018 IEEE MTT-S Int. Microwave Workshop Series on Advanced Materials and Proc. for RF and THz Applications (IMWS-AMP)* pp 1–3

[448] Kamimura T, Nakata Y and Higashiwaki M 2020 Delay-time analysis in radio-frequency β-Ga_2O_3 field effect transistors *Appl. Phys. Lett.* **117** 253501
[449] Xia Z *et al* 2019 β-Ga_2O_3 delta-doped field-effect transistors with current gain cutoff frequency of 27 GHz *IEEE Electron Device Lett.* **40** 1052–5
[450] Krishnamoorthy S *et al* 2017 Modulation-doped β-$(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$ field-effect transistor *Appl. Phys. Lett.* **111** 023502
[451] Oshima T, Kato Y, Kawano N, Kuramata A, Yamakoshi S, Fujita S, Oishi T and Kasu M 2017 Carrier confinement observed at modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunction interface *Appl. Phys. Express* **10** 035701
[452] Ahmadi E, Koksaldi O S, Zheng X, Mates T, Oshima Y, Mishra U K and Speck J S 2017 Demonstration of β-$(Al_xGa_{1-x})_2O_3/$β-Ga_2O_3 modulation doped field-effect transistors with Ge as dopant grown via plasma-assisted molecular beam epitaxy *Appl. Phys. Express* **10** 071101
[453] Zhang Y *et al* 2018 Demonstration of high mobility and quantum transport in modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures *Appl. Phys. Lett.* **112** 173502
[454] Zhang Y, Xia Z, Mcglone J, Sun W, Joishi C, Arehart A R, Ringel S A and Rajan S 2019 Evaluation of low-temperature saturation velocity in β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ modulation-doped field-effect transistors *IEEE Trans. Electron Devices* **66** 1574–8
[455] Kumar A, Ghosh K and Singisetti U 2020 Low field transport calculation of 2-dimensional electron gas in β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures *J. Appl. Phys.* **128** 105703
[456] Kalarickal N K, Xia Z, McGlone J F, Liu Y, Moore W, Arehart A R, Ringel S A and Rajan S 2020 High electron density β-$(Al_{0.17}Ga_{0.83})_2O_3/Ga_2O_3$ modulation doping using an ultra-thin (1 nm) spacer layer *J. Appl. Phys.* **127** 215706
[457] Vaidya A, Saha C N and Singisetti U 2021 Enhancement mode β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure FET (HFET) with high transconductance and cutoff frequency *IEEE Electron Device Lett.* **42** 1444–7
[458] Hrubišák F *et al* 2023 Heteroepitaxial growth of Ga_2O_3 on 4H-SiC by liquid-injection MOCVD for improved thermal management of Ga_2O_3 power devices *J. Vac. Sci. Technol.* A **41** 042708
[459] Nepal N *et al* 2020 Heteroepitaxial growth of β-Ga_2O_3 films on SiC via molecular beam epitaxy *J. Vac. Sci. Technol.* A **38** 063406
[460] Tahara D, Nishinaka H, Morimoto S and Yoshimoto M 2017 Stoichiometric control for heteroepitaxial growth of smooth ε-Ga_2O_3 thin films on c-plane AlN templates by mist chemical vapor deposition *Jpn. J. Appl. Phys.* **56** 078004
[461] Karim M R, Chen Z, Feng Z, Huang H-L, Johnson J M, Tadjer M J, Hwang J and Zhao H 2021 Two-step growth of β-Ga_2O_3 films on (100) diamond via low pressure chemical vapor deposition *J. Vac. Sci. Technol.* A **39** 023411
[462] Cheng Z, Wheeler V D, Bai T, Shi J, Tadjer M J, Feygelson T, Hobart K D, Goorsky M S and Graham S 2020 Integration of polycrystalline Ga_2O_3 on diamond for thermal management *Appl. Phys. Lett.* **116** 062105
[463] Xu W *et al* 2019 First demonstration of waferscale heterogeneous integration of Ga_2O_3 MOSFETs on SiC and Si substrates by ion-cutting process *2019 IEEE Int. Electron Devices Meeting (IEDM)* (IEEE) pp 12.5.1–12.5.4
[464] Xu W *et al* 2021 Efficient thermal dissipation in wafer-scale heterogeneous integration of single-crystalline β-Ga_2O_3 thin film on SiC *Fundam. Res.* **1** 691–6
[465] Song Y *et al* 2021 Ga_2O_3-on-SiC composite wafer for thermal management of ultrawide bandgap electronics *ACS Appl. Mater. Interfaces* **13** 40817–29
[466] Seki S, Funaki T, Arima J, Fujita M, Hirabayashi J and Hanabusa K 2023 Evaluation of thermal resistance reduction by thinning substrate of β-Ga_2O_3 SBD *2023 Int. Conf. on Electronics Packaging (ICEP)* (IEEE) pp 193–4
[467] Green A J *et al* 2022 β-Gallium oxide power electronics *APL Mater.* **10** 029201
[468] Fu H, Huang X, Chen H, Lu Z, Baranowski I and Zhao Y 2017 Ultra-low turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers *Appl. Phys. Lett.* **111** 152102
[469] Guo X *et al* 2021 High-voltage and high-I_{ON}/I_{OFF} quasi-vertical GaN-on-Si Schottky barrier diode with Argon-implanted termination *IEEE Electron Device Lett.* **42** 473–6
[470] Kizilyalli I C, Edwards A P, Nie H, Disney D and Bour D 2013 High voltage vertical GaN p-n diodes with avalanche capability *IEEE Trans. Electron Devices* **60** 10
[471] Wang J *et al* 2021 Demonstration of $Al_{0.85}Ga_{0.15}N$ Schottky barrier diode with >3 kV breakdown voltage and the reverse leakage currents formation mechanism analysis *Appl. Phys. Lett.* **118** 173505
[472] Kumaresan R, Umezawa H and Shikata S 2010 Vertical structure Schottky barrier diode fabrication using insulating diamond substrate *Diam. Relat. Mater.* **19** 1324–9
[473] Umezawa H, Shikata S and Funaki T 2014 Diamond Schottky barrier diode for high-temperature, high-power, and fast switching applications *Jpn. J. Appl. Phys.* **53** 05FP06
[474] Bormashov V S, Terentiev S A, Buga S G, Tarelkin S A, Volkov A P, Teteruk D V, Kornilov N V, Kuznetsov M S and Blank V D 2017 Thin large area vertical Schottky barrier diamond diodes with low on-resistance made by ion-beam assisted lift-off technique *Diam. Relat. Mater.* **75** 78–84
[475] Matsumoto T, Mukose T, Makino T, Takeuchi D, Yamasaki S, Inokuma T and Tokuda N 2017 Diamond Schottky-pn diode using lightly nitrogen-doped layer *Diam. Relat. Mater.* **75** 152–4
[476] Yang J, Ren F, Tadjer M, Pearton S J and Kuramata A 2018 2300V reverse breakdown voltage Ga_2O_3 Schottky rectifiers *ECS J. Solid State Sci. Technol.* **7** Q92
[477] Li J-S *et al* 2022 Demonstration of 4.7 kV breakdown voltage in NiO/β-Ga_2O_3 vertical rectifiers *Appl. Phys. Lett.* **121** 4
[478] Zhang Z *et al* 2016 Studies on high-voltage GaN-on-Si MIS-HEMTs using LPCVD Si_3N_4 as gate dielectric and passivation layer *IEEE Trans. Electron Devices* **63** 731–8
[479] Liu Y, Yu Q and Du J 2020 Simulation design of a high-breakdown-voltage p-GaN-gate GaN HEMT with a hybrid AlGaN buffer layer for power electronics applications *J. Comput. Electron.* **19** 1527–37
[480] Meunier R 2016 Optimization of the elaboration of insulating layers for the gate structures and the passivation of MIS-HEMT transistors on GaN *Theses* Université Paul Sabatier—Toulouse III (available at: https://hal.laas.fr/tel-01376016)
[481] Ji D, Agarwal A, Li H, Li W, Keller S and Chowdhury S 2018 880 V/2.7 Ω.cm^2 MIS gate trench CAVET on bulk GaN substrates *IEEE Electron Device Lett.* **39** 6
[482] Zhang W, Zhang J, Xiao M, Zhang L and Hao Y 2018 High breakdown-voltage (>2200 V) AlGaN-channel HEMTs with ohmic/Schottky hybrid drains *IEEE J. Electron Devices Soc.* **6** 931–5
[483] Saha N C, Oishi T, Kim S, Kawamata Y, Koyama K and Kasu M 2020 145-MW/cm^2 heteroepitaxial diamond MOSFETs with NO_2 p-type doping and an Al_2O_3 passivation layer *IEEE Electron Device Lett.* **41** 1066–9
[484] Soleimanzadeh R, Naamoun M, Khadar R A, van Erp R and Matioli E 2020 H-terminated polycrystalline diamond p-channel transistors on GaN-on-silicon *IEEE Electron Device Lett.* **41** 119–22

[485] Kawarada H *et al* 2016 Diamond MOSFETs using 2D hole gas with 1700V breakdown voltage *2016 28th Int. Symp. on Power Semiconductor Devices and ICs (ISPSD)* (IEEE) pp 483–6
[486] Bhattacharyya A, Ranga P, Roy S, Peterson C, Alema F, Seryogin G, Osinsky A and Krishnamoorthy S 2021 Multi-kV class β-Ga_2O_3 MESFETs with a lateral figure of merit up to 355 MW/cm^2 *IEEE Electron Device Lett.* **42** 1272–5
[487] Lv Y *et al* 2020 Enhancement-mode β-Ga_2O_3 metal-oxide-semiconductor field-effect transistor with high breakdown voltage over 3000 V realized by oxygen annealing *Phys. Status Solidi* **14** 1900586
[488] Hu Z, Nomoto K, Li W, Tanen N, Sasaki K, Kuramata A, Nakamura T, Jena D and Xing H G 2018 Enhancement-mode Ga_2O_3 vertical transistors with breakdown voltage >1 kV *IEEE Electron Device Lett.* **39** 869–72
[489] Chabak K D *et al* 2018 Recessed-gate enhancement-mode β -Ga_2O_3 MOSFETs *IEEE Electron Device Lett.* **39** 67–70
[490] Micovic M *et al* 2016 High frequency GaN HEMTs for RF MMIC applications *2016 IEEE Int. Electron Devices Meeting (IEDM)* pp 3.3.1–4
[491] Tang Y, Shinohara K, Regan D, Corrion A, Brown D, Wong J, Schmitz A, Fung H, Kim S and Micovic M 2015 Ultrahigh-speed GaN high-electron-mobility transistors with f_T/f_{max} of 454/444 GHz *IEEE Electron Device Lett.* **36** 549–51
[492] Schuette M L *et al* 2013 Gate-recessed integrated E/D GaN HEMT technology with f_T/f_{max} >300 GHz *IEEE Electron Device Lett.* **34** 741–3
[493] Shinohara K *et al* 2010 220GHz f_T and 400GHz f_{max} in 40-nm GaN DH-HEMTs with re-grown ohmic *2010 Int. Electron Devices Meeting* pp 30.1.1–4
[494] Shinohara K *et al* 2011 Electron velocity enhancement in laterally scaled GaN DH-HEMTs with f_T of 260 GHz *IEEE Electron Device Lett.* **32** 1074–6
[495] Huang S *et al* 2014 High-f_{MAX} high Johnson's figure-of-merit 0.2-μm gate AlGaN/GaN HEMTs on silicon substrate with AlN/SiN_x passivation *IEEE Electron Device Lett.* **35** 315–7
[496] Murase Y, Asano K, Takenaka I, Ando Y, Takahashi H and Sasaoka C 2014 T-shaped gate GaN HFETs on Si with improved breakdown voltage and f_{MAX} *IEEE Electron Device Lett.* **35** 524–6
[497] Zheng X, Guidry M, Li H, Ahmadi E, Hestroffer K, Romanczyk B, Wienecke S, Keller S and Mishra U K 2016 N-polar GaN MIS-HEMTs on sapphire with high combination of power gain cutoff frequency and three-terminal breakdown voltage *IEEE Electron Device Lett.* **37** 77–80
[498] Downey B P, Meyer D J, Katzer D S, Roussos J A, Pan M and Gao X 2014 SiN_x/InAlN/AlN/GaN MIS-HEMTs with 10.8 THz.V Johnson figure of merit *IEEE Electron Device Lett.* **35** 527–9
[499] Romanczyk B, Zheng X, Guidry M, Li H, Hatui N, Wurm C, Krishna A, Ahmadi E, Keller S and Mishra U K 2020 W-band power performance of SiN-passivated N-polar GaN deep recess HEMTs *IEEE Electron Device Lett.* **41** 349–52
[500] Romanczyk B, Li W, Guidry M, Hatui N, Krishna A, Wurm C, Keller S and Mishra U K 2020 N-polar GaN-on-sapphire deep recess HEMTs with high W-band power density *IEEE Electron Device Lett.* **41** 1633–6
[501] Then H W *et al* 2022 Scaled submicron field-plated enhancement mode high-K gallium nitride transistors on 300mm Si(111) wafer with power FoM (RON xQGG) of 3.1 mohm-nC at 40V and f_T/f_{MAX} of 130/680GHz *2022 Int. Electron Devices Meeting (IEDM)* pp 35.1.1–4
[502] Baca A G, Armstrong A M, Klein B A, Allerman A A, Douglas E A and Kaplar R J 2020 Al-rich AlGaN based transistors *J. Vac. Sci. Technol.* A **38** 020803
[503] Ivanov T G, Weil J, Shah P B, Birdwell A G, Kingkeo K and Viveiros E A 2018 Diamond RF transistor technology with $f_T = 41$ GHz and $f_{max} = 44$ GHz *IEEE MTT-S Int. Microwave Symp. Digest* (Institute of Electrical and Electronics Engineers Inc.) pp 1461–3
[504] Yu C *et al* 2019 RF performance of hydrogenated single crystal diamond MOSFETs *2019 IEEE Int. Conf. on Electron Devices and Solid-State Circuits (EDSSC)* pp 1–3
[505] Yu C, Zhou C J, Guo J C, He Z Z, Wang H X, Cai S J and Feng Z H 2020 650 mW/mm output power density of H-terminated polycrystalline diamond MISFET at 10 GHz *Electron. Lett.* **56** 334–5
[506] Yu X, Hu W, Zhou J, Liu B, Tao T, Kong Y, Chen T and Zheng Y 2021 1 W/mm output power density for H-terminated diamond MOSFETs with Al_2O_3/SiO_2 Bi-layer passivation at 2 GHz *IEEE J. Electron Devices Soc.* **9** 160–4
[507] Kudara K, Imanishi S, Hiraiwa A, Komatsuzaki Y, Yamaguchi Y, Kawamura Y, Shinjo S and Kawarada H 2021 High output power density of 2DHG diamond MOSFETs with thick ALD-Al_2O_3 *IEEE Trans. Electron Devices* **68** 3942–9
[508] Kudara K, Arai M, Suzuki Y, Morishita A, Tsunoda J, Hiraiwa A and Kawarada H 2022 Over 1 A/mm drain current density and 3.6 W/mm output power density in 2DHG diamond MOSFETs with highly doped regrown source/drain *Carbon* **188** 220–8
[509] Russell S A O, Sharabi S, Tallaire A and Moran D A J 2012 Hydrogen-terminated diamond field-effect transistors with cutoff frequency of 53 GHz *IEEE Electron Device Lett.* **33** 1471–3
[510] Kasu M and Oishi T 2016 Recent progress of diamond devices for RF applications *2016 IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS)* pp 1–4
[511] Joishi C, Zhang Y, Xia Z, Sun W, Arehart A R, Ringel S, Lodha S and Rajan S 2019 Breakdown characteristics of β-$(Al_{0.22}Ga_{0.78})_2O_3/Ga_2O_3$ field-plated modulation-doped field-effect transistors *IEEE Electron Device Lett.* **40** 1241–4
[512] Wu Y-F *et al* 1999 High Al-content AlGaN/GaN HEMTs on SiC substrates with very high power performance *Int. Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318)* pp 925–7
[513] Kubovic M, Kasu M, Kallfass I, Neuburger M, Aleksov A, Koley G, Spencer M G and Kohn E 2004 Microwave performance evaluation of diamond surface channel FETs *Diam. Relat. Mater.* **13** 802–7
[514] Camarchia V *et al* 2011 RF power performance evaluation of surface channel diamond MESFETs *Solid-State Electron.* **55** 19–24
[515] Yassine M, Nair A, Fammels J, Wade E, Fu Z, Yassine A, Kirste L and Ambacher O 2022 Influence of structural properties on the ferroelectric behavior of hexagonal AlScN *J. Appl. Phys.* **132** 114101
[516] Wang D, Wang P, He M, Liu J, Mondal S, Hu M, Wang D, Wu Y, Ma T and Mi Z 2023 Fully epitaxial, monolithic ScAlN/AlGaN/GaN ferroelectric HEMT *Appl. Phys. Lett.* **122** 090601