Cmos spdt switch for wlan applications

To cite this article: M A S Bhuiyan et al 2015 IOP Conf. Ser.: Mater. Sci. Eng. 78 012011

View the article online for updates and enhancements.

Related content
- Radiation effects on scientific CMOS image sensor
  Zhao Yuanfu, Liu Liyan, Liu Xiaohui et al.
- 10-bit segmented current steering DAC in 90nm CMOS technology
  R Bringas Jr, F Dy and O J Gerasta
- Two-phase low-power analogue CMOS peak detector with high dynamic range
  E Malankin
Cmos spdt switch for wlan applications

M A S Bhuiyan, M B I Reaz, L F Rahman and K N Minhad
Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia

E-mail: asobhan@eng.ukm.my

Abstract. WLAN has become an essential part of our today’s life. The advancement of CMOS technology let the researchers contribute low power, size and cost effective WLAN devices. This paper proposes a single pole double through transmit/receive (T/R) switch for WLAN applications in 0.13 µm CMOS technology. The proposed switch exhibit 1.36 dB insertion loss, 25.3 dB isolation and 24.3 dBm power handling capacity. Moreover, it only dissipates 786.7 nW power per cycle. The switch utilizes only transistor aspect ratio optimization and resistive body floating technique to achieve such desired performance. In this design the use of bulky inductor and capacitor is avoided to evade imposition of unwanted nonlinearities to the communication signal.

1. Introduction

The increased popularity of WLAN applications, in the recent years, has raised the demand for small power and less off-chip components which tends to achieve integration of multiple transmitter/receiver chains on the same die [1], which further increases the demand for highly integrated and area efficient designs.

![Figure 1. T/R switch at the WLAN transceiver front-end.](image)

All WLAN transceivers essentially need an efficient T/R switch for sharing a single antenna between its transmitter and receiver to compensate the size, cost and portability. It is one of the very...
crucial parts of a transceiver which deals with both high power transmitter and low power receiver circuit as shown in Figure 1. During transmission stage, the switch connects the antenna to the power amplifier of the transmitter to radiate large signal to the surroundings and at the same time protects the low power receiver circuit from being get damaged [2]. On the other hand, during reception stage, the switch ensures that the low noise amplifier receives the intended signal with minimum loss. However, the major requirements for a T/R switch are low insertion loss, high power handling capability, high linearity, good isolation and acceptable reliability [3-4].

Advances in CMOS technology allows the researchers to fabricate fully on-chip transceivers without compromising the performance issues [5]. This results in low power, small size and low cost wireless terminals for different applications such as RFID, Bluetooth, Zigbee, Wi-Fi and WLAN devices [6-7]. Consequently, to a great extent, this attracts more subscribers to enjoy affordable wireless communication services through WLAN.

The CMOS T/R switch presented, in this paper, can withstand more than 24 dBm PA output power with the normal 0.13 µm CMOS devices, by employing a novel floating device scheme. Over the 802.11g operation frequency band, the insertion loss due to the switch is less than 1.4 dB and it provides isolation of more than 25 dB to the receiver. This switch will be very useful for 2.4 GHz WLAN devices.

2. Methodology

The objective of this study is to design and simulate a CMOS switch to obtain better performance. The software named Mentor Graphics by Emerald Systems is used for the design and simulation of the switch. This software has two parts; first part is Design Architect IC (DA-IC) and second part is IC-Station. Design Architect has been used to design the schematics of the T/R switch circuit and for the simulation to obtain the result.

The schematic of the proposed series-shunt T/R switch is illustrated in Figure 2. It consists of one voltage source, six transistors and eight resistors only. The transistors M5 and M6 form an inverter circuit. Control signals Vc and Vc´ are used to switch the transistors M1, M2, M3 and M4 from their ON to OFF states and vice versa. The series transistors, M1 and M2, perform main switching task while the shunt transistors, M3 and M4, provide low-impedance paths for the unwanted signals to the RF ground. Therefore, the two shunt arms make the T/R switch achieve relatively better isolation between transmitter and receiver port but at the cost of high insertion loss.

Transistor ON state resistance is the dominant factor responsible for insertion loss. Because of this, only n-channel MOS transistors are utilized in the design as their conductivity is higher than the p-channel MOSs. The drain-to-body and source-to-body junction capacitances of the transistors are also
critical factors determining insertion loss. Therefore, optimization of the transistor width-length is very important [8-9].

The gate resistances help to improve the isolation by decreasing the effect of capacitive coupling of the OFF transistors [10] whereas the body floating resistors helps to meliorate power handling capacity by retaining the high input impedance of the transistor by offering a high resistance to the source/Drain to body diode [11-12]. The components used in this study are given in Table 1.

<table>
<thead>
<tr>
<th>Elements</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 – M4</td>
<td>60/0.13 µm</td>
</tr>
<tr>
<td>RG1 – RG4</td>
<td>5 Ω</td>
</tr>
<tr>
<td>RB1 – RB4</td>
<td>50Ω</td>
</tr>
<tr>
<td>Vc and Vc’</td>
<td>1.2 V and 0 V</td>
</tr>
</tbody>
</table>

3. Results and discussions
The switch proposed in this paper has been designed in 130 nm CMOS technology. Mentor graphics Design Architect has been used for the simulation study. The isolation, insertion loss and power handling capacity are the three main characteristics of a transmit/receive switch. These parameters are also interrelated and tradeoffs among them cannot be ignored [9].

![Figure 3. Insertion loss of the switch at 2.4 GHz band.](image)

In this paper, the insertion loss, isolation and power handling capacity of the proposed switch is measured in transient analysis mode. Figure 3 and Figure 4 show the insertion loss and isolation of the switch. From the simulation it is obvious that the switch exhibit 25.1 dB isolation and 1.36 dB insertion loss. It is also apparent that the values of insertion loss and isolation for the 2.4 GHz WLAN remains almost constant for the proposed switch.
Figure 4. Isolation of the switch at 2.4 GHz band.

Figure 5 shows the insertion loss and isolation of the switch as a function of input power (Pin). The insertion loss of the switch is found to increase exponentially with input power but the isolation is found to decrease steadily. At P1dB point the values of the insertion loss and isolation are 1.36 dB and 25.3 dB respectively.

Figure 5. Insertion loss and isolation of the switch with input power.
The linearity as well as the power handling capacity of a switch is usually determined by the 1 dB compression (P1dB) point. The higher the P1dB point, the more the switch handles RF power within acceptable level of nonlinearity. Therefore, this characteristic can be considered as stability of the switch at high input power during the transmission period. Figure 6 shows the large signal linearity of the switch and the value of the P1db found is 24.3 dBm.

Therefore, the proposed switch can handle large amount of power during transmission mode with a very small insertion loss and better isolation of low power receiver circuit. It also dissipates very small amount of power which is only 786.7 nW per cycle. Table 2 gives the summery of the performance of the switch.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion loss</td>
<td>1.36 dB</td>
</tr>
<tr>
<td>Isolation</td>
<td>25.3 dB</td>
</tr>
<tr>
<td>P1dB</td>
<td>24.3 dBm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>786.7 nW</td>
</tr>
</tbody>
</table>

4. Conclusion
This paper proposes a single pole double through transmit/receive (T/R) switch for compact WLAN devices. For the simulation, Mentor graphics 0.13 µm CMOS technology is used. The proposed switch exhibit 1.36 dB insertion loss, 25.3 dB isolation and 24.3 dBm power handling capacity. Transistor aspect ratio optimization and resistive body floating technique are utilized in this circuit to achieve such desired performance. It only dissipates 786.9 nW power per cycle. In this design the use of bulky inductor and capacitor is avoided and therefore, the size and cost of the devices will be reduced. Such a switch will be very useful for cost effective WLAN devices.

5. References
Rael J J and Marholev B 2007 a fully integrated MIMO multiband direct conversion CMOS transceiver for WLAN applications (802.11n) *IEEE J. Solid-St. Circ.* **42** 2795


