Low-power low-jitter PLL clock synthesizer for microprocessors with clock range 200-768 MHz

To cite this article: V Baykov and A Garmash 2016 IOP Conf. Ser.: Mater. Sci. Eng. 151 012036

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Low-power low-jitter PLL clock synthesizer for microprocessors with clock range 200-768 MHz

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Abstract: In this article the results of the clock synthesizer development are shown. Different variants of voltage repeater for the system of automatic frequency tuning were analyzed. It was shown that for the purpose of energy consumption and jitter reducing the repeater on peripheral transistor can be used. The synthesizer was created on the technology with design rules 180 nm. Scaling for the technology with design rules 90 nm is also possible.

1. Introduction
Frequency synthesizers (FS) with phase locked loop (PLL) are widely used in modern high-performance digital, switching and wireless systems. Usage of complex functional (IP) block of SC PLL is the effective way of clock signals distribution chain construction and reducing energy consumption in it. For this chain, SC can be both sources and distributor (knot of chain) of clock signals.

Using PLL as the sources of synchronous signal demands high stability of frequency. Its jitter should be as low as possible. Phase deviation of a clock pulse from the reference signal can cause a malfunction in system times of date setup and date holding. This situation is most dangerous in communication systems and systems with the import of date from external sources. In both cases very precision synchronization must be provided.

PLL jitter reduction questions are discussed in many publications and some methods of solving these problems have been proposed [1-2]. In this work jitter decreasing was achieved not only by means of known methods but also due to simplification of analog part of PLL. Peripheral n-channel MOSFET transistor was used as voltage repeater, what allowed 5-times are reducing of phase jitter.

2. Interface
For perspective Micron technologies with design rules, 90 nm was constructed a functional block of IPPLL. The purpose of the design was solving synchronization problems in high-performance microprocessors which clock frequency is in the range of 5-800 MHz. Characteristics of IP-block were optimized for the range of power source voltage 1.0-1.2 V and the range of working temperature 60-125°C.

FS-block designed to be integrated into VLSI system on chip and is the source of the clock signal for distribution tree of clock signal propagation. The symbol of IP-block PLL is shown in Figure 1, the appointment of external connections is described in Table 1.
### Table 1. Appointment of external connections of IP-block.

<table>
<thead>
<tr>
<th>Pin name</th>
<th>Pin type</th>
<th>Pin function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_IN</td>
<td>I</td>
<td>Input frequency</td>
</tr>
<tr>
<td>PLL_EN</td>
<td>I</td>
<td>PLL on/off</td>
</tr>
<tr>
<td>SEL[6:0]</td>
<td>I</td>
<td>PLL programming</td>
</tr>
<tr>
<td>CLK_OUT</td>
<td>O</td>
<td>Output frequency</td>
</tr>
</tbody>
</table>

3. **PLL realization feature**

Common structural scheme of IP block FSPLL [3] is shown in Figure 2. It consists of digital and analog components. Digital part includes frequency divider with programmable coefficients K and L, which value are determined by the control signal. Analog part includes: stabilized block of bias voltage (is not shown); phase-frequency detector (PFD); charge pump; 2-d order capacitive filter of low frequency (LPF); integrated capacity (C); damping circuit C_d, R_d; voltage repeater (1); voltage control frequency generator (VCO).

![Figure 2. Common structural scheme of IP block SC PLL.](image)

Earlier authors substantiated [4-5] that good decision for microprocessor’s PLL is inverter generator and voltage repeater shown in Figure 3. For the technology with design rule, 180 nm the jitter of this scheme is in acceptable limits [6].

However, computer simulation of this circuit solution has shown that for 90-nm technology the value of phase jitter can reach critical limit 100 psec. It is unacceptable for microprocessors with a clock frequency in the range 200-780 MHz and high. As it turned out the main source of jitter in this design is voltage repeater. Transistor’s electrical noise in it causes voltage oscillations $U_{ref}$ (Fig.2). Whereas $U_{ref}$ is the control voltage for frequency generator, the frequency of the last also changes proportionally to the voltage of transistor’s noise.
One of the methods of noise reduction is the increase of transistor’s size. Correction of transistors area (increase in 1.5 times) allowed reducing of phase jitter in 4.5 times. For normal condition, its value did not exceed an acceptable level of 18.5 psec. However, this correction inevitably reduces the coefficient of noise suppression for power bus.

To solve the problem of jitter reduction without disturbing the noise suppression, the peripheral transistor was used as voltage repeater. For this purpose charge pump block was modernized (Fig 4) and adapted for peripheral voltage supply 2.5 V (PVDD).

4. Measurement

On Fig. 5 the plots of the relation between noise reduction coefficient and frequency for 3 variants of voltage repeater are shown. The best characteristic in working frequency range has the repeater on the peripheral transistor.

![Figure 4. Modernized voltage repeater.](image)

![Figure 5. Noise reduction coefficient in power bus.](image)
In Table 2 the results of measurement of phase noise and phase jitter of FSPLL for 3 variants of voltage repeater. The best characteristics also belong to variant with a peripheral transistor.

Table 2. Results of measurement.

<table>
<thead>
<tr>
<th>Repeater variant</th>
<th>Phase noise (for 1 MHz)</th>
<th>Phase jitter (sigma)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>-72 dB</td>
<td>82.8 ps</td>
</tr>
<tr>
<td>Standard with increased area</td>
<td>-85 dB</td>
<td>18.6 ps</td>
</tr>
<tr>
<td>Single peripheral transistor</td>
<td>-87.7 dB</td>
<td>15.4 ps</td>
</tr>
</tbody>
</table>

5. Conclusion
Results of computer simulations and tests shown that the usage of voltage repeater on the peripheral transistor in PLL can significantly reduce phase jitter. It is very important for technologies with high transistor’s noise level. The disadvantage of this technical decision is the necessity of additional lines of peripheral voltage and ground supply.

Developed FSPLL possesses following characteristics:
- Frequency range 4-762 MHz;
- Reference frequency 4-6 MHz;
- Phase jitter – not more 16 ps;
- Setting time of frequency - not more than 50 μs;
- Mean current consumption for PLL EN = 0 – not more than 65 μA;
- Mean current consumption for PLL EN = 1 – not more than 1 mA.

References