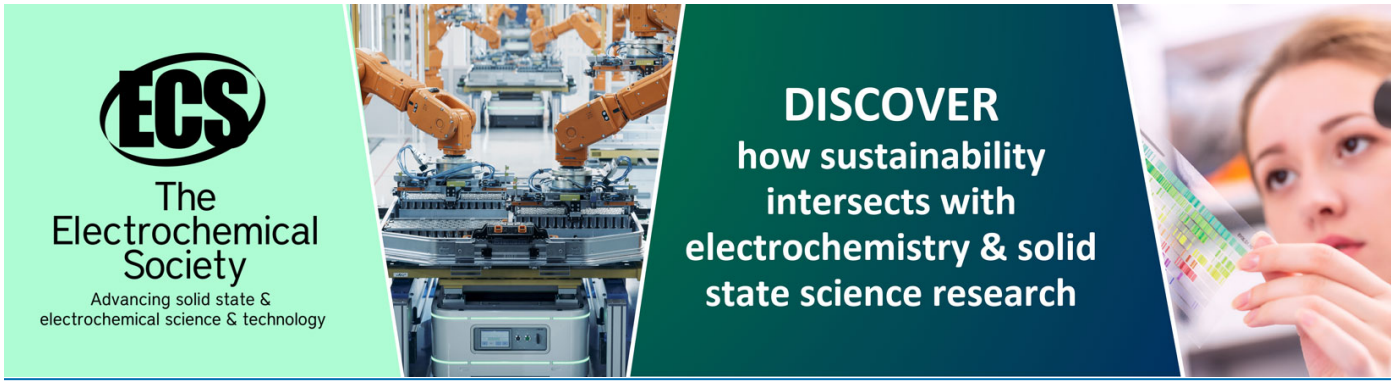
A grid-connected single-phase photovoltaic micro inverter



A grid-connected single-phase photovoltaic micro inverter

X Y Wen[1], P J Lin[1,2,3], Z C Chen[1,2], L J Wu[1,2] and S Y Cheng[1,2,3]

[1]Institute of Micro/Nano Devices and Solar Cells, College of Physics and Information Engineering, Fuzhou University, Fuzhou 350116, China
[2]Jiangsu Collaborative Innovation Center of Photovoltaic Science and Engineering, 213164 Changzhou, China

E-mail: linpeijie@fzu.edu.cn/ sycheng@fzu.edu.cn

Abstract. In this paper, the topology of a single-phase grid-connected photovoltaic (PV) micro-inverter is proposed. The PV micro-inverter consists of DC-DC stage with high voltage gain boost and DC-AC conversion stage. In the first stage, we apply the active clamp circuit and two voltage multipliers to achieve soft switching technology and high voltage gain. In addition, the flower pollination algorithm (FPA) is employed for the maximum power point tracking (MPPT) in the PV module in this stage. The second stage cascades a *H*-bridge inverter and LCL filter. To feed high quality sinusoidal power into the grid, the software phase lock, outer voltage loop and inner current loop control method are adopted as the control strategy. The performance of the proposed topology is tested by Matlab/Simulink. A PV module with maximum power 300W and maximum power point voltage 40V is applied as the input source. The simulation results indicate that the proposed topology and the control strategy are feasible.

1. Introduction

Recently, distributed photovoltaic (PV) power plants have become increasingly popular all over the world. Compared to the traditional centralized inverter or string inverter, photovoltaic micro-inverter has the advantage of achieving maximum power point tracking (MPPT) in single PV module [1-3]. Due to the characteristics of independence, single or several micro inverters fault would not affect the normal operation of entire PV power plant. In addition, micro inverter can locate the fault point quickly and accurately, so the PV micro inverter can improve the reliability of PV plants and the output efficiency of PV modules greatly. As the core of photovoltaic power generation system of power conversion, PV inverter's reliability and energy conversion efficiency have attracted great attention. For this, there is an effective way for improving the reliability and efficiency of the photovoltaic inverter to enhance topology and grid control strategy.

According to the number of transform stage, the topology of micro inverter can be divided into single-stage and multi-stage inverters [4,5], among which the two-stage converter is mainly applied. Generally, the first stage DC-DC realizes the MPPT and boost, and the second stage DC-AC realizes the inverter and grid-connected. According to whether the power transformer is supplied in convertor, micro inverters can be subdivided into isolated or non-isolated [6,7]. The former has the advantages of high voltage gain and simple circuit, but the volume is large and the efficiency is low. Since there has no transformer, the non-isolated inverter has the advantages of high efficiency, small size, light weight and low cost. However high voltage gain should be solved urgently because of the low output voltage of PV modules. Consequently, we propose a micro inverter, whose first stage DC boost contains non-

isolation, coupled inductor and active clamp module in the first stage as well as adopts *H*-bridge topology in second stage. Moreover, the flower pollination algorithm (FPA) is applied as the global MPPT technology. Finally, a simulation based on Matlab/Simulink is carried out to test the feasibility of the proposed topology and control strategy.

2. Analysis of system structure and working principle

2.1. System structure

The proposed inverter consists of DC-DC boost, DC-AC conversion, voltage and current acquisition, data processing and MPPT controller. The system block diagram is shown in figure 1. The flower pollination algorithm (FPA) is used to track maximum power point. The *H*-bridge topology is adopted in the second stage. The amplitude of the inverter's output current is controlled by the inner current loop and the outer voltage loop. The output filter is LCL filter.

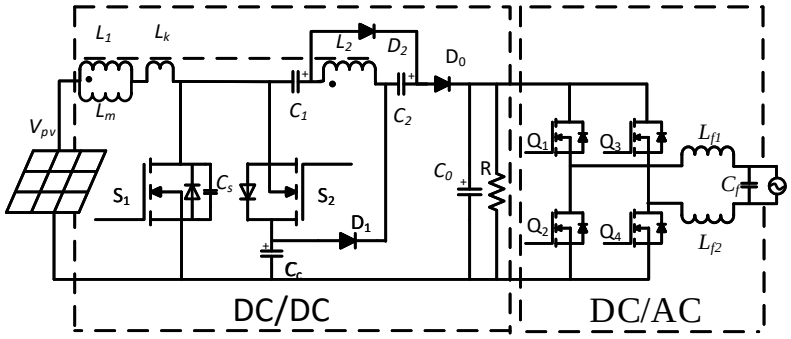


Figure 1. The block diagram of the proposed topology.

2.2. Operation principle of front stage DC-DC converter

The proposed DC-DC converter applies the non-isolated boost circuit with coupled inductor and active clamp module, which can obtain a higher voltage gain than basic boost circuit at the same duty ratio [8]. The coupled inductor is equivalents to ideal transformer (L_1, L_2), magnetizing inductance L_m and leakage inductance L_k. The active clamp module consists of the clamp switch S_2 and the clamp capacitor C_c, as shown in figure 1. The input voltage range of DC/DC converter is designed as 30-65 V, and the output DC bus voltage is about 400 V.

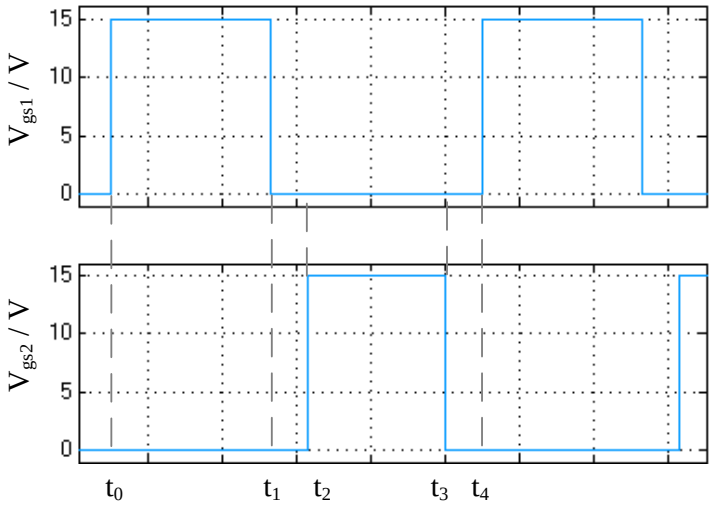


Figure 2. Switching sequence of S_1 and S_2.

The proposed topology operates under the continuous conduction mode (CCM). The switching sequence of DC/DC converter is shown in figure 2, which includes four operating periods, i.e, *t_0-t_1, t_1-t_2, t_2-t_3 and t_3-t_4*, and the corresponding operating mode is shown in figure 3. The steady-state analysis of the four mode is described as follows.

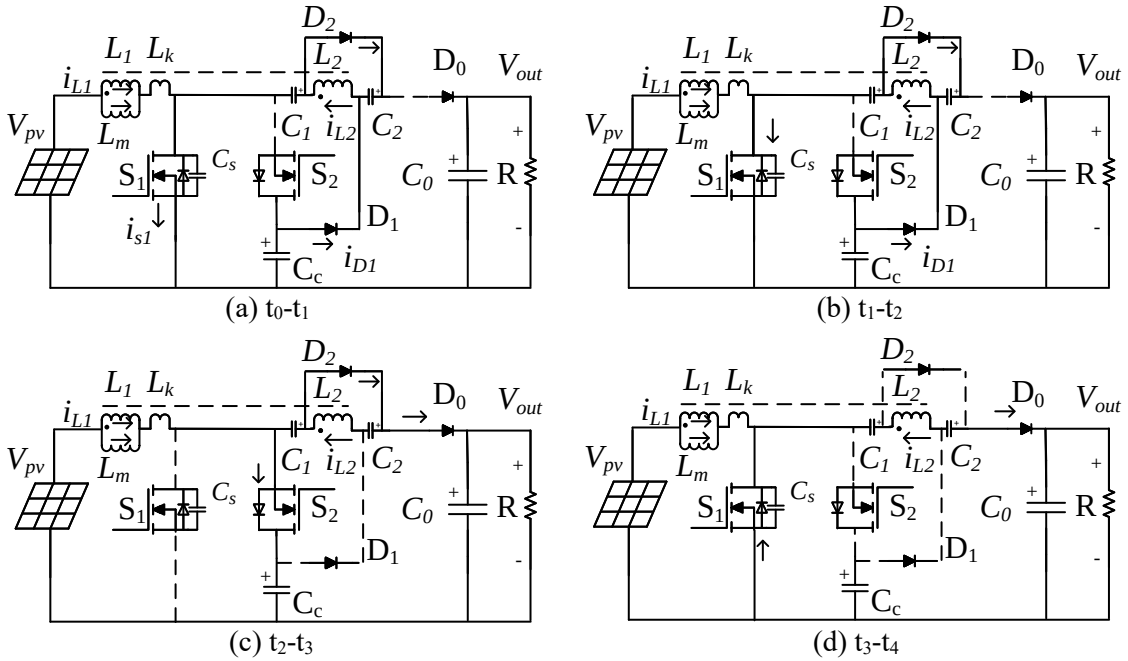


Figure 3. The four operating mode of DC/DC converter.

Mode 1(t_0-t_1): once PV module output voltage exceeds 30 V, the power switching S_1 and S_2 begin to be controlled by a set of complementary PWM signals with different duty cycles. When the main switch S_1 is turned on, and the clamp switch S_2 is turned off, the primary current i_{L1} and secondary current i_{L2} of the coupling inductance start to increase linearly. The energy stored on the clamp capacitor C_c through D_1, L_2 to C_1; L_2's energy through D_2 to C_2; and D_0 is turned off. At the same time, the DC bus capacitor C_0 provides energy to the second stage. According to the capacitance volt-seconds balance theorem, the average charge current value of the capacitor equals to the average discharge current value as shown in equation (1).

$$\bar{I}c_{1\_discharge} = \bar{I}c_{2\_discharge} = \bar{I}_{D_0} = \bar{I}_0 \tag{1}$$

The secondary peak current can be expressed as:

$$I_{L_2\_on\_peak} = \frac{2\left(I_{C_{1\_charge}} + I_{C_{2\_charge}}\right)}{D} = \frac{4\bar{I}_0}{D} \tag{2}$$

The voltage of leakage inductance L_k can be expressed as:

$$V_{L_{k\_on}} = L_K N \frac{I_{L_2\_on\_peak}}{DT} = \frac{4N\bar{I}_0 L_k f_s}{D^2} \tag{3}$$

The voltage of the capacitor C_1 and C_2 can be expressed as:

$$V_{c1} = V_{Cc} + N(V_{in} - V_{L_K\_on}) \tag{4}$$

$$V_{c2} = N(V_{in} - V_{L_K\_on}) \tag{5}$$

Mode 2(t_2-t_3): when the main switch S_1 is turned off and the clamp switch S_2 is turned on, then the primary current of coupling inductance begins to charge C_c via S_2. Meanwhile, the secondary current of coupling inductance i_{L2} begin to decline. Then D_1 is cut off, and the energy stored on C_1 and C_2 begins to charge C_0 through D_2 and D_0 for providing to the second stage.

The secondary peak current can be expressed as:

$$I_{L_{2\_off\_peak}} = \frac{2\bar{I}_{D_0}}{1-D} = \frac{2\bar{I}_0}{1-D} \tag{6}$$

The voltage of leakage inductance L_k can be expressed as:

$$V_{L_{k\_off}} = L_K N \frac{I_{L_{2\_off\_peak}}}{(1-D)T} = \frac{2N\bar{I}_0 L_k f_s}{(1-D)^2} \tag{7}$$

Mode 3(t_1-t_2/t_3-t_4): when the main switch S_1 and S_2 are turned off together, there are two cases. Case 1(t_1-t_2): L_k and parasitic capacitance C_s in S_1 induce resonance. Due to the small value of C_s, V_{cs} can quickly rises to V_{Cc}, leading to the anti-parallel diode of switch S_2 turn on, which can clamp V_{cs} at V_{Cc}. Since the anti-parallel diode of S_2 has been turned on, the S_2 can achieve zero-voltage-switching (ZVS) when there is a drive signal at t_2, which greatly reduces the switching loss; Case 2(t_3-t_4): At t_3 the switch S_2 turned off, the C_s in S_1 begins to supply power to the load. Because C_s is very small, the voltage of S_1 drops to zero rapidly. Then the anti-parallel diode of S_1 is turned on, which makes the S1 working at zero voltage switching possible [9]. At t_4, the DC/DC converter returns to the working state of mode 1.

According to the Thévenin's theorem, the output voltage is:

$$V_{\text{out}} = V_{Cc} + V_{c1} + N(V_{Cc} - V_{pv} - V_{L_{k\_off}}) + V_{c2} \tag{8}$$

where V_{Cc} equals V_{pv} / (1-D) according to the inductance volt-seconds balance theorem. The voltage gain can be calculated by substituting the V_{Cc}, equations (6) and (7) into equation (8) as follows,

$$\frac{V_{\text{out}}}{V_{pv}} = \frac{(2+2N-ND)}{1-D} \frac{1}{1+\frac{8N^2 L_k f_s}{RD^2} + \frac{2N^2 L_k f_s}{R(1-D)^2}} \tag{9}$$

where N is the ratio between the secondary side and the primary side of coupling inductance, D is the duty cycle of the main switch S_1, R is the equivalent resistance of the second stage, L_k is the inductance value of the leakage inductance, f_s is the switching frequency. Obviously, the voltage gain is related to N, D, R, L_k, f_s.

2.3. Maximum power point tracking control algorithm

According to the output P-V characteristic curve of the photovoltaic module, the maximum power point varies with the change of irradiance and module temperature. There are a variety of MPPT algorithms, such as open circuit voltage method, perturb and observe method, conductance increment method and global intelligent optimization algorithm [10]. It is difficult for the traditional algorithms to judge the global maximum power point in the situation of multi-peak under partial shadow. Therefore, the evolution algorithm FPA is adopted [11].

FPA algorithm is a global group optimization algorithm, which follows the natural pollen propagation behaviour. The algorithm includes two processes of global pollination and local pollination [12]. In the global pollination stage, pollinators carry pollen for Levy flight, which can reach far places, and ensure that the most polluted and pollinated flowers of the environment. The

global pollination is defined as follows:

$$x_i^{t+1} = x_i^t + C_p \cdot L\left(x_i^t - g^*\right) \tag{10}$$

where x_i^t represents the i^{th} solution at t^{th} generation, g^* is the best flower, C_p is the step coefficient of *Levy* flight, L is *Levy* flight distance. The typical *Levy* flight in a two-dimension plane is depicted in figure 4. After searching an area with many smaller steps, it will shift to another area by long distance jumps. Comparing to other evolution algorithms, these small steps, occasionally large-step and long jumps may increase the accuracy and speed of pollination search significantly in some cases, especially for multimodal, nonlinear problems.

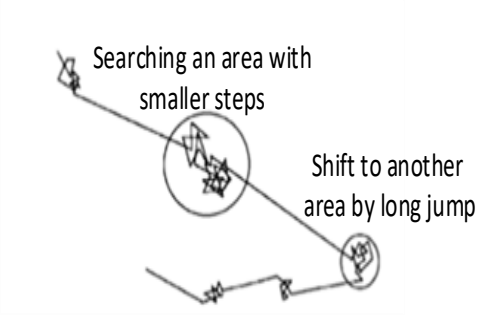


Figure 4. A Levy flight in 2-dimensional plane.

Local pollination is abiotic media self-pollination criteria, which can be expressed as follows,

$$x_i^{t+1} = x_i^t + \varepsilon\left(x_j^t - x_k^t\right) \tag{11}$$

where x_j^t and x_k^t are pollens from different flowers of the t^{th} generation, respectively; Mathematically, if x_j^t and x_k^t come from the same species or selected from the same population, this will become a local random walk if we draw ε from a uniform distribution in [0,1].

Most flower pollination activities can occur at both local and global scale. In practice, adjacent flower patches or flowers in neighbourhood are more likely to be pollinated by local flower pollens than those far away. For this, we can use a switch probability p_o to switch between common global pollination and intensive local pollination. From simulations, we have found that $p_o = 0.8$ works better for most applications. When the random number r uniform distributed between [0,1] is greater than p_o for the global pollination, otherwise for the local pollination.

2.4. System control strategy

Figure 5 shows the micro-inverter control system structure. V_{pv} and I_{pv} are the PV array input voltage and input current, respectively. Sampling the voltage of V_{pv} and the current of I_{pv} is used for MPPT operation. By the logic circuit to generate different duty cycle D_{new} PWM signal to control the first stage power switch S_1, to trick maximum power point. V_g is the grid voltage sampling value. through the software phase-locked loop (SPLL) to get the current reference phase sinΘ; DC bus voltage V_{dc} and bus voltage reference value V_{dref} error value are calculated by the outer ring PI after the current reference amplitude i *, i * and sinΘ to get the reference current i_{ref}; i_g for the inverter output current sampling value. The error of i_{ref} and i_g is calculated by PI calculation and logic circuit. The SPWM signal is used to control the switching of the power at the second stage, and then the current signal with the same frequency and phase as grid voltage is generated [13,14].

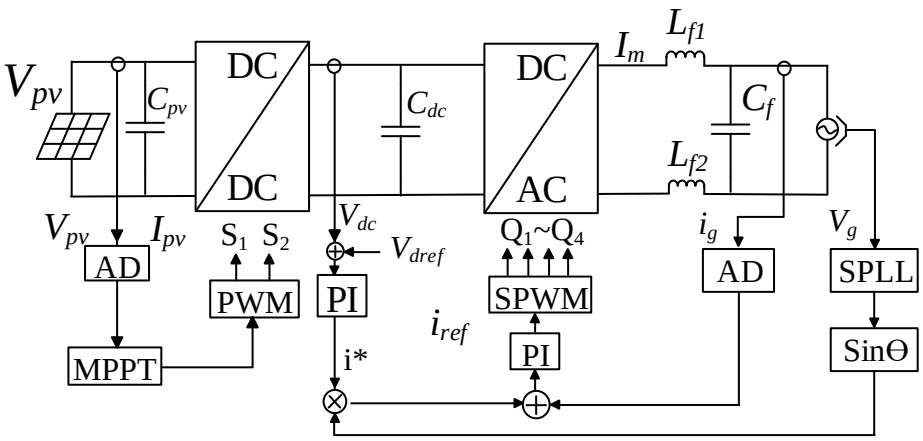


Figure 5. The structure of the control system.

3. Simulation analysis

In order to verify the feasibility of the proposed topology and control strategy, a 3×2 simulated PV array is established based on the SM55 in Matlab/Simulink. The mathematical model of PV array is based on the literature [15]. The parameters of power circuit and the PV array are set in tables 1 and 2, respectively. The ratio between primary and secondary of coupling inductance is 1:2. The switching frequency is 100 kHz and the dead time is 100 ns. The parameters of FPA is set as: p_o = 0.8, n = 4, and termination condition: *Maxgen*=30 or ΔD <0.01. The *H*-bridge adopts unipolar modulation.

Table 1. Parameters of power circuit.

Parameters	value	Parameters	value
Grid voltage V_g/V	220	Input filter capacitor C_{pv}/uF	980
Grid frequency f_g/Hz	50	DC bus capacitor C_{dc}/uF	1320
Switching frequency f_s/kHz	100	Filter inductance L_{f1}/mH	2.5
Coupling inductance L_m/uH	375	Filter inductance L_{f2}/mH	2.5
leakage inductance L_k/ uH	10	Filter capacitor C_f/uF	4.7
Voltage gain capacitor C_1/C_2/uF	2.2/4.4	The clamp capacitor C_c/uF	1

Table 2. Parameters of the PV module and PV array.

Parameters	PV module	PV array
Open voltage V_{oc}/V	21.7	65.1
Operating voltage V_{mp}/V	17.4	52.2
Short-circuit current I_{sc}/A	3.40	6.80
Operating current I_{mp}/A	3.16	6.32
Peak power P_{mp}/W	55	330

Note: the parameters in the table are measured under STC with irradiance 1000W/m^2 and temperature 25℃, AM 1.5.

Under the input voltage of 40 V and the duty ratio of 60%, the output voltage of the proposed DC-DC converter reaches 325 V, while that of the traditional boost [16] is 100 V. The DC-DC voltage gain of the proposed and traditional boost is shown in figures 6 and 7, respectively. The voltage gain of the proposed topology is 8.125, while that of the traditional boost is only 2.5, which verifies the

proposed DC-DC converter with high voltage gain performance.

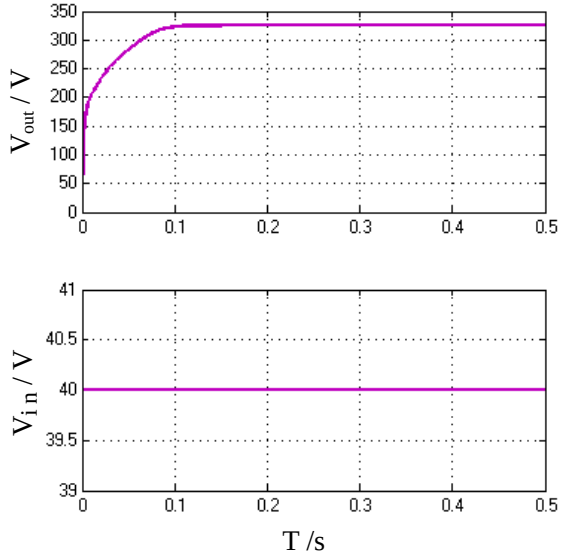


Figure 6. The proposed DC-DC voltage gain.

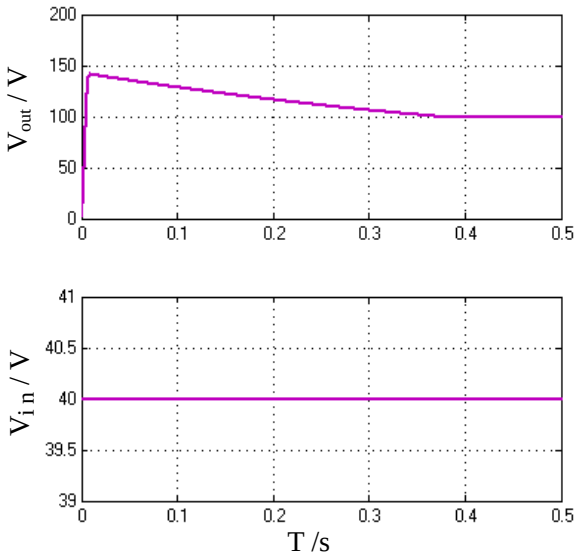


Figure 7. The traditional boost DC-DC voltage gain.

To verify the performance of the MPPT, the PV array is simulated under STC with partial shading. The MPPT control process is shown in figure 8. The proposed approach is tracking for the MPP from t=0 s to 0.6 s. The FPA algorithm generates a different number of flower pollens during which corresponds to different duty cycles during this period. Therefore, we can see the voltage and power of PV array output gradually increased, accompanying with the slightly drop of PV array output current. The maximum power point is tracked at about 1.2 s and the output power is 280 W. DC bus voltage in the 1.2 s is stable at 400 V. At 0.6 s the system is successful in connecting the power grid, also the output current and grid voltage achieve the same frequency in phase, seen in figure 9.

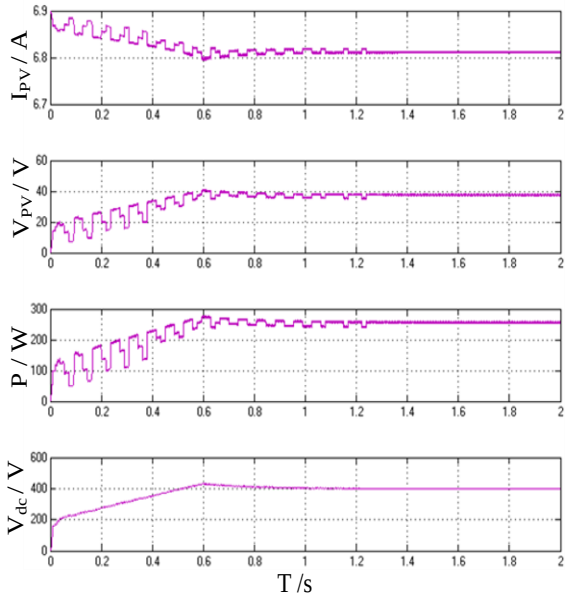


Figure 8. MPPT tracking process.

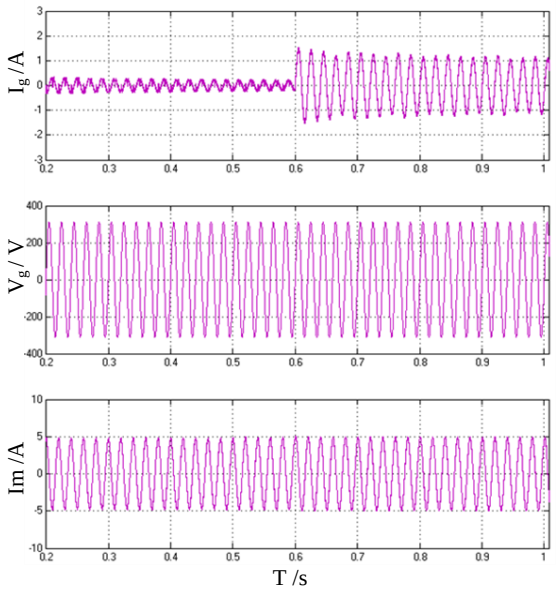


Figure 9. Grid connection process.

4. Conclusions

In this paper, we propose a two-stage PV grid-connected micro-inverter topology and control strategy. In the first stage, the working principle of high voltage gain DC-DC circuit based on coupled inductor, active clamp and voltage multiplier is analysed, and the condition of high efficiency is realized by suppressing the reverse recovery of diode and applying the technology of zero-voltage switching. Furthermore, the global flower pollination algorithm is adopted to improve the efficiency of photovoltaic array, and the simulate results verify the feasibility of the above scheme. In the second stage, the *H*-bridge topology is adopted, and the software phase lock, outer voltage loop and inner current loop are taken as control strategy. Finally, it has realized the global MPPT, high-boosting voltage gain and produced an output current that has a shape similar to a sinusoidal waveform in phase with the grid voltage.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant No. 61574038 and Grant No. 31300473), the Science Foundation of Fujian Education Department (Grant No. JAT160073), the Science Foundation of Fujian Science & Technology Department (Grant No. 2015H0021 and Grant No. 2015J05124), and the Scientific Research Foundation for the Returned Overseas Chinese Scholars, State Education Ministry (Grant No. LXKQ201504).

References

[1] Sher H A and Addoweesh K E 2012 Micro-inverters-Promising solutions in solar photovoltaics Energy for Sust Dev **16** 389-400
[2] Tan K S F, Rahim N A, Hew W P, *et al* 2014 Comparison and analysis of single-phase transformerless grid-connected PV inverters IEEE Trans Pow Electr **29** 5358-69
[3] Jiang S, Cao D, Li Y, *et al* 2012 Grid-connected boost-half-bridge photovoltaic microinverter system using repetitive current control and maximum power point tracking IEEE Trans Pow Electr **27** 4711-22
[4] Islam M, Mekhilef S and Hasan M 2015 Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review Renew Sust Energ Rev **45** 69-86
[5] Hassaine L, OLias E, Quintero J, *et al* 2014 Overview of power inverter topologies and control structures for grid connected photovoltaic systems Renew Sust Energ Rev **30** 796-807
[6] Hasan R, Mekhilef S, Seyedmahmoudian M, *et al* 2017 Grid-connected isolated PV microinverters: A review Renew Sust Energ Rev **67** 1065-80
[7] Ahmad Z and Singh S N 2017 Comparative analysis of single phase transformerless inverter topologies for grid connected PV system Sol Energy **149** 245-71
[8] Cha W J, Kwon J M and Kwon B H 2016 Highly efficient step-up dc–dc converter for photovoltaic micro-inverter Sol Energy **135** 14-21
[9] Li W and He X 2011 Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications IEEE Trans Ind Electron **58** 1239-50
[10] Kandemir E, Cetin N S and Borekci S 2017 A comprehensive overview of maximum power extraction methods for PV systems Renew Sust Energ Rev **78** 93-112
[11] Yang X S 2012 Flower pollination algorithm for global optimization International Conference on Unconventional Computation and Natural Computation **7445** 240-9
[12] Alam D F, Yousri D A and Eteiba M B 2015 Flower pollination algorithm based solar PV parameter estimation Energ Convers Manage **101** 410-22
[13] Petreuş D, Daraban S, Ciocan I, *et al* 2013 Low cost single stage micro-inverter with MPPT for grid connected applications Sol Energy **92** 241-55
[14] Oncu S and Karafil A 2017 Pulse density modulation controlled converter for PV systems International Journal of Hydrogen Energy **42** 17823-30
[15] Shell S M 55 Photovoltaic solar module http://www.aeet-service.com/pdf/shell/Shell-Solar_SM55.pdf

[16] Hasaneen B M and Mohammed A A E 2008 Design and simulation of DC/DC boost converter Power System Conference 12th International Middle-East IEEE pp 335-40