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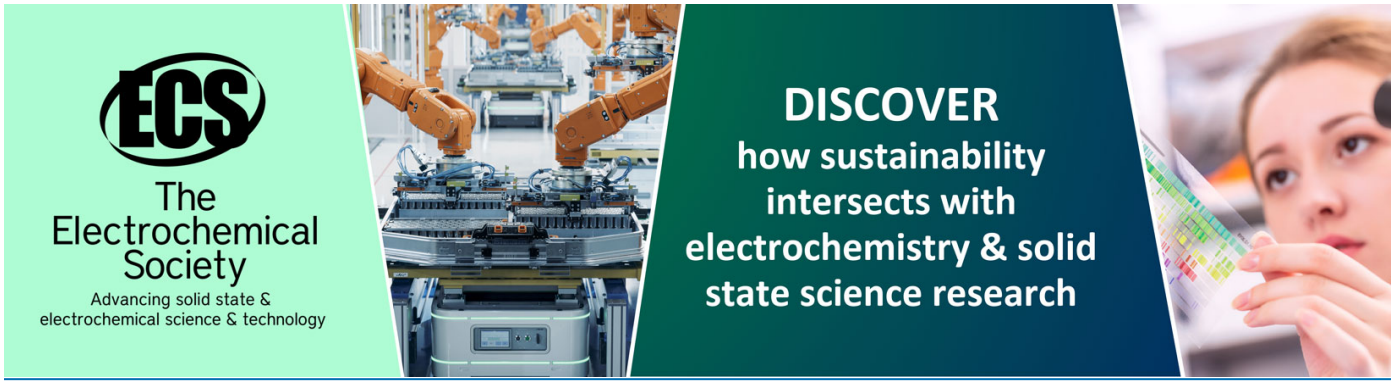

Comparison on modulation schemes for 15-level cascaded H-bridge multilevel inverter

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Abstract. In series with each other, the cascaded H-bridge multilevel inverter (CHML) could apply same or different DC bus voltage. By modifying the isolated DC voltage supplies of a traditional 7-level 3H-bridge inverter with voltage ratio 4:2:1, the proposed inverter outputs a near-sinusoid, 15-level resoluted, stepped voltage with low distortion. The pros and cons of different modulation schemes including PWM, staircase modulation and hybrid PWM are analyzed on switching losses, low order harmonics and THD, which are then verified by Saber simulation.

1. Introduction

Comparing to one full bridge inverter, the cascaded H-bridge multilevel (CHML) inverter which consists of individual DC supplies supported H-bridge modules [1] can provide relatively high resolution, near-sinusoid stepped-voltage, hence reduces the output voltage harmonics [2,3] and become a preference in large power and high voltage field.

More voltage levels brings higher cost on devices, including the topologies with neutral point clamped PWM inverter [4-7] and flying-capacitor [8-14], and also brings higher complexity to the implementations of the inverters [15].

Simply change the voltages of isolated DC voltage sources to some unequal ratio such as 9:3:1 or 4:2:1, the traditional CHML inverter is then modified into a hybrid CHML inverter, with more output voltage levels [16], and more voltage levels then leads to closer sinusoidal output voltage, which at last reduces the THD of output voltage without adding any additional costs. Due to the advantages above, tremendous power electronics devices have applied the hybrid CHML inverter including intelligent transformer [17], battery energy storage systems [18], electric vehicle [19,20], Static Var Compensator (SVC), Active Power Filter (APF) [21] and distribution generation [22].

Different modulation methods including staircase modulation, Pulse-Width Modulation (PWM) and hybrid PWM are applied on hybrid CHML inverter. Different voltage levels including 5, 7 and 9 are discussed by applying PWM, staircase modulation and hybrid PWM with voltages of isolated DC voltage sources changed [23,24], staircase and hybrid PWM are applied with source voltage ratio 8:4:2:1, hence produces a 31 voltage levels output [15].

The control strategy mentioned above is to make the output voltage closer to sinusoid to reduce the harmonics, however some researchers applied harmonic elimination strategy [25-28] on tremendous

topologies with all attemptions on DC voltage ratios [25]. In [3], an efficient multilevel-synthesis approach is made with voltage ration 9:3:1, which is realized by different turns in a transformer. However, such a complicated transformer would increase the device cost and the power losses as well.

In this paper, PWM, staircase, and hybrid PWM modulation are applied on a 15-level hybrid CHML inverter, with the voltage ratio of isolated DC power sources 4:2:1. The comparison on harmonics with frequency under 40 kHz, THD and the power losses due to the high switching frequency are made according to Saber simulation. As result, one can choose the suitable modulation scheme for specific need on THD, filter design and heat sink.

2. Topology and modulation schemes of the proposed h-bridge multilevel inverter

The 3 H-bridge traditional inverter with isolated DC voltage sources 1:1:1 is shown in figure 1(a) [1], which produces 7 voltage levels in per unit (Vpu), including -3Vpu, -2Vpu, -1Vpu, 0Vpu, 1Vpu, 2Vpu, 3Vpu, by controlling the IGBTs of the inverter.

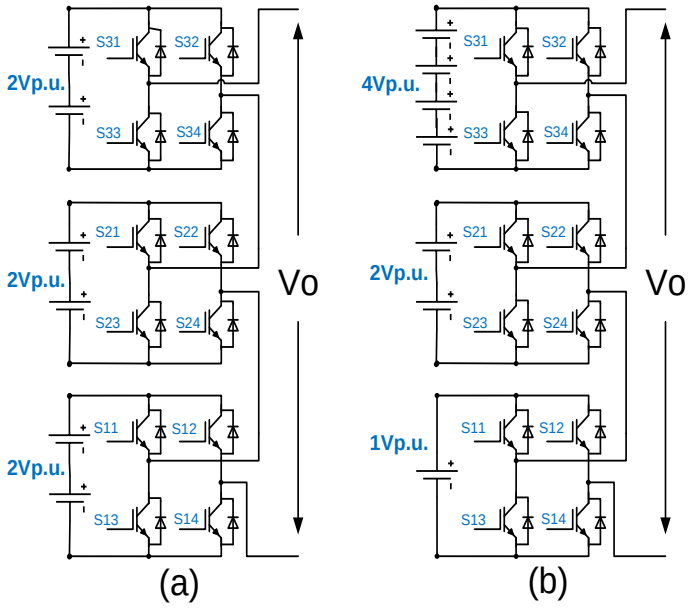

Figure 1. (a) Traditional 1:1:1 CHML inverter (b) Hybrid 4:2:1 CHML inverter.

Figure 1(b) shows the schematic diagram of a hybrid 15-level inverter which modifies the isolated DC voltage sources 4:2:1, resulting 15 output voltage levels from -7Vpu to 7Vpu.

Comparing to the traditional 7-level inverter, the proposed one can reduce the cost by introducing lower switching frequency switches, reduce the harmonics by introducing more voltage levels, and reduce the size and power loss of filter. However, the large number of voltage levels will make the control of inverter more complex, and high frequency switches will bring more switching losses and reduce the lives of switching components.

Table 1 shows the switching patterns that forms the voltage levels from -7Vpu to 7Vpu. The isolated DC voltage sources are mainly batteries and capacitors which is usually forbidden to connect with opposite polarities, such as connecting +4Vpu and -1Vpu to get +3Vpu [3], hence protect the batteries and capacitors from damage.

The inverter can operate in both staircase mode [29], PWM mode and hybrid PWM mode [30,31]. The hybrid PWM mode combines the staircase modulation on 4Vpu module and 2Vpu module and PWM on 1Vpu module, hence the switching losses of 4Vpu module and 2Vpu module will be much lower as well as the total switching losses, although the switching losses of 1Vpu module will be higher.

Table 1. Patterns of fifteen voltage levels.

V(pu)	Patterns	V(pu)	Patterns
7	+1+2+4	-7	-1-2-4
6	+2+4	-6	-2-4
5	+1+4	-5	-1-4
4	+4	-4	-4
3	+1+2	-3	-1-2
2	+2	-2	-2
1	+1	-1	-1
0	0	0	0

To apply PWM scheme on 7-level or 15-level CHML inverter, the traditional method is to introduce 7 or 15 carrier signals with horizontal or vertical shifts [32-34]. The high switching frequency due to the PWM leads to near sinusoidal output voltage with high order harmonics which can be attenuated by small size filter, as well as high switching losses. Moreover, 7 or 15 carrier signals will add up the complexity of the control method.

To apply staircase modulation scheme on 7-level or 15-level CHML inverter, one sinusoidal modulating wave is needed to be divide into 7 zones or 15 zones, then the switching patterns and switching angles for each zone is calculated and listed for digital implementation, as shown in figure 2.

In figure 2, the staircase voltage consisted of 4Vpu, 2Vpu and 1Vpu modules are marked with switching angles from θ_1 to θ_{30}. The switching angles from θ_1 to θ_{30} for the 4 IGBTs in a single H-bridge such as 1Vpu module are S11, S12, S13 and S14, and however can be shared with all IGBTs in 4Vpu, 2Vpu and 1Vpu modules. For instance, 2Vpu H-bridge share the switching angles θ_2, θ_4 and θ_6 with the modulation results of 1Vpu H-bridge. Advanced algorithm can be applied on the switching angles [35,36], sequential switching hybrid single-carrier sinusoidal modulation [37,38].

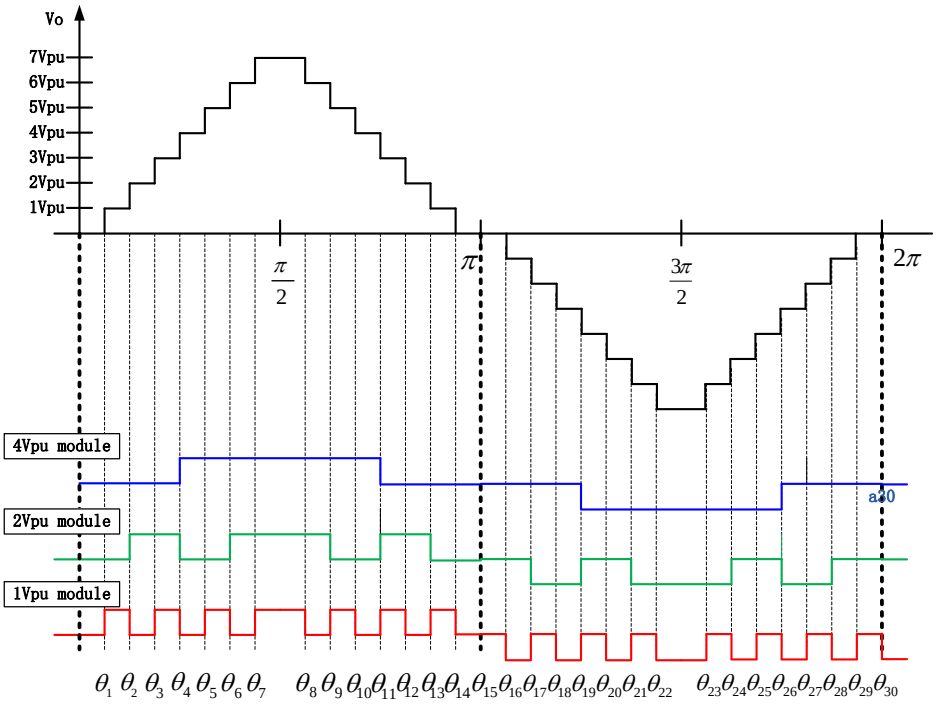

Figure 2. Stepped output voltage of 4Vpu, 2Vpu and 1Vpu modules.

The frequency for 4Vpu, 2Vpu and 1Vpu modules in figure 2 can be calculated as:

$$f_{sw} = f_0 \times \left(2^{S+1} - 1\right) \tag{1}$$

where f_0 is 50 Hz, *S* equals to 4, 2 and 1 for 4Vpu, 2Vpu and 1Vpu modules.

The IGBT switching frequency of 4Vpu, 2Vpu and 1Vpu modules calculated by (1) are 150 Hz, 350 Hz, and 750 Hz respectively. The high isolated DC source voltage such as 4Vpu module works at the lower switching frequency which reduces the electromagnetic interference (EMI) and total switching losses [39].

Table 2. Stresses for different topologies.

Topologies	Modules	Voltage stress	Current stress	Switching frequency
Traditional 7-level CHML inverter	2.3Vp.u. modules	2.3Vp.u.	1Ap.u.	1 kHz-10 kHz
Hybrid 15-level CHML inverter	4Vp.u. module	4Vp.u.	1Ap.u.	150 Hz
	1Vp.u. module	1Vp.u.	1Ap.u.	750 Hz

The comparison on voltage stress, current stress and switching frequency for traditional CHML inverter and hybrid CHML inverter which both provide a 7Vpu (3*2.3Vpu and 4Vpu+2Vpu+1Vpu) amplitude output voltage is shown in table 2. It can be seen from figure 2 that the current stresses are the same due to the cascaded connection, and voltage stresses equal to isolated DC source voltage. The switching frequency of hybrid 15-level CHML inverter does not exceed 1 kHz, hence reduces the switching losses and cost on switching components [39].

The staircase voltage shown in figure 2 is defined in Fourier series expansion as:

$$Vo(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi}(\cos(n\theta_1)) + (\cos(n\theta_2)) + \cdots + \cos(n\theta_m))\sin(n\omega t) \tag{2}$$

where *n* is up to 50 which represents the harmonic order, *m* equals to 7 for 15 voltage levels which represents switching angle numbers.

The switching angles of IGBTs are given by:

$$\theta_n = \arcsin\frac{(n-1)+k}{j+k} \tag{3}$$

where *n* represents the triggering signal sequence, *j* equals to 7 for 15 voltage levels which represents switching angle numbers, and *k* is an additional coefficient to preserve more voltage levels when modulation index is low, which can by calculated by:

$$M = \frac{V_1}{m \times \frac{4Vdc}{\pi}} \tag{4}$$

where V_1 is the amplitude of the fundamental voltage, and equals to 7 for 15 voltage levels which represents switching angle numbers.

The THD can be calculated as:

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=3,5,7}^{\infty} V_n^2} \tag{5}$$

where V_1 and V_n can be calculated from (2) by:

$$V_1 = \frac{4Vdc}{\pi}(\cos(\theta_1)) + (\cos(\theta_2)) + \cdots + \cos(\theta_7)) \tag{6}$$

$$V_n = \sum_{n=3,5,7}^{m} \frac{4Vdc}{n\pi}(\cos(n\theta_1)) + (\cos(n\theta_2)) + \cdots + \cos(n\theta_7)) \tag{7}$$

By introducing coefficient *k*, the THD of the output voltage shown in figure 3 decrease from 6.8% to 4.7%, when coefficient *k* increase from 0 (*k=0* means without coefficient *k*) to 0.5, make it lower than the upper limit of the IEEE Std 519-1992 (5%) [38] without any filter.

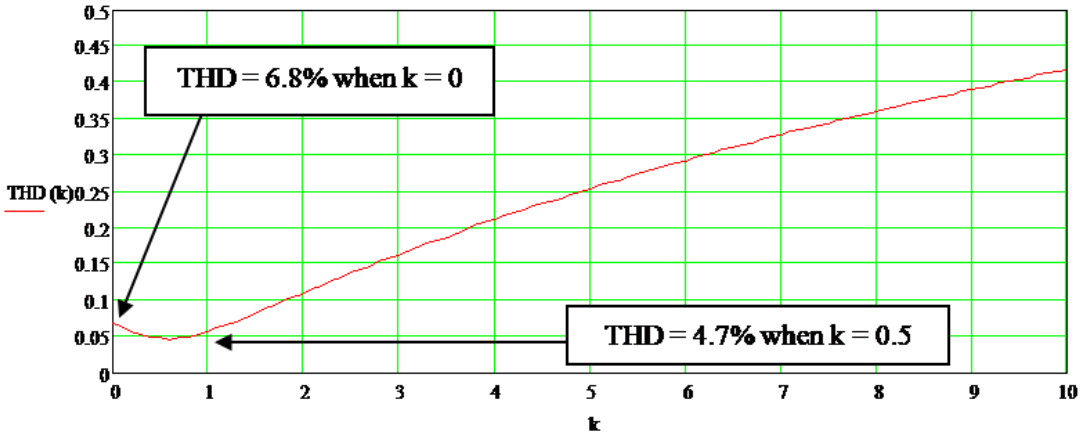

Figure 3. THD of the output voltage with coefficient k.

3. Simulation verification

The simulation on the proposed 1:1:1 CHML inverter and 4:2:1 CHML inverter is performed in Saber simulation, and the specification of the system are listed below:

Hybird 15-level inverter DC source voltage 1: 100 V.
Hybird 15-level inverter DC source voltage 2: 50 V.
Hybird 15-level inverter DC source voltage 3: 25 V.
Tranditional 7-level inverter DC source voltage: 60 V.
Resistance of the load: 46 ohm.

3.1. PWM for Tranditional 7-level CHML inverter

In order to apply PWM on a 7-level CHML inverter, 7 zones from a standard sinusoidal wave has been divided in magnitude for 7 different switching patterns. The controller chooses the corresponding switching patterns according to the sampling result on standard sinusoidal wave, and then calculated the duty cycle time for the amplitude of the output voltage.

The turn-on time T_{on} for the IGBT in the simulation can be given by:

$$T_{on} = \frac{V_{ref} - V_{low}}{(V_{high} - V_{low}) \times f_{samp}} \tag{8}$$

where the V_{ref} is the standard sinusoidal modulating voltage, V_{high} and V_{low} are 2 voltages from 2

different switching patterns in the pulse of the output voltage, and f_{samp} represents the sampling frequency.

The PWM-staircase output voltage as well as a standard sinusoidal wave are shown in figure 4, whose THD is 29% with FFT analysis form the Saber simulation.

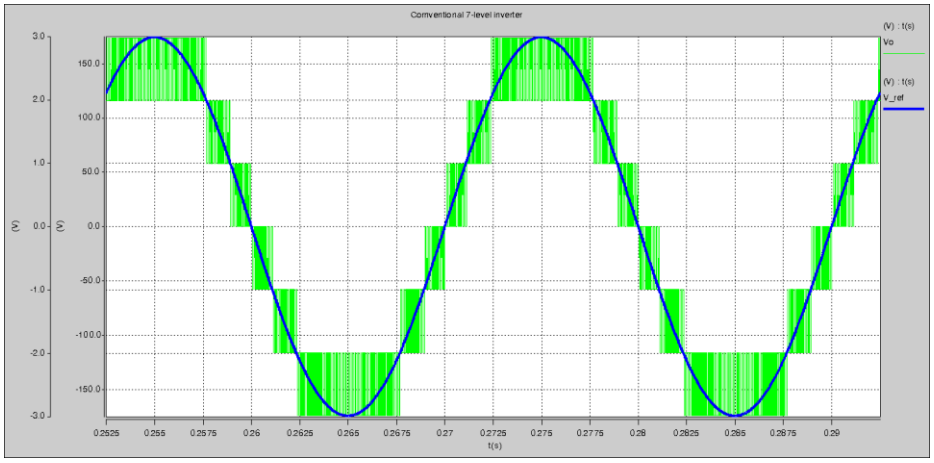

Figure 4. Simulation results of stepped output voltage waveform for traditonal 7-level CHML inverter.

3.2. Staircase modulation for hybrid 15-level CHML inverter

By applying staircase modulation on a 15-level CHML inverter, a stepped output voltage with peak point 175 V is shown in figure 5 according the switching patterns in table 1.

The THD of the stepped output voltage can be calculated by the Saber simulation software with FFT analysis as 5.43% when no filter is included in the simulation circuit in figure 1(a), hence the switching losses will be reduced.

The THD calculated by MathCAD software is lower than the one in the simulation, as no dead zone, even harmonics, and asymmetry waveform caused by sampling frequency are considered.

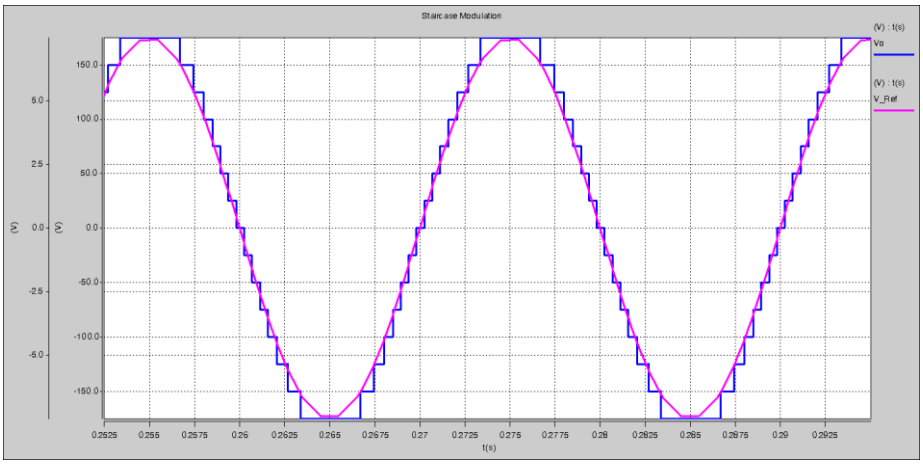

Figure 5. Simulation results of output voltage waveform for staircase modulation scheme.

3.3. PWM for hybrid 15-level CHML inverter

In order to apply PWM on a 15-level CHML inverter, 15 zones from a standard sinusoidal wave has been divided in magnitude for 15 different switching patterns. The controller chooses the corresponding switching patterns according to the sampling result on standard sinusoidal wave, and then (8) is applied on calculating the duty cycle time for the amplitude of the output voltage.

The 15-level PWM-staircase output voltage as well as a standard sinusoidal wave are shown in figure 6, whose THD is 7.75% with FFT analysis form the Saber simulation.

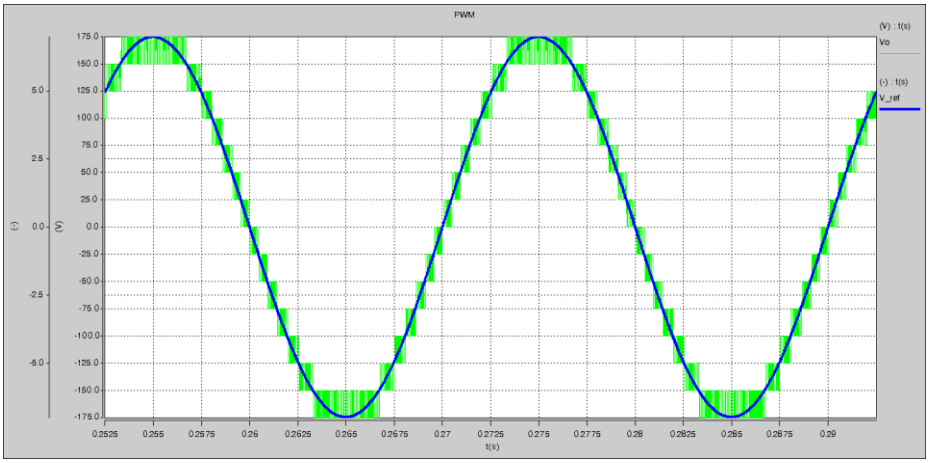

Figure 6. Stepped PWM output voltage waveform.

3.4. Hybrid PWM for hybrid 15-level CHML inverter

To introduce hybrid PWM scheme for 15-level CHML inverter, both PWM and staircase modulation scheme are applied. The PWM scheme is applied on 1Vpu module and staircase modulation scheme is applied on 2Vpu and 4Vpu modules with switching frequency 16 kHz, 350 Hz and 150 Hz, respectively.

The staircase-PWM mixed output voltage is shown in figure 7, whose THD is 7.4%. As a result, the THD of output voltage is reduced by 0.3%, hence the switching losses of 2Vpu and 4Vpu modules will be reduced too.

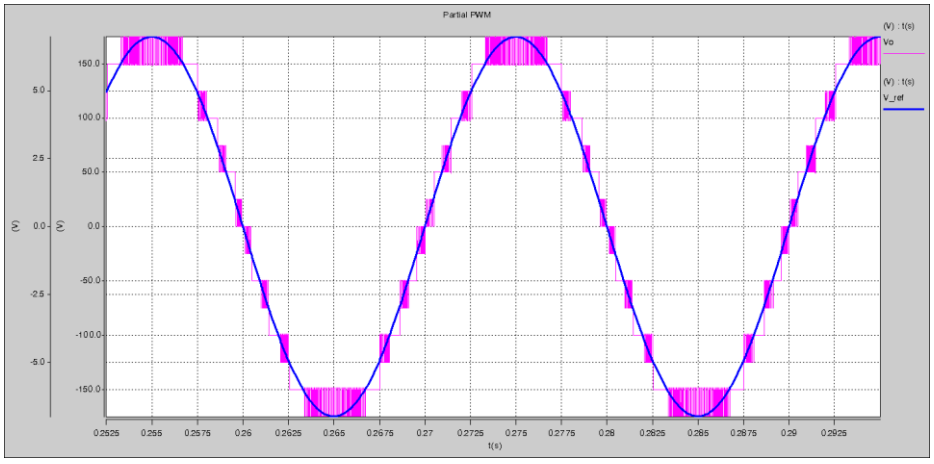

Figure 7. Simulation results of output voltage in hybrid PWM scheme.

Figure 8 illustrates the harmonics spectrums for 7-level CHML inverter output voltage in PWM scheme and 15-level CHML inverter output voltage in PWM scheme, staircase modulation scheme and hybrid PWM scheme.

It can be seen from figure 8 that the magnitude of harmonic voltages for 7-level CHML inverter is the highest, and the ones for 15-level CHML inverter in 3 different modulation schemes which up to 2.5 kHz harmonics are considered.

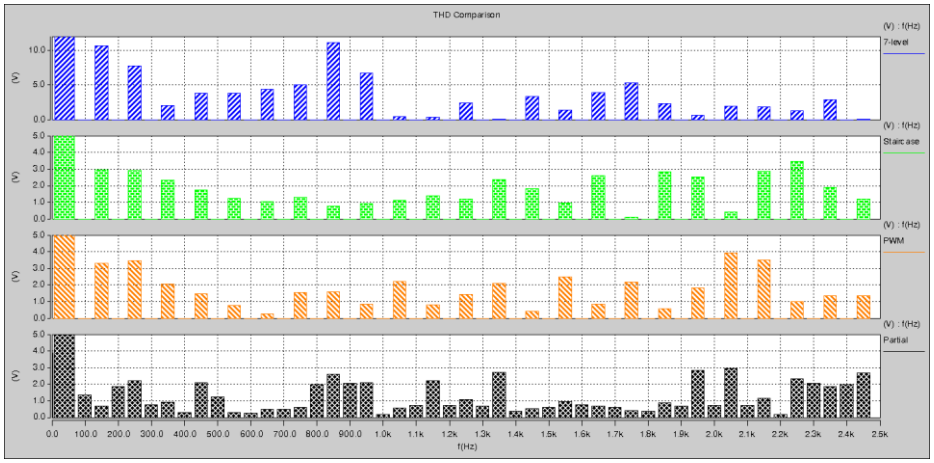

Figure 8. Harmonic spectrums for 7-level and 15 level CHML inverters in PWM, staircase, and hybrid PWM schemes.

The comparison among 4 simulation results illustrated in table 3 shows that the THD for 15-level CHML inverter in staircase modulation is the lowest however with the largest filter size as it has the largest low-order harmonics, and the one in PWM scheme is the highest however with the smallest filter size as it has the smallest low-order harmonics. As a result, the hybrid PWM scheme with small output voltage THD, reduced filter size and low switching losses combines the advantages of other modulation scheme and can be applied in tremendous applications by fulfilling most of the requirements in harmonics, filter size and switching losses.

Table 3. Pros and cons of 4 modulation schemes.

Modulation schemes	Switching losses	Low-order harmonics	THD
7-level PWM	Highest	Highest	Highest
15-level staircase	Low	High	Low
15-level PWM	High	Low	High
15-level hybrid PWM	Medium	Medium	Medium

4. Conclusions

The PWM, staircase modulation, and hybrid PWM schemes are applied on a hybrid 15-level cascaded H-bridge multilevel inverter which is modified from a 7-level cascaded H-bridge multilevel inverter by changing its isolated DC source voltage ratio from 1:1:1 to 4:2:1.

The proposed modulation schemes provide low THD, near sinusoidal output voltage with different low-order harmonics, THD and switching losses which are then verified by Saber simulation.

Without considering the output filter, PWM scheme provides an output voltage with the highest THD and switching losses as well as the lowest low-order harmonics which results in small size filter, and staircase modulation scheme provides an output voltage with the lowest THD and switching losses as well as the highest low-order harmonics which results in large size filter. The hybrid PWM scheme combines the advantages of those two modulation schemes in low-order harmonics, THD and switching losses which fits most of the applications.

Acknowledgments

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