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Life-cycle assessment of computational logic produced from 1995 through 2010

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Abstract
Determination of the life-cycle environmental and human health impacts of semiconductor logic is essential to a better understanding of the role information technology can play in achieving energy efficiency or global warming potential reduction goals. This study provides a life-cycle assessment for digital logic chips over seven technology generations, spanning from 1995 through 2010. Environmental indicators include global warming potential, acidification, eutrophication, ground-level ozone (smog) formation, potential human cancer and non-cancer health effects, ecotoxicity and water use. While impacts per device area related to fabrication infrastructure and use-phase electricity have increased steadily, those due to transportation and fabrication direct emissions have fallen as a result of changes in process technology, device and wafer sizes and yields over the generations. Electricity, particularly in the use phase, and direct emissions from fabrication are the most important contributors to life-cycle impacts. Despite the large quantities of water used in fabrication, across the life cycle, the largest fraction of water is consumed in generation of electricity for use-phase power. Reducing power consumption in the use phase is the most effective way to limit impacts, particularly for the more recent generations of logic.

1. Introduction

The complementary metal oxide semiconductor (CMOS) transistor structure is the most common form of digital logic used in electronics today. This letter presents a life-cycle assessment (LCA) for generic CMOS logic at each technology node over a 15 year period, from the 1995-era 350 nm node to the 45 nm node, which will enter large scale production in 2010. The purpose of this article is to provide a detailed, complete, transparent and accurate inventory of the environmental impacts of many generations of logic chips in order to investigate trends in emissions over time and to allow LCA practitioners to more accurately model electronic equipment, as well as services enabled by electronics. Previous published work in the area of semiconductor LCA has included four environmental impact studies from industry [1–4] which report impacts for wafer fabrication and, in some cases, also the use and production of materials. Most do not include impacts associated with the production of facility infrastructure or process chemicals (aka 'upstream' impacts). Possibly because

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these reports have all been conference papers supported by spoken presentations, they lack complete explanation of data collection methodologies and do not report complete inventory data. None of these studies mention the use of measurement to determine the mass of emissions from the fabrication facility but rather use estimation methods or do not explain whether or how they account for facility emissions. These studies also do not report data uncertainty or discuss the influence of data uncertainty on results. Several researchers have noted that the lack of LCA data for semiconductor devices is a stumbling block in LCA of electronics, and that there is particular need for more complete or transparent LCA of semiconductors [5–11]. Academic work related to semiconductor LCA includes a study from Murphy which presents a methodology for parametric semiconductor life-cycle inventory (LCI) models based on process specifications [7]. Williams has reported energy consumption in logic manufacturing [12] and created an LCA of a memory chip, using both economic-level data and data provided from anonymous industrial contributors, and highlights the importance of upstream impacts and the need for more accurate LCI data for high purity chemicals [8, 13, 14]. Plepys also underscores the need for accounting of the life-cycle stages preceding wafer fabrication in semiconductor LCA [5, 6]. In an earlier paper, Plepys explored a rebound effect in information and communication technology (ICT) consumption, analogous to the rebound effect of dropping energy prices, whereby advancing technology incites the need for ever faster and more powerful ICT and counteracts the environmental efficiencies of technology advancement [15]. A more recent paper from Williams re-introduces this topic with an examination of different functional units in semiconductor LCA [12], and the discussion of functional unit choice is continued in this letter.

In this study, the issues with industry-reported LCA studies described above are addressed. Material demands and emissions have been determined using Fourier transform infrared and mass spectrometric measurement of process inputs, chamber emissions and post-point-of-use abatement emissions. Upstream impacts associated with fabrication facility (fab) infrastructure and process chemicals, as well as water supply are included. The uncertainty associated with each type of data is reported and the sensitivity of results to uncertainty and changes in model parameters is evaluated. Methodology, model assumptions, and inventory data are stated so that the study is transparent, reproducible and adaptable so as to be useful in downstream LCA of electronics. By presenting LCA data for many generations of logic, different types of electronics may be modeled. Chips at the 350 nm node (first produced in volume in 1995) are still currently used in embedded logic for appliances and toys, while an average new personal computer purchased today would contain 65 nm logic. The term 'technology node' and the measurements of 350–45 nm refer to the half-width of the first interconnect layer associated with memory of a given technology generation, and are used as shorthand for relative transistor sizes [16].

2. Methods

These life-cycle inventories (LCIs) describe a production scenario with wafer manufacturing in Santa Clara, California, using chemicals, equipment and construction materials produced in the US. 'Back-end' operations (die packaging and testing) are located 3000 miles away. The inventory is a hybrid model, containing primarily process data, supplemented by economic input–output LCA (EIO-LCA) data from the Carnegie Mellon database [17] where process data are unavailable. The functional unit of the study is one die over a lifetime of 6000 h, though data are provided in the supporting information (available at stacks.iop.org/ERL/5/014011/mmedia) to re-evaluate these results for a different use-phase chip power or lifetime and to allow normalization by computational power or number of transistors.

The functional unit drastically alters how the life-cycle impacts of semiconductors appear and there are arguments for every option of functional unit: an average device, a certain device area, a metric of computational power or a given number of transistors. The natural first choice is a measure of computational power, such as one million transistors, because this seems to reflect a constant functionality. However, the functionality of one million transistors has decreased over time, as the average personal computer has required increasing computational power to serve roughly the same purposes over the past 15 years. Presenting impacts per million transistors shows dramatic decreases in impacts over time which do not match real-world dynamics [15, 18] as, for example, one million transistors today do not provide the same functionality as a decade ago in personal computing applications. Because this study spans a fifteen year period, results reported per million transistors would exhibit misleading trends. The functional unit of an average-sized personal computer (PC) central processor for each year reflects a set functionality over time because this unit serves the same product function within its corresponding timeframe. The functional unit used in this study is thus one average-sized die, as defined for cost-performance CMOS logic by the International Technology Roadmap for Semiconductors (ITRS) [16] but these results may also be adapted to represent any CMOS logic-based chip, if the chip size or number of transistors is known.

The LCIs for wafer production are built on a set of process, device and fab spreadsheet models. Each process model represents one process step (e.g., chemical vapor deposition) with a set of energy and mass flows per wafer into and out of the manufacturing equipment, based on measurements taken at the process chamber inlet, chamber outlet and post-point-of-use (POU) abatement. Each device model defines the device size, wafer size and typical yield for the device's technology generation as well as the process flow—the order and number of process steps used to make the device. Chip sizes and yield models are those developed through ITRS [16]. Each fab model represents all of the infrastructure and fab facility systems beyond the process tools and POU abatement equipment, which are characteristic to each technology node. The energy and resource demands for each fab model are based

on the capacity of its facility systems, which change with wafer size, as well as the demands for utility nitrogen, process cooling water, industrial city water and abatement chemicals, as determined by the process flow at each technology node. The fab models also reflect technology and operational changes which have resulted in facility energy efficiency improvements over the last fifteen years.

These LCIs represent the impacts associated with all life-cycle stages, though data for end-of-life effects are limited. Studies of end-of-life electronics have measured the end effects of computer disposal which largely represent emissions (dioxins, brominated flame retardants, etc) from the breakdown or combustion of a computer's more massive components. In this study, EOL impacts include only the lead emissions from wire-bonding solder contained inside the packaged chip. EOL lead emissions stop at 2006, when the Restriction on Hazardous Substances regulation banned lead containing solders. While there may be other harmful emissions from the decomposition of a logic chip, these have not yet been measured exclusively and are not included in the model.

2.1. Manufacturing process power and emissions

The mass flows for each process step, with the exception of lithography and certain thermal steps, have been determined using in-line mass spectrometry and Fourier transform infrared (FT-IR) spectroscopy. (Details of the process models can be found in a previous, related study of an individual chip [19].) Each emission measurement closes mass balance within 10% of chamber or POU abatement system inputs and thus has a maximum uncertainty of $\pm 10\%$. Process equipment power consumptions are based on measurements taken at Applied Materials which have an associated error of $\pm 2.5\%$ [19]. Emissions and power consumption of photolithographic and thermal processes are taken from the process measurements from Murphy [7], supplemented by data from an unpublished academic report from Peterson [20].

2.2. Facility energy efficiency

The techniques used in industry to optimize the sizing and operation of fabs include a long list of practices, including more efficient cleanroom airflow (including the use of mini-environments), reduced clean dry air (CDA) and nitrogen pressures, reduced exhaust system pressures and increased sizing of cooling towers to allow reduced chiller sizes. More information concerning the sizing and design of facility systems in the fab models is given in the supplementary data (available at stacks.iop.org/ERL/5/014011/mmedia).

2.3. Abatement

Both point of use (POU) and central facility abatement systems are included in the model. The central abatement systems in each fab model include a central acid scrubber, an ammonia scrubber, a volatile organic compound (VOC) oxidizer and an acid waste neutralization unit as well as copper CMP and fluoride wastewater treatment systems. The abatement efficiencies of these central systems for gaseous acids,

ammonia and VOCs and are based on measurements published by semiconductor industry members [21–26]. Conversion of liquid waste is calculated based on expected reactions and the pH requirements of effluents to the public water treatment system. Combustion and water scrubbing, plasma oxidation and cold bed adsorption POU systems are associated with certain process steps (see the supplementary data available at stacks.iop.org/ERL/5/014011/mmedia). The abatement efficacies of POU units are taken from pre- and post-POU abatement emissions measurements [19].

2.4. Environmental impact metrics

Environmental effects are characterized using the mid-point impact factors established in the Tool for the Reduction and Assessment of Chemical and other environmental Impacts (TRACI), a program developed by the US EPA. About a third of the TRACI impact factors used in the model are specific to California, and the remaining are representative of the United States in general. All photochemical smog formation impact factors are for California, and some acidification, eutrophication, human health criteria and human non-cancer health impact factors are also California specific. Impacts for ecotoxicity and carcinogenic human health effects are all US general. Because impact factors specific to the location of back-end operations, Costa Rica, are not available, the same factors are used for wafer manufacturing and back-end operations. Global warming potentials are those defined in the 2007 Intergovernmental Panel on Climate Change (IPCC) Fourth Assessment Report [27]. Land use is omitted from the inventory due to a lack of land use data for all life-cycle stages.

2.5. Electricity generation emissions factors and water use

The life-cycle global warming potential (GWP) of electricity from coal, natural gas and large scale hydroelectric and solar are taken from Pacca [28], while that of nuclear power is from Fthenakis [29]. EPA GWP emissions factors are used for geothermal and biomass electricity [30]. For non-greenhouse gases, only direct emissions from Santa Clara's electric utility (Pacific Gas and Electric) are included in the model. Average NO_x, SO_2, and mercury emissions for Pacific Gas and Electric's conventional fuel plants are taken from the EPA's eGrid database [31]. Water consumed in electricity generation is taken as the US average of $1.76 \, l \, kWh^{-1}$ [32].

3. Results and discussion

3.1. Global warming potential

Global warming emissions per die have risen at each successive technology node (figure 1). Use-phase electricity consumption generates the majority of life-cycle GWP impacts at all nodes, with an increasing share over time. Device power in the use phase contributes an average of 75% across all nodes, and 92% at 45 nm. If POU abatement is used for PFC-emitting wafer processes, as assumed for these results, fabrication (including electricity and natural gas use, and direct emissions) emits on average 6% of life-cycle GWP in all years, and 2% at
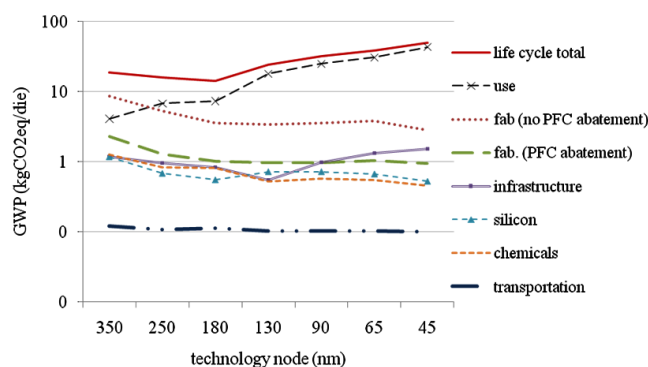
Figure 1. Global warming potential per die by life-cycle stage, over 7 technology nodes.

Figure 3. Smog formation per die by technology node.
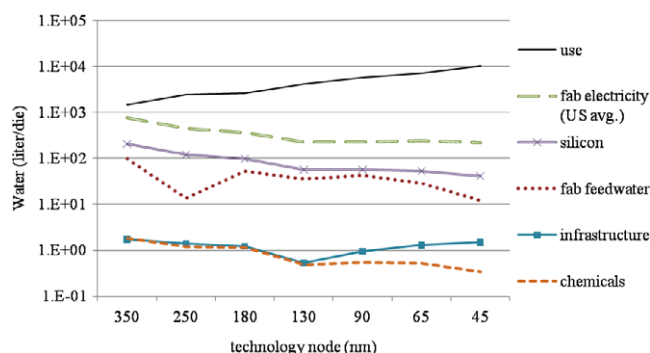

Figure 2. Water use per die, by life-cycle stage, over 7 technology generations.

the most recent generation. (Without PFC abatement, fab emissions are 8–17 times higher and become the second largest origin of GWP after the use phase.) GWP from production of silicon, process chemicals and the facility infrastructure (the fab building and equipment) each account for less than 7% of life-cycle GWP at the 350 nm node, and represent successively smaller fractions in the following years. The sensitivity of life-cycle energy and GWP to production factors has been analyzed in a related paper [18].

3.2. Water use

Life-cycle water consumption is dominated by electricity generation and the overall increase in water use is driven by climbing use-phase power as illustrated in figure 2. Water used in fabrication has fallen significantly per device over the period under study due to a number of changes in wafer processing. At the 130 nm node front-end-of-line (FEOL) photoresist removal steps switch from a wet sulfuric acid hydrogen peroxide mixture (SPM) strip, to a dry plasma process which reduces the number of 'wet' steps (in which the wafer is submerged in an UPW-based solution). As with transportation and fabrication emissions, the switch to 300 mm wafers at the 130 nm node results in a reduction in water use but in this case the process change plays a greater role. Recycling of post-process UPW is not assumed in any of this study's fabs.
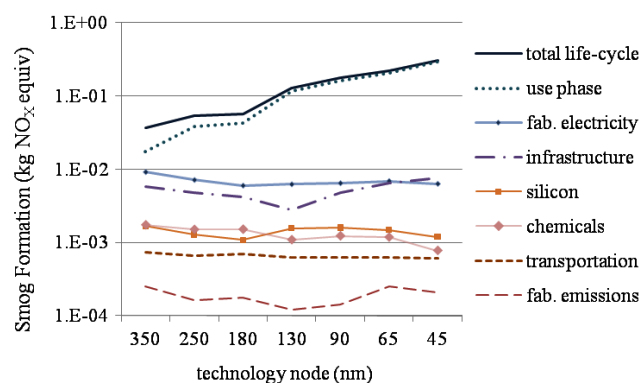
Land use is not included in this study because data concerning the land utilization for processes throughout the life cycle were not attainable, and the land occupied by the fab alone is not sufficiently representative of the entire life cycle.

3.3. Photochemical oxidant formation, acidification and eutrophication impacts via air emissions

Impacts from air emissions in the categories of photochemical oxidant formation (POF), acidification and eutrophication are primarily caused by use-phase electricity. Taking an average across all technology nodes, use-phase electricity is accountable for 81% of smog formation, 80% of acidification and 81% of eutrophication impacts via air, and over 94% of all of these categories at the most recent technology node. Over the generations, impacts related to use-phase electricity have grown due to escalation of device power demand, which is the dominating factor defining the variation over time in POF, acidification, eutrophication and criteria health impacts per die which follow a common pattern, as shown in figures 3 through 6. This common trend results from a number of influencing factors: escalation over time is driven by increases in use-phase electricity as well as a steady rise in the size and complexity of fab infrastructure, while a jump in net die yield causes the countervailing drop in per-die infrastructure, transportation and fabrication emissions at the 130 nm node. (The switch to 300 mm wafers results in a higher number of die harvested from a transported wafer and less transportation wasted on unused wafer area and packaging.)

3.4. Human health impacts

EPA criteria human health impacts are public health damages, measured in disability affected life years (DALY), resulting from particulate matter, NO_x and SO_2 emitted during electricity production and transportation. Over the period of study, use-phase electricity is the cause of an average of 77% of these health impacts. Life-cycle emissions from the fabrication building and equipment account for an average of 12% of criteria health impacts over this 15 year period (figure 6).

Non-cancer human health effects (such as developmental or neurological toxicity) are caused by the lead contained in chips produced before 1996 (350 through 90 nm
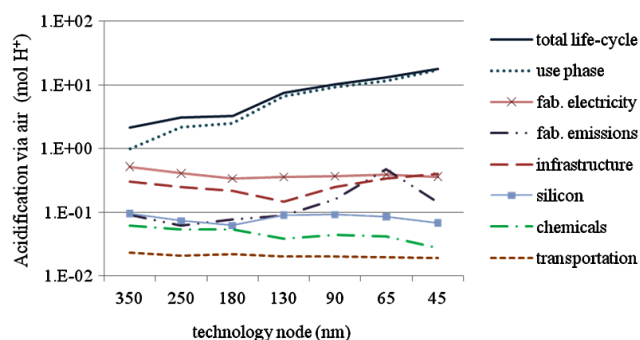
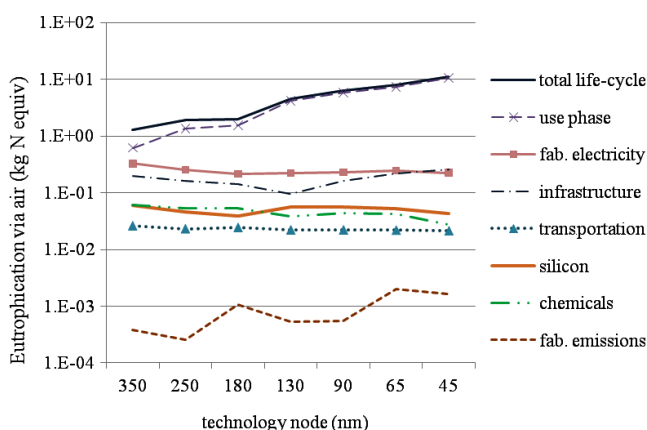**Figure 4.** Acidification per die by technology node.

Figure 7. Human non-cancer health impacts per die by technology node.

Figure 5. Eutrophication via air emissions per die by technology node.
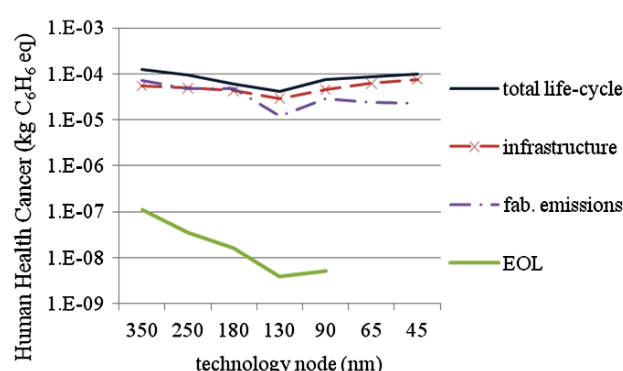
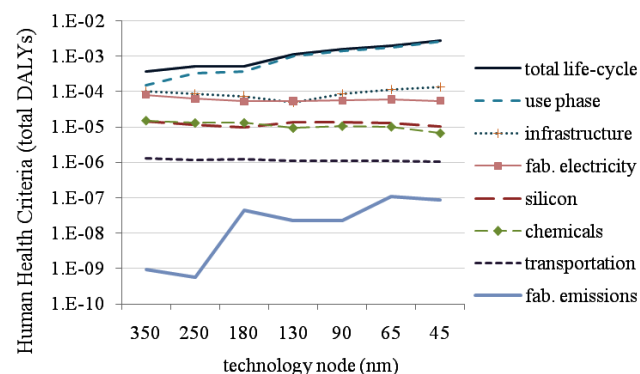**Figure 8.** Human carcinogenic impacts per die by technology node.

Figure 6. EPA criteria human health impacts per die by technology node.

nodes), electricity-related mercury emissions, lead emissions occurring throughout the upstream life cycle of facility infrastructure as well as hydrochloric acid releases to water from wafer fabrication. At the most recent technology generation, 75% of non-cancer human health impacts are caused by use-phase electricity, via mercury emissions, 9% were caused by fab direct emissions, 8% by fab electricity and 7% were due to facility infrastructure (figure 7). HCl vapor is abated with ⩾99% efficiency in the fab scrubber and though liquid HCl is neutralized in the acid waste system with close
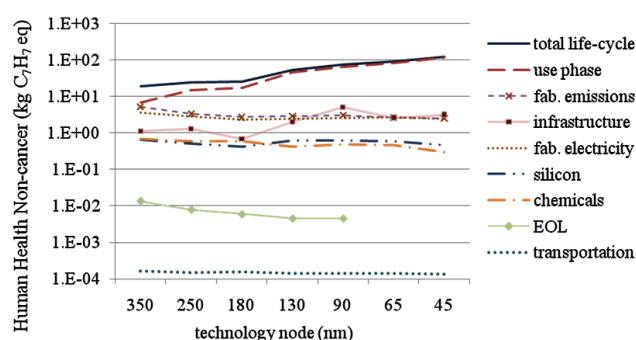
to an equivalent efficacy, a small fraction evades treatment (figure 7). Waterborne fab waste containing HCl flows to the municipal waste treatment system, where its actual impacts are lower than those predicted here.

Human carcinogenicity results from the lead content of the chip disposed at end of life (EOL), as well as lead emitted in production of facility construction and manufacturing equipment and emissions from wafer fabrication. Among the fab emissions, formaldehyde and ammonia are the largest causes of these impacts. The v-shaped trend in impact magnitude over time reflects a decrease in fab-related emissions per die, due to yield improvements, combined with a steady increase in the size of the fab building and quantity of manufacturing equipment (figure 8).

Ecotoxicity impacts are largely due to airborne mercury emitted during electricity generation. EPA data for plants operated by Pacific gas and electric are estimated to emit 0.0038 g of mercury per MWh of electricity produced. The trend in ecotoxic impacts over time is influenced by that of life-cycle electricity demand (figure 9). Fabrication emissions in the form of waterborne copper waste from die packaging and copper chemical mechanical polishing (CMP) account for less than 1% of ecotoxicity at all technology nodes.

Evaluation of the eutrophication potential of waterborne emissions is complicated by the fact that modern fabs do not release any untreated liquid waste directly into the environment, but rather pass treated wastewater into the municipal sewer system. CMOS logic fabs use large quantities of both ammonia and sulfuric acid in wafer cleaning
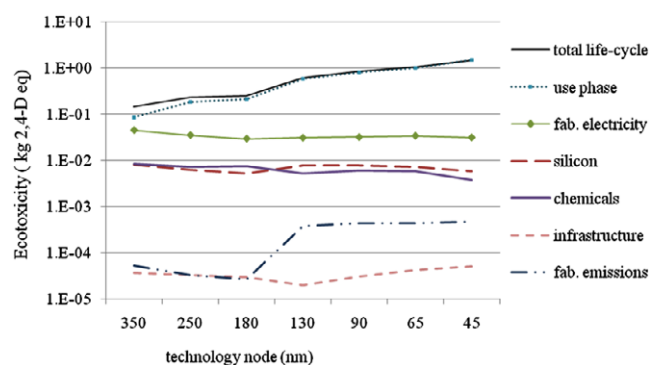
Figure 9. Ecotoxicity per die by technology node.

Figure 10. Worst-case eutrophication impacts (via water) per die by technology node.

processes. Liquid ammonia may be recycled on site using membrane filtration or distillation, or sent to the acid waste neutralization (AWN) system. In this model, the latter is assumed and thus ammonium sulfate, which results from the neutralization of ammonia and sulfuric acid effluents, is among the liquid wastes produced in the highest volume by wafer fabrication. Ammonium sulfate may experience a number of possible reactions in the municipal wastewater treatment system, but unless the waste is de-nitrified in a bioreactor, it will likely be released to surface or coastal water as dilute ammonium. The worst-case eutrophication impacts, assuming no downstream reaction or treatment of liquid waste, are presented in figure 10.

4. Uncertainty

Abatement products have inherently high uncertainty because uncertainty in the mass of process exhaust is compounded by variation in abatement efficiency. (Abatement efficiency is typically defined as the molar ratio for a target species of abated output to system input.) The uncertainty associated with the output of abatement is thus always higher than input flows, but small mass flows of untreated materials have a particularly high uncertainty. For example, if the removal efficiency of a particular species falls between 97% and 99%, the uncertainty in the mass of untreated material will be ±50%. As the efficacy of treatment approaches 100% and the mass flow of untreated compound falls, uncertainty associated with that flow is magnified. Consequently, the uncertainty of impacts from fabrication emissions which are treated by facility abatement is much higher than for energy or water use, or PFC emissions, which have been measured post-abatement.

4.1. Sensitivity analysis

Human health cancer impacts have the highest absolute sensitivity to lead emission factors for production of materials in the supply chain of fab equipment and building construction, and the highest relative sensitivity to abatement efficiencies. The impact category of water-borne eutrophication, which results only from fab emissions, has the greatest sensitivity to fab abatement efficiencies for nitrogen compounds (mainly ammonia).
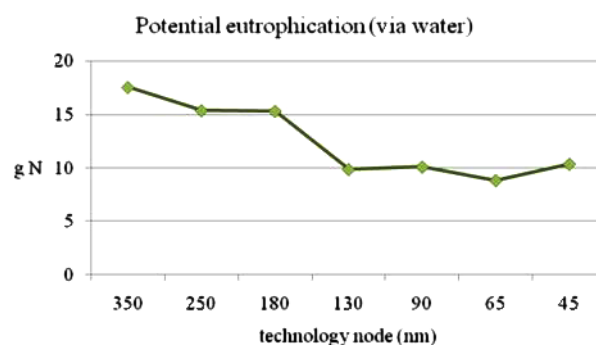
All other impact categories have the highest absolute sensitivity to use-phase power demand and utilization, power supply efficiency, and to a lesser extent fabrication yields. A more detailed report of the quantitative sensitivity analysis of the model and findings for the sensitivity of life-cycle energy use and GWP to data uncertainty and model assumptions is available in a previous paper [18].

4.2. Unaccounted impacts

While less than 0.5% of life-cycle POF is due to wafer fabrication releases, 8 of the 17 VOCs used in semiconductor fabrication do not have impact factors, neither in TRACI nor among the EPA reactivity factors, and thus are unaccounted for in the model. While these releases amount to less than 0.02% of the total mass of VOCs throughout the life cycle (contributing to about 40% of fabrication VOC releases by mass), the need for POF impact factors for the omitted chemicals (listed in the supplementary data available at stacks.iop.org/ERL/5/014011/mmedia) are noted. Ecotoxicity, human health cancer and non-cancer impact factors also lack for a number of process chemicals (e.g., hexa-methyl disilazane, octamethyl-cyclotetrasiloxane, ruthenium compounds) which, while emitted in small quantities, have undefined impact factors. Process emissions lacking health and ecotoxicity impact factors are noted in the supplementary data (available at stacks.iop.org/ERL/5/014011/mmedia). Because many sources of process inventory data for chemicals describe only energy use, the impacts associated with chemicals production in this model only include primary energy use, water consumption, GWP, and no other emissions. This lack of information on environmental emissions from the production of chemicals is noted as an area of data scarcity.

Data for chemical production representative of industrial products of relatively low purity is used for chemicals of high purity. Data for the energy consumed in purification of common process reactants such as silane and elemental gases (N_2, Ar, He, O_2) to semiconductor requirements (99.999 9997%) would enable more accurate semiconductor LCA in the future.

5. Discussion

A complete and transparent LCA of semiconductor logic has hitherto been unavailable to LCA practitioners seeking to assess the impacts of electronic systems and devices. This lack of data has limited the analysis of ICT as a tool in energy efficiency and GWP goals. The efficacy of a particular application of ICT in reducing net energy use or GWP can be more definitively evaluated using the values for the environmental and human health impacts of semiconductor logic presented here. Many generations of CMOS logic are evaluated in this study, with earlier generations representing logic currently used in lower performance applications such as embedded logic in appliances and the later generations, computers and servers. The lack of life-cycle inventory data for high purity chemicals and environmental impact factors for exotic or specialty chemicals continues to be a difficulty in semiconductor LCA, however. Listed in the appendix are process emission which may be of environmental concern but lack impact factors, as well as chemicals for which, in this study, a generic energy intensity value is used in place of specific inventory data.

By viewing the LCA results over time we can see trends in impacts per die. As use-phase power consumption and the complexity of fabrication have escalated, so have electricity- and infrastructure-related emissions. Reductions in fabrication emissions have been achieved at certain points with a few key process changes, as well as the limitation of test and monitor wafer runs which results in higher line yield (the ratio of finished wafers to processed wafers). Average line yield increased from 68 to 88% in the period under study, but as this metric approaches its practical limit, its benefits taper. As device complexity lengthens the process flow, fabrication impacts per die can be expected to rise in the future unless process technologies and fab operations can continue to adapt to meet emissions targets.

Emissions due to electricity consumed in the use-phase dominate most impact categories, particularly in the more recent technology generations. At the latest 45 nm technology node 95% of smog formation, 94% of acidification, 95% of eutrophication via air, 97% of ecotoxicity as well as 93% of human non-cancer health effects and 92% of EPA criteria health impacts are due to use-phase electricity. Limiting use-phase power consumption, through technical or operational means, is the most effective way to limit the life-cycle impacts of digital logic as we go forward.

Acknowledgments

References

[1] Tekwawa M, Miyamoto S and Inaba A 1997 Life cycle assessment; an approach to environmentally friendly PCs *Proc. IEEE Int. Symp. on Electronics and the Environment* pp 125–30

[2] Schischke K, Stutz M, Ruelle J-P, Griese H and Reichl H 2001 Life cycle inventory analysis and identification of environmentally significant aspects in semiconductor manufacturing *Proc. IEEE Int. Symp. on Electronics and the Environment* pp 145–50

[3] Taiariol F, Fea P, Papuzza C, Casalino R, Galbiati E and Zappa S 2001 Life cycle assessment of an integrated circuit product *Proc. IEEE Int. Symp. on Electronics and the Environment* pp 128–33

[4] Yao M A, Wilson A R, McManus T J and Shadman F 2004 Comparative analysis of the manufacturing and consumer use phases of two generations of semiconductors [microprocessors] *Proc. IEEE Int. Symp. on Electronics and the Environment* pp 97–103

[5] Plepys A 2004 Environmental implications of product servicising: the case of outsourced computing utilities *PhD Thesis* Lund University, September

[6] Plepys A 2004 The environmental impacts of electronics: going beyond the walls of semiconductor fabs *Proc. IEEE Int. Symp. on Electronics and the Environment* pp 159–65

[7] Murphy C F, Kenig G A, Allen D T, Laurent J-P and Dyer D E 2003 Development of parametric material, energy and emission inventories for wafer fabrication in the semiconductor industry *Environ. Sci. Technol.* **37** 5373–82

[8] Williams E D, Ayres R U and Heller M 2002 The 1.7 kilogram microchip: energy and material use in the production of semiconductor devices *Environ. Sci. Technol.* **36** 5504–10

[9] Blazek M, Rhodes S, Kommonen F and Weidman E 1999 Tale of two cities: environmental life cycle assessment for telecommunications systems *Proc. IEEE Int. Symp. on Electronics and the Environment (May 1999)* pp 76–81

[10] Ueno T, Shiino T and Onishi H 1999 Evaluation of electronic components in life cycle assessment *J. Mater. Cycles Waste Manag.* **1** 25–32

[11] Betz M, Schuckert M and Herrmann C 1998 Life cycle engineering as decision making support in the electronics industry *Proc. IEEE Int. Symp. on Electronics and the Environment* pp 231–6

[12] Deng L and Williams E 2008 Measures and trends in energy use of semiconductor manufacturing *Proc. IEEE Int. Symp. on Electronics and the Environment*

[13] Williams E 2004 Energy intensity of computer manufacturing: Hybrid assessment combining process and economic input–output methods *Environ. Sci. Technol.* **38** 6166–74

[14] Krishnan N, Williams E D and Boyd S B 2008 Case studies in energy use to realize ultra-high purities in semiconductor manufacturing *Proc. IEEE Int. Symp. on Electronics and the Environment*

[15] Plepys A 2002 The grey side of ICT *Environ. Impact Assess. Rev.* **22** 509–23

[16] Sematech 1999–2005 The international technology roadmap for semiconductors: 2005, 2003, 2001 and 1999 editions *Technical Report*

[17] CMU 2009 *Economic Input–Output Life Cycle Assessment* Carnegie Mellon University Green Design Institute, available at www.eiolca.net/

[18] Boyd S, Horvath A and Dornfeld D 2009 Life-cycle energy and global warming potential of computational logic *Environ. Sci. Technol.* **43** 7303–9

[19] Krishnan N, Boyd S, Somani A, Raoux S, Clark D and Dornfeld D 2008 A hybrid life cycle inventory of nano-scale semiconductor manufacturing *Environ. Sci. Technol.* **42** 3069–75

[20] Peterson T W 1999 VOC emissions reduction from photolithographic processes *Technical Report* University of Arizona, available at www.erc.arizona.edu/

[21] Sherer J M and Swauger J W 1998 *High Removal Efficiency Water Scrubbers for Low Inlet Acid Compound Concentrations in the Semiconductor Industry* October 1998

[22] Li S-N, Hsu J-N, Shih H-Y, Lin S-J and Hong J-L 2002 FT-IR spectrometers measure scrubber abatement efficiencies *Solid State Technol.*

[23] Chang F-T, Lin Y-C, Bai H and Pei B-S 2003 Adsorption and desorption characteristics of semiconductor volatile organic compounds on the thermal swing honeycomb zeolite concentrator *J. Air Waste Manag. Assoc.* **53** 1384–90

[24] Chein H and Chen T M 2003 Emission characteristics of volatile organic compounds from semiconductor manufacturing *J. Air Waste Manag. Assoc.* **53** 1029–36

[25] Stewart S 2005 Reducing volatile organic compound emissions through improved waste management *Proc. ISMI Symp. on Manufacturing Effectiveness*

[26] Sherer J M 2005 *Semiconductor Industry Wafer Fab Exhaust Management* (Boca Raton, FL: CRC Press)

[27] IPCC 2007 *Climate Change 2007: The Physical Science Basis, Contribution of Working Group I to the Fourth Assessment Report of the Intergovernmental Panel on Climate Change* (Cambridge: Cambridge University Press)

[28] Pacca S and Horvath A 2002 Greenhouse gas emissions from building and operating electric power plants in the upper colorado river basin *Environ. Sci. Technol.* **36** 3194–200

[29] Fthenakis V M and Kim H C 2007 Greenhouse-gas emissions from solar electric and nuclear power: a life-cycle study *Energy Policy* **35** 2549–57

[30] EPA 2008 *The Emissions and Generation Resource Integrated Database for 2007 (eGrid2007) Technical Support Document* US Environmental Protection Agency, September 2008

[31] EPA 2008 *The Emissions and Generation Resource Integrated Database for 2007 (eGrid2007)* US Environmental Protection Agency, available at www.epa.gov/cleanenergy/energy-resources/egrid/index.html (September 2008)

[32] King C W and Webber M E 2008 The water intensity of the Plugged-In automotive economy *Environ. Sci. Technol.* **42** 4305–11