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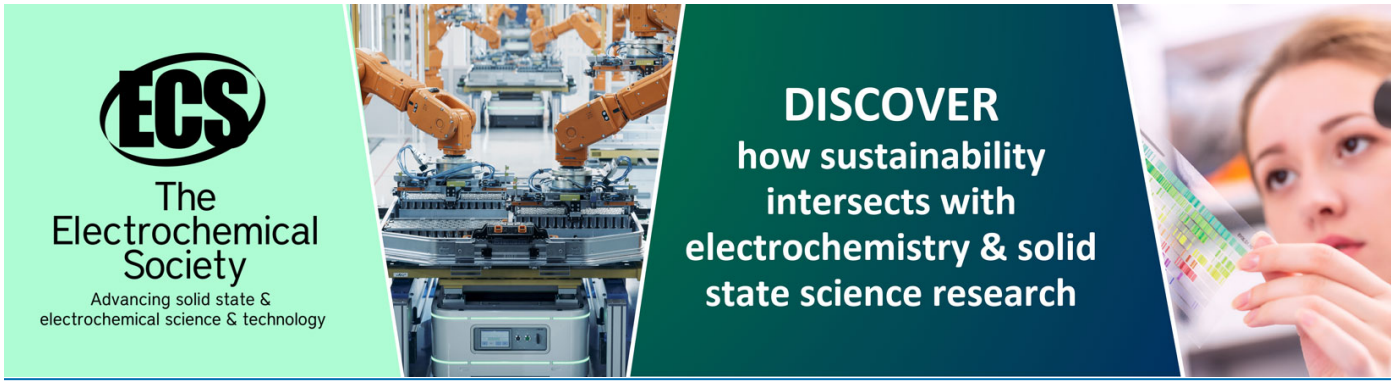

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Research of a long distance clock distribution system

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ABSTRACT: Ultrahigh-energy neutrinos with energies in excess of 100 PeV from the GZK effect will be studied using a new detector at the South Pole called the Askaryan Radio Array (ARA). The radiofrequency emission which occurs when these particles interact in the glacial ice is detected by an array of antennas spread out over an enormous area, over 100 km^2 and embedded in the ice at depths of 200 m to increase sensitivity. Signals from the antennas are digitized by specialized electronics and must be time synchronized with accuracies of order 50 ps or less for event reconstruction to function properly. A system has been proposed which digitizes the impulse waveforms *in situ* in the ice and sends the data to the surface using high-speed serial links. This requires distribution of a low-jitter clock to each hole but has substantial advantages in cost and power which drive our development effort to realize this technology. Last year we implemented a first version of a long distance clock synchronization system using electrical signaling over CAT5. This year we have updated our solution to optical fiber using high speed transceiver blocks in Spartan 6 FPGAs. The master clock is embedded into the data stream and distributed to the various holes where a phase-locked derivative is recovered. In this way, we have implemented a 1.25 Gbps data link over a bi-directional communication system fulfilling the requirements of the project. This note describes our efforts on the latter solution: technical details as well as methods of maintaining fixed phase difference between two clocks after power cycle and reset.

KEYWORDS: Digital electronic circuits; Trigger concepts and systems (hardware and software); Data acquisition circuits

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Contents

1 Introduction

The Askaryan Radio Array (ARA) [1] is a new detector to be deployed in the ice at the South Pole to detect ultrahigh energy neutrinos ($E > 100\,\text{PeV}$) by detecting the radiofrequency emission from electro-magnetic cascades formed when these neutrinos interact with nuclei in the ice. The completed array will contain 37 stations (see figure 1) and cover 160 km^2 surface area.

Each station consists of 4, 15 cm diameter boreholes spaced up to 70 m apart and 200 m deep (see figure 2). The 2 VPOL and 2 HPOL antennas in each hole operate between 100 MHz and 1 GHz near the thermal noise floor to pick up the weak RF emission. Signals from a station are combined to trigger full waveform readout from all 16 antennas later used to identify neutrino events from thermal and anthropogenic noise and reconstruct possible neutrino events for energy and direction.

A custom-designed ASIC resides on the DDA board (digitizing daughterboard for ARA). It digitizes 4 channels of waveforms from the antennas deployed in each hole at sampling speeds of up to 4 GSPS. Four DDA boards in total are used for one station.

In order to perform event reconstruction using cross-correlation techniques to arrive at sub-degree angular determination of the incident RF impulse, it is required that the clocks for all channels within a single station be synchronized: clocks on each DDA board need exactly the same frequency and must maintain a fixed phase difference relative to each other and a jitter less than 50 ps. The absolute phase offset is not important because it can be determined by using timing calibration sources (pingers) deployed in additional 200 meter deep calibration holes local to each station.

There are two options for signal transport out of the antenna holes to the station surface trigger and data acquisition computer. One is to transfer the analog RF signal from each antenna through individual optical fibers to DDAs located on the surface using COTS electrical-optical and optical-electrical converters. This solution is currently being used for the first ARA station. The other option is to put one DDA board down each hole close to the antennas and transfer the digitized signals to the surface. In order to do this, the surface logic has to distribute a low-jitter 125 MHz system clock to each of the 4 down-hole boards controlling each DDA. Additionally a data throughput of

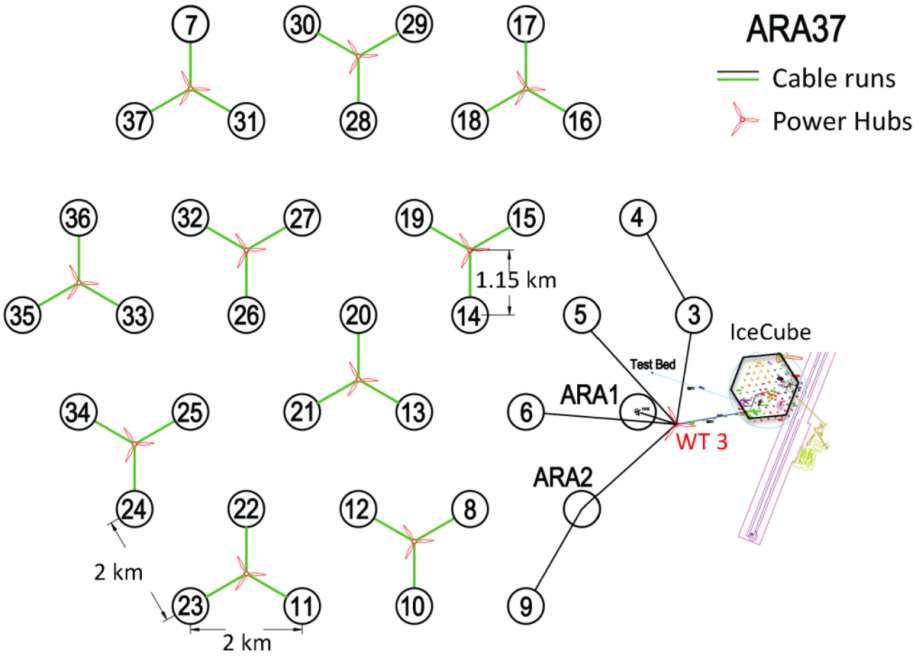

Figure 1. The cabling and power supply scheme of the ARA detector, each numbered circle represents one station.

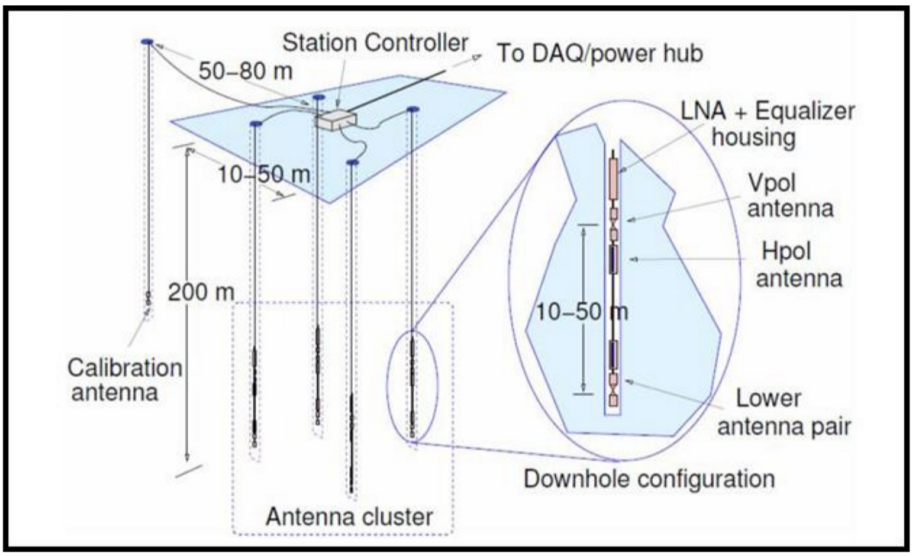

Figure 2. A schematic view of one ARA station.

approximately 500 Mbps is required to transfer the digitized data and low-latency trigger signals over a high-speed bi-directional serial link.

This latter option has substantial advantages in cost and power that are extremely important parameters to optimize for the success of the ARA project.

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2 Long distance clock distribution system

In 2010, we implemented a clock distribution and data transfer system over ordinary CAT5 cable [2], by transferring clocks and data separately. In this system we were able to distribute a 20 MHz clock over 250 meters of CAT5 while keeping the skew jitter between the original clock and the clock at the far end less than 50 ps. Due to the insufficient bandwidth of the long copper cable, 80 Mbps instead of 500 Mbps, the physical transmission medium had to be changed to optical fibers and high speed optical transceivers used in place of the Ethernet PHYs used in the first design. This new architecture benefits from recent developments in commercial-grade FPGAs with embedded high speed serial blocks and jitter-attenuating precision digital clock generators.

2.1 Technical detail and architecture description

The GTP [3] is a power-efficient high-speed serial transceiver included in variants of the Spartan 6 FPGA programmable logic family, it is highly configurable and tightly integrated with the programmable logic resources of the FPGA. It supports multiple industry standards with line rates from 614 Mb/s to 3.125 Gb/s, and includes built-in function modules like 8b/10b encoder and SERDES. The payload data at the transmitter may be coded into self-clocking signals and transferred serially; a copy of the transmitter clock is thus recovered at the receiver as well as the payload data by using the default CDR circuits and SIPO. In this way, clock distribution can be embedded with data transfer that eliminates the need of a separate clock path. A key issue preventing direct use of the recovered clock is that the jitter of the recovered clock is increasing with the increase of the link length even over SM fiber.

The quality of a high-speed serial data link between two GTPs is determined both by the reference clock on each side and the phase and frequency difference between the two endpoints. Normally one can use either a high quality differential oscillator or a high performance clock generator to drive the dedicated clock pins of a GTP.

In our architecture, an external jitter cleaner is used to both drive the GTP and clean the extra jitter of the recovered clock induced by the link itself. It solves not only the aforementioned problems but also provides enough flexibility to be used in both surface and down-hole boards, thus symmetrizing the system design (see figure 3).

At the surface board, a 10 MHz GPS-disciplined Rb clock is used as the system clock, from which a 125 MHz clock, generated by an internal PLL, is used as the reference clock of the jitter cleaner. The cleaned 125 MHz clock is used as the master clock to drive the GTP at a line rate of 1.25 Gbps or 2.5 Gbps, as needed. The high-speed serial data stream is then attached to an SFP (Small Form-factor Pluggable) transceiver for conversion to optical signaling and then transferred through the optical fiber. At the down-hole board, initially a cost effective 25 MHz oscillator is used to generate the 125 MHz GTP clock with the help of PLL and jitter cleaner in order to establish a first data link with the surface board. As soon as a noisy-though-stable recovered clock is available at the down-hole board, an internal multiplexer switches the reference clock of the jitter cleaner from the PLL to the recovered clock. In this way, the down-hole GTP is actually driven by a cleaned recovered clock that has exactly the same frequency as the surface GTP. A stable high-speed data link thus can be maintained with little effort. In addition, this cleaned recovered clock can be used as both the system clock of the down-hole board and the reference clock of the DDA

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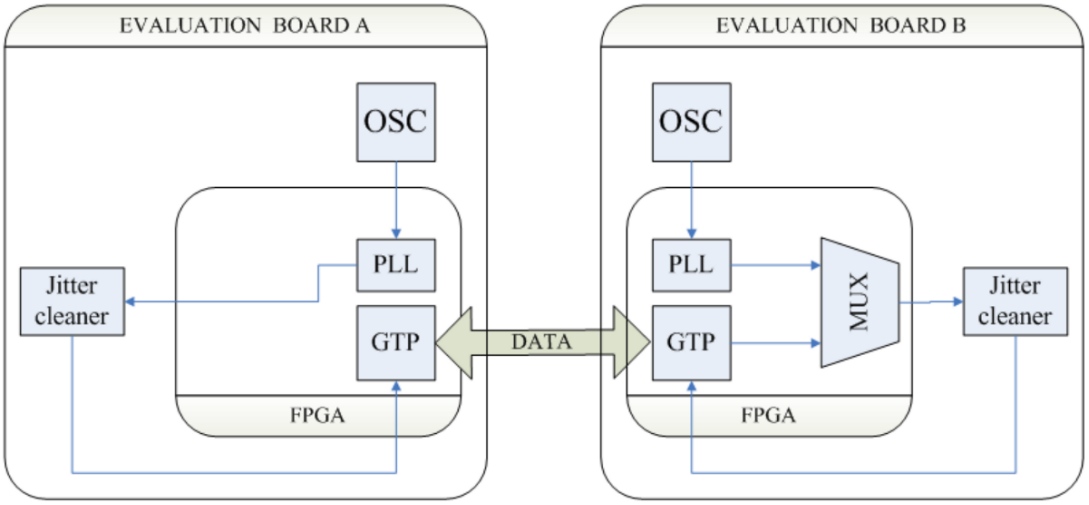

Figure 3. Architecture block of new clock distribution system.

board, and finally a fully synchronized data transfer system can be established as well as a high precision clock distribution system.

Compared to similar systems, like the timing system for XFEL [4, 5], which uses external CDR to distribute a 1.3 GHz system clock, and the white rabbit project [6] based on Synchronous Ethernet (SyncE) with extended IEEE1588 standard, our system requires relatively less external components aside from the FPGA and internal logic resources. This design is more suited to projects in extreme environments such as the South Pole due to the specific limitations of space, power consumption and reliability concerns.

2.2 Measurements and results

In order to verify our architecture, a PCIe x1 evaluation board has been designed. A Spartan 6 LX45T FPGA is used as the main PLD; two of the four GTPs contained in the FPGA are connected to SFP modules to implement the data link. A jitter-attenuating precision clock multiplier, Silicon Labs' SI5368 [7], is used as the jitter cleaner. Due to lack of availability of 25 MHz oscillator chips at the time of assembly of the evaluation boards, a 24 MHz oscillator has been mounted as the main clock source for the internal PLL resulting in a non-standard 126 MHz system clock. A soft-core MicroBlaze processor [8] is used to take care of various management functions, such as configuration of the SI5368 and clock switching. Because of the built-in holdover operation mode of SI5368, the reference clock can be switched smoothly without affecting the output of the clock synthesizer. This characteristic is very important for our system since the stability of the recovered clock is highly dependent on the stability of the GTP reference clock.

The measurement platform consists of two evaluation boards acting as the surface board and down-hole board pair connected via paired 2.67 Gbps WDM SFPs (SFPEX SMR353/SMR535) over 50 m of single mode optical fiber (see figure 4). A Tektronix DPO7254 running the DPOJET Jitter and Eye Diagram analysis software was used to measure and calculate all jitter measurements.

CK (see table 1) is the original clock generated at surface board, Ch4 is the clock at the down-hole board which is firstly recovered from optical fiber data and then cleaned by the jitter cleaner.

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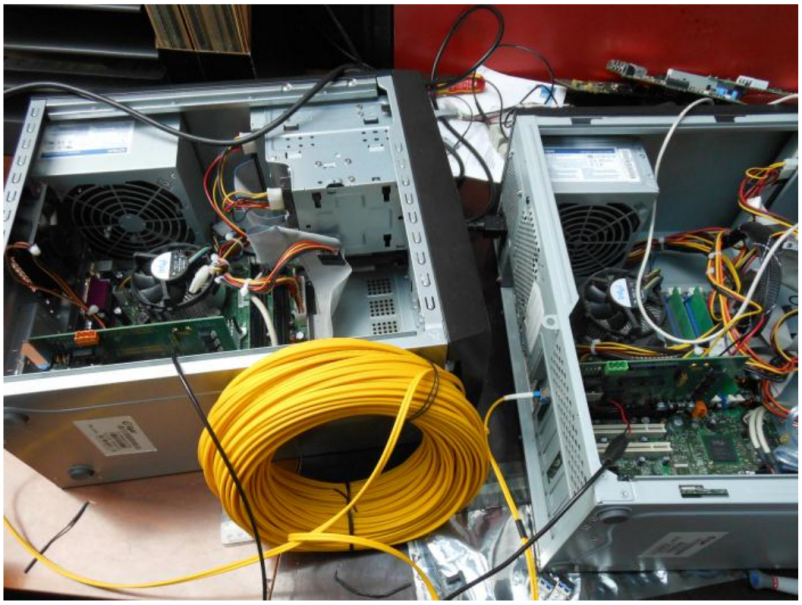

Figure 4. Measurements setup.

Table 1. Skew measurement results.

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Period1, Ch4	7.9367 ns	15.153 ps	8.0083 ns	7.8702 ns	138.10 ps	188994	115.77 ps	−136.90 ps
Current acquisition	7.9367 ns	15.124 ps	7.9940 ns	7.8726 ns	121.43 ps	62998	110.71 ps	−108.33 ps
Freq1, Ch4	126.00 MHz	240.56 kHz	127.06 MHz	124.87 MHz	2.1910 MHz	188994	2.1718 MHz	−1.8350 MHz
Current acquisition	126.00 MHz	240.10 kHz	127.02 MHz	125.09 MHz	1.9295 MHz	62998	1.7232 MHz	−1.7605 MHz
Period2, CK	7.9367 ns	14.813 ps	8.0000 ns	7.8732 ns	126.79 ps	188994	114.29 ps	−114.29 ps
Current acquisition	7.9367 ns	14.767 ps	8.0000 ns	7.8750 ns	125.00 ps	62998	104.76 ps	−114.29 ps
Freq2, CK	126.00 MHz	235.16 kHz	127.01 MHz	125.00 MHz	2.0129 MHz	188994	1.8116 MHz	−1.8116 MHz
Current acquisition	126.00 MHz	234.44 kHz	126.98 MHz	125.00 MHz	1.9841 MHz	62998	1.8116 MHz	−1.6636 MHz
Skew1, Ch4, CK	−1.5964 ns	16.293 ps	−1.5250 ns	−1.6646 ns	139.58 ps	188997	95.595 ps	−104.29 ps
Current acquisition	−1.6044 ns	15.028 ps	−1.5417 ns	−1.6646 ns	122.92 ps	62999	92.857 ps	−96.429 ps

The mean value of skew1 represents the absolute phase difference between the two clocks, and the standard deviation value of skew1 is the jitter. In current setup we have been able to distribute a 126 MHz clock over 50 meters optical fiber while keeping a skew jitter of < 20 ps between the cleaned recovered clock relative to the master clock. A stable data transfer speed of 2.52 Gbps was achieved.

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2.3 Fixed-latency system overview

Although we can benefit from a calibration pulser source to calibrate the absolute clock offset at any moment, we wish simplify operation and further generalize the applicability of the design by implementing a system which is completely capable of auto-determining clock offsets without need of external devices. In order to achieve this goal based on our architecture, we have implemented a fixed-latency data link for both directions.

In our architecture, the GTPs and jitter cleaners are the two main components which bring in uncertainties to the clock offset between master clock and cleaned recovered clock. As described in [9], the uncertain latencies in the GTP can be eliminated by using a custom comma detector and clock recovery phase shifting circuit, bypassing the equivalent functional blocks within the GTP which obscure the phase. In order to deal with the jitter cleaner, a fixed phase difference jitter cleaner CDCE62005 [10] as well as a 0-dealy jitter cleaner LMK03200 [11] were chosen for the next design: an evaluation board based on the AMC (Advanced Mezzanine Card) standard. Thus far the fixed-latency link is based on the CDCE62005.

The measurement setup will nearly the same for this board revision except this time we will repeat measurements before after power cycles on both evaluation boards to verify the stability of the link latency across FPGA reset conditions.

3 Summary and outlook

We have tested the performance of a system designed for simultaneous data transmission and distribution of a low-jitter clock across long serial communication links. A series of measurements have demonstrated that the clock skew jitter performance of less than 20 ps is adequate for our application. Due to the lack of software support on the Tektronix DPO7254, it has not possible to execute automated skew measurements. Therefore, our experiments to verify fixed-latencies across power cycles could only be done manually resulting in statistically poor measurements. Although the first results have been positive, many more tests are still needed.

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