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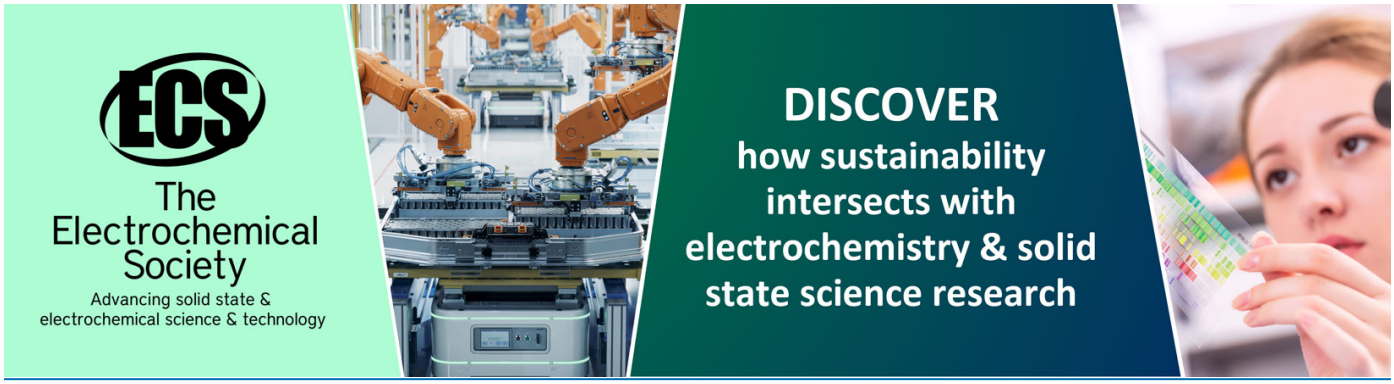

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Very forward muon trigger and data acquisition electronics for CMS: design and radiation testing

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ABSTRACT: With the forthcoming High Luminosity LHC accelerator upgrade, the CMS Endcap Muon system will require new electronics to handle the increased data rate while maintaining high data collection efficiency. Maintaining trigger efficiency for pseudorapidity above 2.1 requires deployment of higher performance electronics already in 2013. With the increased luminosity, the new electronics will be exposed to substantial radiation levels requiring higher tolerance of the components to radiation. We report on the progress in developing and building the new system and the results of radiation tolerance testing of the commercial components used in the system.

KEYWORDS: Radiation damage to electronic components; Muon spectrometers; Large detector systems for particle and astroparticle physics

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1 Introduction

The Compact Muon Solenoid (CMS) experiment [1] is a general-purpose particle detector at the Large Hadron Collider (LHC) at Cern. It is designed to make precision measurements of high-energy particles produced in proton-proton collisions, leading to greater understanding of the interactions between fundamental particles. The LHC will soon undergo an upgrade to increase the beam intensity, leading to five times higher data rate in CMS, and a corresponding improvement in experimental sensitivity. This High Luminosity LHC (HL-LHC) upgrade will increase the rate of particles passing through the Cathode Strip Chambers (CSC) [2] in the endcap muon system at CMS. The CSCs will require new electronics to handle the increased data rate and maintain high data collection efficiency, and the new electronic components must be proven to withstand the radiation levels present in the CMS endcap region. To this aim, radiation testing has been performed on over 40 commercial off-the-shelf (COTS) components. The performance and survivability of these devices for use in CSC electronics is evaluated in this paper.

2 Radiation testing of electronic components

The design considerations and motivation for the CSC electronics upgrade project are detailed in our previous work [3] which was based on tests performed in 2011. Several customized circuit boards were developed at Texas A&M University to study the radiation survivability of candidate commercial components proposed for use in the CMS Endcap Muon project. These include the Trigger Motherboard mezzanine prototype boards, used as a test bed for cyclotron-based Single Event Upset (SEU) studies in the digital components, as well as simpler test boards used for reactor-based Total Ionizing Dose (TID) and displacement damage testing for the non-digital components. This study builds upon the 2011 work in many ways, with several additional components under test, more extensive studies of SEUs and mitigation techniques, and increased proton fluence for device testing with a higher exposure level.

Table 1. Summary of SEU observations for each component during proton irradiation at the UC Davis cyclotron, and the resulting cross sections. The measurements and results reflect the integrated exposure for the devices under each test. The last column shows the rate of SEUs expected for each device in the CSCs during HL-LHC operation. Mitigation is implemented in the logic for the FPGA BRAM and CLB tests.

Component Tested	SEU	Proton Fluence ($\times 10^9$ p/cm^2)	SEU Cross section $\sigma(\times 10^{-11}\text{cm}^2)$	Expected SEU Rate at CMS
Finisar Tx	195	446	44 ± 3	13/year/link
Finisar Rx	3340	446	750 ± 10	1/day/link
Emcore Snap12 Tx	73	439	17 ± 2	1/year/link
Emcore Snap12 Rx	1922	196	980 ± 20	4/month/link
Reflex Photonics Rx	1275	200	640 ± 20	3/month/link
TI Level Shifter	0	445	< 0.52	0
Virtex-6 GTX	160	157	102 ± 8	3/year/link
Virtex-6 CLB	157	26.8	590 ± 50	1/day/chip
Virtex-6 BRAM	0	2.79	< 82	$<$ 4/month/chip

2.1 Digital component testing

Tests were performed on five digital components in 2011 using the 55 MeV proton beam available in the Radiation Effects Facility at the Texas A&M University Cyclotron Institute. The 2011 tests yielded good SEU cross section measurements, but the limited beam flux allowed for only 6 to 7 krad of exposure. Furthermore, the Field-programmable Gate Array (FPGA) tests in 2011 did not include any SEU mitigation logic.

To expand upon the 2011 study, the digital tests performed in 2012 included two additional test components and extended the exposure level with the higher flux provided by the 64 MeV proton cyclotron at the UC Davis Crocker Nuclear laboratory. While neutrons with energy over 20 MeV are the true cause for 90% of the SEUs in the endcap region of CMS [4], protons are suitable for use in this study because the upset susceptibility in silicon for protons at this energy is equivalent to that for neutrons. In this way, the increased flux provided by the UC Davis beam made it possible to test for TID and displacement damage at more than three times the full exposure level expected in the CMS endcap during HL-LHC operations, while also performing new SEU tests with FPGA logic that incorporates SEU mitigation in the firmware.

The procedures used in this study were similar to those in 2011. Our customized monitoring system was used to detect errors in each component, identify the type of digital failure that occurred, and save the information from each occurrence in a log file for offline analysis.

The components tested include a Xilinx Virtex-6 FPGA, a TI SN74CB3T16212 bus exchange level shifter, a duplex opto-coupler from Finisar, a Snap12 receiver opto-coupler from Reflex Photonics, and similar Snap12 transmitter and receiver opto-couplers from Emcore. At least two samples of each digital component were tested, and the results are presented in table 1. The table shows the total integrated proton fluence and the measured SEU cross sections for the devices, as well as for the independent internal elements within the Virtex-6 FPGA. The last column lists the corresponding rate of SEUs expected during HL-LHC operation for each device.

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The Snap12 components tested here include the Reflex Photonics SN-R12-C00501 receiver (Rx), Emcore EMRS1216 receiver (Rx), and the Emcore EMTS1216 transmitter (Tx). The test results were comparable to the previous 2011 results, including the newly-tested Emcore parts which show SEU sensitivity similar to those from Reflex Photonics. All the Snap12 components survived beyond the required 30 krad exposure level, and the SEU rates are acceptable for operation in the CMS endcap region.

The Finisar FTLF8524E2GNL transceiver was tested on both the transmit (Tx) and receiver (Rx) side in 2012. The transmit test in this study was performed at five-times higher packet transfer rate relative to the 2011 study, and the increased duty cycle is reflected in the 4-fold increase of the measured SEU cross section over the previous results.[1] Extending this relationship to correct for the higher duty cycle in use during normal CMS operation leads to approximately ten SEUs expected per day per link, equivalent to about one error in every 20 trillion bits transmitted. This low rate of errors is acceptable for reliable operations in the CMS endcap.

The Finisar receiver test was added to meet a new design requirement established in 2012; in this test module, gigabit Ethernet data packets were sent from the control PC to the FPGA through the Finisar, and the software monitored the FPGA status to verify valid reception. The data transfer rate in this test was consistent with that used for normal CMS operations, so no duty-cycle correction is needed, and the SEU rate is low enough for reliable CMS endcap operations.

Testing of the Texas Instruments SN74CB3T16212 Bus Exchange Level Shifter was repeated exactly as it was done in 2011. No SEUs were observed, even with the additional fluence provided by the UC Davis cyclotron. The 2012 SEU cross section measurement is shown in table 1; combining this with statistics from 2011 yields an SEU cross section smaller than 4×10^{-12} cm^2 at 90% confidence level.

The Xilinx XC6V195T-2FFG1156CES Virtex-6 FPGA was used in these tests. Three different elements of the Virtex-6 FPGA structure were tested: GTX transceivers (55% of GTX resources were utilized in the chip), Block RAMs (74% were used), and CLB logic blocks (43% used). All of these elements were operated in parallel and the status of each module was monitored independently during exposure.

The FPGA GTX test was performed just as in the 2011 study, with the exception that eight fiber links were operating, as opposed to the six used in 2011. Taking this into account, the GTX test results were consistent with the low rate of errors found previously. With just a few SEUs expected per year on each link, there should be no significant impact on performance for CMS endcap electronics.

The FPGA CLB test in this study was performed using several 16384-bit serial shift registers implemented in the logic fabric, each injected with identical randomized patterns. The outputs of these shift registers were voted against each other, and the results were monitored for errors in terms of single bit errors in individual shift registers, as well as the voted bit failures that involve two or more bits in different shift registers. The purpose of this test was to determine the level of SEU mitigation provided by the use of triple-voting in the logic elements. However, during the FPGA exposure the error monitoring system showed SEUs occurring in a pattern which suggested the test control logic itself was being corrupted by SEUs, and the CLB tests could not be analyzed in some of the high-flux proton exposure runs due to the resulting inconsistencies. It was then

[1] The SEU relationship with the link duty-cycle was noted in the 2011 study.

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realized that while the voted test elements in the CLB test may have some protection against SEUs, the non-voted control logic responsible for random pattern injection and error checking did not, which made interpretation of the results more complicated. However, the test runs performed with lower proton flux presented less difficulty for offline analysis, and several of these runs could be clearly analyzed. Results from the low-flux runs show the SEU rate in this CLB test was lower by a factor of six relative to the unmitigated CLB tests performed in 2011. The incompleteness of this triple-voting implementation has certainly limited its effectiveness, but the observations from the study demonstrate significant promise for this SEU mitigation technique when fully implemented in firmware for the CMS endcap electronics.

For the FPGA Block RAM test, the firmware used BRAMs implemented as 64-bit RAM units with the embedded Virtex-6 ECC error correction feature activated in order to mitigate SEU effects. The control and monitoring software loaded randomized patterns into the BRAMs via the gigabit Ethernet link, then read back the BRAMs to check for errors. As with the CLB tests, there were some test limitations due to SEUs in the test control logic. Because of this, the test analysis was limited to the low-flux runs in the proton beam, and this is reflected in table 1. However, in the final analysis no BRAM SEUs were observed. This is a substantial improvement relative to the 2011 results, where SEUs in the unmitigated BRAMs were shown to be a significant concern, and it proves the SEU mitigation capability of the embedded ECC feature in the Virtex-6 FPGAs to be used in the endcap electronics.

All of the digital components in the study survived beyond the 30 krad exposure level, and the SEU rates are acceptable for operation in the CMS endcap region. However, it should be noted that two of the three Finisar parts tested died in the 31 to 35 krad range.

2.2 Non-digital component tests

CSC electronics development began in 2011 and continued into 2012. Several non-digital component candidates were identified to fill various design requirements based upon electrical and mechanical specifications provided by the manufacturers. As in the 2011 studies, components selected in 2012 were tested for TID and displacement damage in the Texas A&M Nuclear Science Center reactor. In 2012 we tested 25 different COTS components with 1 MeV neutrons, following the same procedures used in 2011. The goal of these studies was to determine the overall survivability of selected COTS components in the radiation environment of the CMS endcap, with no distinction drawn between TID and displacement damage failure modes.

The full set of pass/fail results for these tests are presented in tables 2 through 6, along with the manufacturer and model information. At least two samples of each component were tested to 30 krad, with over 10^{13} n/cm^2 neutron fluence in every case. The pass/fail results are based on experimental observations that the devices continued (or failed) to operate properly after the exposure.

Table 2 shows the pass/fail status for the 13 voltage regulators tested. Six of the devices survived the exposure, all with 3 A or higher current capability, making them suitable for use as stable low-voltage power supplies for the CMS endcap electronics.

Similarly, results for the low-current voltage references are summarized in table 3, amplifiers in table 4, transistors and sensors in table 5, and diodes in table 6. Although several component failures are noted in these tables, the set of surviving candidates is sufficient to meet the design requirements for the CSC electronics project.

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Table 2. Voltage regulator test results with 30 krad and over 10^{13} n/cm^2 of 1 MeV neutron exposure at the TAMU Nuclear Science Center reactor.

Part/Chip Name	Chip Type	30 krad Exposure
Maxim 8557ETE	Voltage Regulator	Fail
Micrel MIC69502WR	Voltage Regulator	Pass
Micrel MIC49500WU	Voltage Regulator	Pass
National Semi LP38501ATJ-ADJCT-ND	Voltage Regulator	Pass
National Semi LP38853S-ADJ-ND	Voltage Regulator	Pass
Sharp PQ05VY053ZZH	Voltage Regulator	Fail
Sharp PQ035ZN1HZPH	Voltage Regulator	Fail
Sharp PQ070XZ02ZPH	Voltage Regulator	Fail
Sharp PQ7DV10	Variable Output 10A Voltage Regulator	Pass
TI TPS740901KTWR	Voltage Regulator	Pass
TI TPS75601KTT	Voltage Regulator	Fail
TI TPS75901	Voltage Regulator	Fail
TI TPS7A7001	Very Low Dropout, 2A Regulator	Fail

Table 3. Low-current voltage reference test results after neutron exposure at the TAMU Nuclear Science Center reactor.

Part/Chip Name	Chip Type	30 krad Exposure
Analog Devices ADM660AR	CMOS Switched-Capacitor Voltage Converter	Pass
Analog Devices ADM8828	Switched-Capacitor Voltage Inverter	Pass
Intersil ICL7660S-BAZ	Switched-Capacitor Voltage Converter	Fail
Linear Technology LTC1044CS8	100mA CMOS Voltage Converter	Pass
Maxim MAX664CSA	Micropower Voltage Regulator	Fail
Maxim MAX680CSA	+5V to ±10V Voltage Converter	Pass
Maxim MAX860-UIA "uMAX"	Switched-Capacitor Voltage Converter	Pass
Maxim MAX861-ISA	Switched-Capacitor Voltage Converter	Pass
Maxim MAX1044CSA	Switched-Capacitor Voltage Converter	Fail
Microchip TC1044SCOA	Charge Pump DC-TO-DC Voltage Converter	Pass
Microchip TC962COE	High Current Charge, Pump DC-to-DC Converter	Pass
National Semi LM41211M5-1.2	Micropower Low, Dropout Voltage Reference	Pass
National Semi LM4121AIM5-ADJ	Micropower Low, Dropout Voltage Reference	Pass

Table 4. Amplifier chip test results after neutron exposure at the TAMU Nuclear Science Center reactor.

Part/Chip Name	Chip Type	30 krad Exposure
Maxim MAX4372	High-Side Current-Sense Amplifier	Pass
Micrel MIC35302	High-Side Current-Sense Amplifier	Fail
Micrel MIC37302	High-Side Current-Sense Amplifier	Fail
Analog Devices AD8028AR	High Speed, Rail-to-Rail Input/Output Amplifiers	Pass

Table 5. Transistor and sensor chip test results after neutron exposure at the TAMU Nuclear Science Center reactor.

Part/Chip Name	Chip Type	30 krad Exposure
Fairchild 2N7000	N-channel FET transistor	Pass
National Semi LM19CIZ	TO-92 Temperature Sensor	Pass
TI SN74LVC2T45	Two-bit Dual-supply, Tri-statable Bus Transceiver	Pass
Analog Devices ADM812	Voltage Monitor	Pass

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Table 6. Diode radiation test results after neutron exposure at the TAMU Nuclear Science Center reactor.

Part/Chip Name	Chip Type	30 krad Exposure
ST Micro 1N5819	diode	Pass
ON Semi 1N5819	diode	Pass
Fairchild MM3Z4V7C	Zener Diode	Pass
Fairchild MM3Z5V1B	Zener Diode	Pass

3 Conclusion

Several commercial components to be used in the CSC electronics project were tested at the UC Davis Crocker Nuclear Laboratory and the TAMU Nuclear Science Center. Over 40 devices in total were tested, and 32 radiation-tolerant components were identified that are good candidates for use in the CMS endcap environment during HL-LHC operation.

SEU tests showed that the Virtex-6 FPGA is the only component in the CSC system with significant SEU susceptibility. Promising SEU mitigation methods were identified to ensure an acceptable rate of errors for firmware operating in the CMS endcap. Prototypes of the new CSC electronics boards have been built using the tolerant components, and firmware development to integrate these SEU mitigation techniques is underway.

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