

Review of radiation hard electronics activities at European Space Agency

To cite this article: G Furano *et al* 2013 *JINST* **8** C02007

View the [article online](#) for updates and enhancements.

You may also like

- [An homeopathic cure to pure Xenon large diffusion](#)
C.D.R. Azevedo, L.M.P. Fernandes, E.D.C. Freitas et al.
- [Recent progress in the development of 3D deep n-well CMOS MAPS](#)
G Traversi, L Gaioni, A Manazza et al.
- [Building blocks X-FAB SOI 0.18 m](#)
J.-B. Cizel, S. Ahmad, S. Callier et al.



ECS
The
Electrochemical
Society
Advancing solid state &
electrochemical science & technology

DISCOVER
how sustainability
intersects with
electrochemistry & solid
state science research

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2012,
17–21 SEPTEMBER 2012,
OXFORD, U.K.

Review of radiation hard electronics activities at European Space Agency

G. Furano,¹ R. Jansen and A. Menicucci

*European Space Agency, European Space Research & Technology Centre,
Postbus 299 - 2200 AG Noordwijk, The Netherlands*

E-mail: gianluca.furano@esa.int

ABSTRACT: Several Research and Development activities are ongoing at European Space Agency [1] to secure the supply of key electronic parts for current and future space avionics systems. Analogously to astro-particle and high-energy physics, the space missions radiation environment drives the radiation hardness requirements, which limits availability of suitable electronic components. In particular for the future ESA flagship Jupiter science mission, the necessary processing, reliability, mass, power performance requirements are difficult to meet with current components and systems with sufficient radiation tolerance margins. Improved radiation characterisation and modelling of the Jupiter radiation environment as well as operational radiation monitoring during the mission will be key in ensuring adequate margins for the operation of electronic components.

KEYWORDS: On-board data handling; Space instrumentation; On-board space electronics

¹Corresponding author.

Contents

| | | |
|----------|--|----------|
| 1 | Overview — electronics R&D activities at ESA | 1 |
| 2 | Overview — radiation environment and effect characterisation, modelling and radiation hardness assurance at ESA | 2 |
| 3 | Environmental requirements for different classes of missions at ESA | 2 |
| 3.1 | Global monitoring for Earth and security and Earth observation missions | 3 |
| 3.2 | Telecom and navigation missions | 3 |
| 3.3 | Planetary exploration missions | 4 |
| 4 | Radiation monitors: space weather monitoring and design margin verification | 4 |
| 5 | Space technology requirements of future ESA missions | 5 |
| 6 | Space technology trends | 6 |
| 6.1 | Trends in space electronic systems: FLASH-based mass memories | 6 |
| 6.2 | Trends in space electronic systems: system on a chip | 6 |
| 6.3 | Trends in space electronic systems: configurable & programmable systems | 7 |
| 6.4 | Trends in space integrated circuits technology | 8 |
| 7 | Future technologies for space electronics at ESA | 9 |

1 Overview — electronics R&D activities at ESA

In support to the spacecraft developments for the ESA missions, several research and developments activities are undertaken to ensure the supply of their key avionics electronic components [2, 3]. The Technology Research Programme (TRP), Core Technology Programme (CTP) and European Component Initiative (ECI) focus on the development of spacecraft platform and payload building blocks, which may be used across multiple missions. Such an approach, coordinated with the national space agencies at a European level, requires a clear strategy, harmonisation and standardisation in terms of avionic spacecraft architectures, including the functional elements like processors and memories as well as communication interfaces and protocols. Cooperation is also required with software disciplines to ensure that hardware elements can be integrated with a minimum of effort (see [7]).

Current electronic systems R&D activities at ESA focus on:

1. the characterisation, modelling and specification of the radiation effects (TID and SEE, NIEL-displacements) for different classes of missions

2. the continued development of reliable methods, guidelines and standards for the safe use of Commercial-Off-The-Shelf (COTS) components, and rad-hard by design (RHBD) techniques,
3. the up-screening and radiation-effect mitigating of COTS components and in particular of volatile and non-volatile memories down to the sub 45nm CMOS technology node.
4. the deployment and development of European Space Components Coordinated (ESCC) qualified fault-tolerant processors and micro-controllers in single and multi-core configuration,
5. the maintenance and development of ESCC qualified digital radiation hard ASIC processes and technology digital library,
6. the deployment and development of ESCC qualified small, medium and large radiation hard reprogrammable FPGAs,
7. the maintenance and development of Mixed-Signal radiation hard ASIC processes and technology digital and analogue IP core library.

2 Overview — radiation environment and effect characterisation, modelling and radiation hardness assurance at ESA

The correct implementation of a system-wide Radiation Hardness Assurance (RHA) policy especially for what concerns margins, is of paramount importance for space missions. Specific activities to reduce the “hidden” and explicit margins in radiation hardness assurance are needed. Reduced margins are possible, with an accurate measurement, modelling and simulation of radiation environment and its effects. Reduced margins may allow use of ‘softer’ but more advanced EEE components and this will be a major performance/cost benefit and competitive driver for space industries.

A systematic approach towards the accurate measurement of the radiation environment (both for TID and SEE) at unit and component level is being considered.

A key topic in this field is the development and maintenance of the future set of European radiation monitors, with focus on:

1. the Next Generation Radiation Monitor,
2. the Standard radiation hard front-end ASIC for radiation and particle monitors,
3. the Radiation Monitor for the Jupiter mission,
4. the Active Pixel Sensor (APS) based Miniaturized Radiation Monitor.

3 Environmental requirements for different classes of missions at ESA

Space-borne electronic systems may have very variable requirements in terms of operational availability and reliability for radiation hardness assurance.

The whole radiation hardness assurance process is iterative; it starts first with top-level estimations

of the radiation environment, then the radiation levels at component level are calculated, and finally the electronic designs analysed in order to assess the effect on critical or sensitive parts.

The three main sources of radiation that have to be considered are:

- the trapped electrons and protons in the Earth's radiation belts.
- the protons and heavy ions produced by the Solar Particle Events (SPE).
- the Galactic Cosmic Rays (GCR) protons and heavy ions.

but modern transport models, mostly based on monte-carlo simulations, take also into account the non negligible role of secondary electrons created by large and composite structures.

3.1 Global monitoring for Earth and security and Earth observation missions

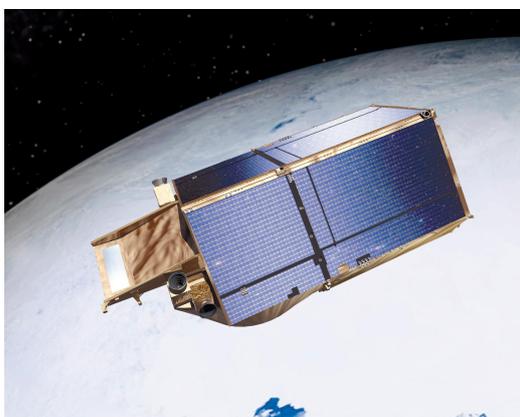


Figure 1. Cryosat, Earth Observer launched 8 April 2010.

Global Monitoring for Earth and Security (GMES) and Earth observation (EO) missions are normally in Low Earth Orbit (LEO), thus well inside magnetosphere, but often in polar orbits, and their lifetime (normally of 2-5 years) is generally determined by operational rather than reliability factors. Accumulated doses are quite low, $\approx 1-5$ krad/yr and due mostly to protons in inner belts (south Atlantic anomaly). Effects of GCRs in polar zones cannot be neglected, and in recent history many in-flight failures have been generated by SEEs. Nevertheless, operational constraints are normally relaxed, and fail-safe modes (at least on payloads) are foreseen, allowing use of 'up-screened' COTS devices.

3.2 Telecom and navigation missions

In contrast telecom satellites are geostationary, and built for continuous operation over more than 15 years. Geostationary orbit crosses outer radiation belts and the accumulated dose is on the order of $\approx 5-10$ krad/yr. The prevalent radiation are electrons (and their Bremsstrahlung), making local shielding of sensitive components complex. Telecom satellites have single failure operational requirements both at payload and platform level, since continuous operation has to be guaranteed. For some critical functions even double-failure operational requirements exist. Furthermore, the operational lifetime of a satellite platform is counted in decades requiring high-reliability components and engineering.

A further commonality exhibited by Telecom and Earth Observation missions is the need to produce multiple satellites or platforms in a restricted time scale and this implies the application of industrial procedures that are not usually implemented in space programs. Science missions require enhanced modularity and multi-instruments support whereas Earth Observation missions need very high data throughput links and increased memory capacity.

Furthermore, Earth Observation missions share with Telecom projects avionics architectures that implement security solutions to protect the payload data and the spacecraft control and monitoring functions.



Figure 2. Alphasat, next generation European telecom platform.

Telecommunications satellites are key elements of the worldwide information infrastructure to be protected against occurrence of events like service denial, misuse, not authorized access or modification of information. All the mentioned events can reduce the availability of the provided services producing economic losses for operators, end users and stakeholders of information systems.

Lastly the spacecraft platform and subsystems need to be available for decades, putting the management electronic component obsolescence in focus when designing a system.

3.3 Planetary exploration missions



Figure 3. Juice, the Jovian system orbiter, due to launch in 2022.

The next ESA flagship mission will be a planetary probe on Jupiter. It will be launched in 2022 from Europe's spaceport in Kourou, French Guiana, on an Ariane 5, arriving at Jupiter in 2030 to spend at least three years making detailed observations with multiple science payloads of the planets and its inner Galileian moons.

Once in Jovian orbit, accumulated dose is foreseen to be hundreds of krad/year, but with the big uncertainties due to a less known environment, where several highly variable trapped belts of protons, electrons

and plasma exist. Such missions are clearly a once-in-a-lifetime scientific opportunity and any failure at platform and payload level is considered not acceptable.

4 Radiation monitors: space weather monitoring and design margin verification

The number of flying or ready to fly European radiation and plasma instruments has increased significantly in the last few years. Research programmes have also made good progresses in investigating innovative technologies and new concepts designs, which will allow a substantial reduction of mass, power and data rate budgets compared to traditional instrumentation, whilst providing

equivalent or higher detection efficiency. With many future missions in Navigation, Telecommunications, Exploration, Science and GMES and EO domains flying in severe radiation environments and carrying highly sensitive components and systems, the need for such radiation instrumentation is increasing. Accurate measurements of the Space Environment plays also a crucial role in improvement of radiation environment models and the development of the space weather services required by the ESA Space Situational Awareness programme. Developments of radiation detectors and monitors are Harmonised through the Industrial Policy Committee (IPC) Technology Harmonisation Advisory Group (THAG) and tracked by the Space Environments and Effects Network of Technical Competencies (SEENoTC — [9]) and classified by the ESCC Component Technology Board (CTB) Radiation Working Group as follows:

1. Devices to provide coarse radiation housekeeping data
2. Devices to provide in-situ radiation data and alert platform systems
3. Devices to support the payload systems
4. Devices designed for providing space-weather data
5. Devices for the provision of science data in preparation of future missions

5 Space technology requirements of future ESA missions

The evolution of electronics technology is opening an incredible amount of possibilities for the spacecraft avionics, that reduce weight and power and increase functionality and processing performance, that have been successively used in automation and embedded applications:

- implementation of high-performance processors architectures
- integration of different functionalities, until now implemented on several boards, onto a single chip (SoC),
- introduction of digital sensor buses.

There is also a dark side in the electronics technology that is evolving faster: quick *obsolescence* of electronic parts. Obsolescence has side effects also on the space electronics world, even if sometimes they are delayed: the evolution of the silicon technologies has basically cancelled the possibility to continue to use components like microcontroller 80C32 and digital signal processor TSC21020 developed and qualified years ago and for which an alternatives are not existing at the time being (they have reached obsolescence in 2010).

Future programs for Science, Exploration, Earth Observation, Telecom and Launcher are the sources of high demanding and additional requirements for the next generation of On-Board Computers (OBC), Data Handling and Data Systems. Increase of the processing power, reduction of mass, volume and power budgets can be considered a sort of natural evolution of the existing requirements. In addition to these top-level requirements there are also those low-level ones associated with the next generation on-board computer architecture, involving lower level communication, that introduce new functional services for the application software.

Furthermore, digitalization and standardization of interfaces allows use of “Building Block” approach, both in development and testing of new equipment [7].

6 Space technology trends

6.1 Trends in space electronic systems: FLASH-based mass memories

A “space grade” Non-Volatile RAM (NVRAM) does not exist, since for this high volume, low-margin device the market is driven by low-reliability consumer electronics. Commercial markets are dominated by NAND (and some NOR) FLASH. Due to its simple structure and high demand for higher capacity, NAND FLASH memory is the most aggressively scaled technology among electronic devices. The technology has reached 20 nm in production (SAMSUNG, INTEL, MICRON). While the expected shrink time-line was a factor of two every three years per original version of Moore’s law, this has recently been accelerated in the case of NAND flash to a factor of two every two years.

As the feature size of flash memory cells reach the minimum limit, further flash density increases will be driven by greater levels for Multi Level Cells, possibly 3-D stacking of transistors, and improvements to the manufacturing process. The decrease in endurance and increase in uncorrectable bit error rates that accompany feature size shrinking shall then be compensated by improved error correction mechanisms.

For these reasons use of FLASH devices in space hits the inconvenient truth: FLASH are not “simple” NVRAM, since management, failure modes, and error correction schemes are very complex and application dependent. Furthermore, we will soon face an environment where DRAM Memory Modules are going to be replaced with NVRAM (FLASH or FRAM) memory modules to overcome the SDRAM obsolescence and to increase the memory density, while keeping power consumption in an acceptable range. Mass memories in space systems are evolving from simple stream tape-like recorders to complex intelligent (sub)systems capable of autonomous operations. This evolution is driven mainly by requirements coming from complex multi-payload missions, where more than the brute performance requirement (speed, capacity), functional requirement play a role. However, high-reliability electronics is struggling in keeping the pace with the aggressive down scaling of NVRAM (mainly NAND flash) technology. As a consequence, the use of NVRAM in space applications is not as established as in the consumer market and is still under research. Considering that the full commercial availability of qualified space memories is not an option for costs, manufacturer’s interest, long lead times or performance reasons, adoption of COTS memories for the proposed application is unavoidable. Up-screening of COTS memory chips has demonstrated in the past that most of those components are not able to successfully operate and survive in the demanding space environment. The few that demonstrate promising robustness request additional design efforts to meet reliability requirements for space missions. Activities in this field, aim at providing practical valuable architectural guidelines, comparisons and trade-offs among the huge number of fault tolerant methodologies for NVRAM applied to the critical space environment.

6.2 Trends in space electronic systems: system on a chip

Reduction of power consumption, mass and dimensions achievable with silicon evolution and introduction of the System On a Chip SoC technology are significant. For example for a key sys-

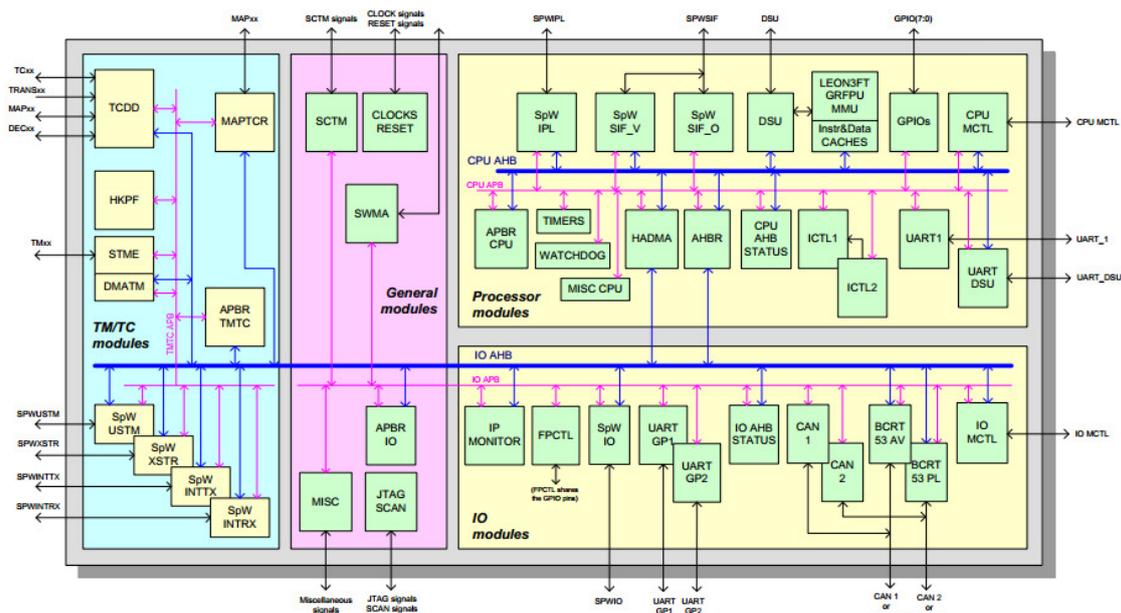


Figure 4. SCOC3 Simplified Block diagram.

tem like the spacecraft On Board Computer (OBC) “classic” designs based on monolithic processor (ERC32) had power consumption of ≈ 90 W, mass of 21 kg, dimensions of $470(L) \times 272(H) \times 332(D)$ mm³ (GOCE EO Mission, launched in 2009). Its evolution, based on the new generation SPARC V8 AT697F processor is the GAIA Command and Data Management Unit (CDMU) (to be launched in 2013), with power consumption of ≈ 40 W, mass 16kg, dimensions of $420(L) \times 270(H) \times (276(D))$ mm³. But, a SoC-based equipment, like SEOSAT OBC (due to launch in 2014, based on SCOC3 ASIC [8]) can reach with very similar functionalities with a power consumption lower than 15 W, a mass of 5.2kg and a much smaller volume of $250(L) \times 150(H) \times 216(D)$ mm³.

For the future ESA is developing a multiprocessor general purpose chip, the *Next Generation Multi-Purpose Processor* (NGMP) based on a Quad-Core LEON4 [5, 6]. The first phase of the activity has been kicked off in 3Q2009 with Aeroflex Gaisler as contractor. The NGMP is based on a SPARC V8 compliant multi-core architecture and the objective is to have a standard product implemented in Deep Sub-Micron (DSM) CMOS (65 nm is today’s baseline), while ASICs in commercial Silicon technology are already available. The NGMP will include a large on-chip memory (128-bit wide Level-1 cache, Level-2 cache of 256kB to 2MB depending on the available technology), Space Wire interface, Ethernet, UARTs, PCI 2.3, general purpose input and outputs together with debug interfaces.

6.3 Trends in space electronic systems: configurable & programmable systems

A number of observable trends has been noted in recent space missions. Complexity of functions for on-board avionics means a steep increase in number of complex ICs, and among those, number and functions of programmable components (especially FPGAs) is very high. Looking at different

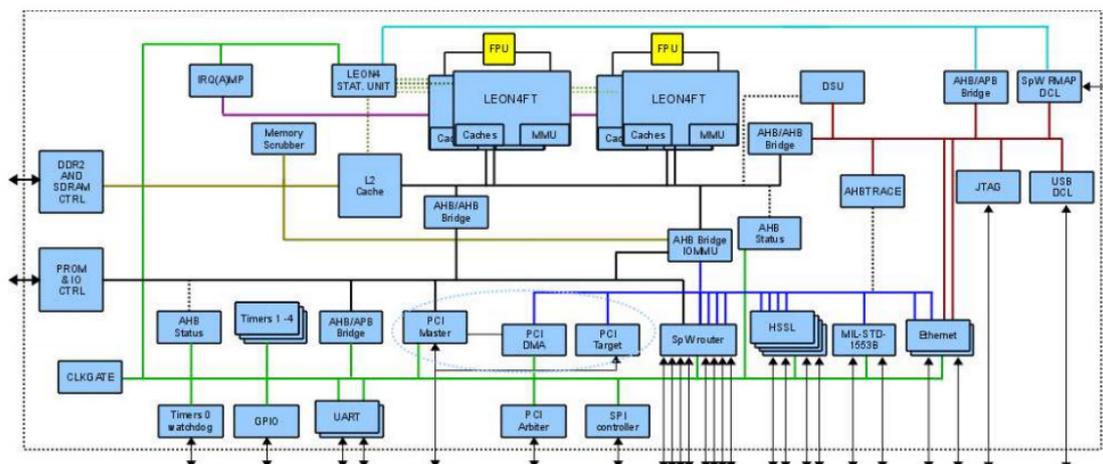


Figure 5. Next generation microprocessor — block scheme.

classes of missions, Telecommunication and Navigation use the largest number of ICs, with some missions having several hundreds of ASIC.

The aim of space electronic designer is often to prefer ASICs with respect to FPGAs, for a number of reasons:

- FPGAs tend to bring uncertainties in design and deployment flow, since there is the misplaced idea that some functions can be changed “last minute” without taking into account the verification work needed to guarantee work’s quality.
- The total Ionizing Dose requirements of 100 Krad (equivalent to 15-year telecom mission) leaves only one possible choice for FPGA: microsemi (ACTEL) antifuse, that are subject to US Department of Defense Export Regulations (ITAR).
- The space FPGAs are one time programmable, very expensive and power hungry devices, that need additionally dual power regulation.
- The latest generation of FPGAs (both One Time Programmable (OTP) or SRAM/FLASH based) come in very big or extremely dense packages, that make miniaturisation and reliable soldering difficult, while their power density makes PCB design more constraining.
- The latest generation of antifuse FPGA devices has relatively ‘soft’ (in radiation terms) embedded RAM, that makes use of EDAC/ECC mandatory.

One of the most welcomed features of antifuse FPGAs is the fact that they are live at power-on, so they don’t need additional NVRAM to store code compared to other intelligent components.

6.4 Trends in space integrated circuits technology

Affordable reliable space electronics component development with Digital and A/MS ASIC Technology feasibility is an endeavour that requires high forefront investments and relies on the dis-

tributed knowledge (an ‘ecosystem’ in modern terms) that is difficult to maintain in the European limited (in terms of volumes) and volatile (in terms of sustainability) space market.

In Europe there is one non-proprietary radiation hard digital ASIC technologies with a high Technology Readiness Level (TRL) due to its extensive space heritage. The ATMEL digital technology has proven itself in space and reached a TRL 9. For Analogue plus Mixed-Signal (A/MS) ASIC technology, there is one non-propriety technology, DARE, that achieves in the immediate future a high TRL 9 in 2013.

The requirements of modern spacecraft systems, forces space companies to seek higher level of performance and integration that can only be realised with custom designed digital and A/MS ASICs. While for digital ASICs the traditional procurement process can be maintained, this appears no longer the case for A/MS ASICs. In the traditional supply chain the responsibilities of the component supplier could be clearly identified and demonstrated with space qualification of the ASIC. For the full custom design for mixed-signal ASICs, required for the higher integration of the space equipment functions, the responsibilities of the ASIC designer, ASIC supplier and users appear to interweave, leading to a fragmentation of the traditional component supply chain. In order to assure the quality of the product and put due responsibility for each step in the ASIC manufacturing ESA is investigating the Process Capability Approval (PCA) quality system.

An indication of the complexity of the space ASIC supply chain is shown in the figure below, where each step in the ASIC development, manufacturing and qualification is indicated. The ‘classical’ discrete parts procurement flow is indicated, which through the A/MS ASIC development by space companies is difficult to maintain. The rationalisation of this supply chain is under investigation at ESA to ensure the continued affordable supply of high-reliability and performance components.

ESA is fostering the development of Design Against Radiation Effects (DARE) “portable” library to ensure functionality, reliability and radiation tolerance of developed components [14, 15]. DARE provides the digital design kit (synthesis library and back-end services), analogue design kit (Analogue library with radiation simulation models) and A/MS building blocks, through affiliated companies. DARE currently targets the UMC 180 nm CMOS technology. The porting of the technology to XFAB 180 nm is under development and the DARE/XFAB ESCC capability approval is under discussion. The A/MS IP core developed by the affiliated companies are also portable, to ensure the continued supply of radiation tolerant building blocks for manufacture at suitable foundries.

7 Future technologies for space electronics at ESA

Future activities at ESA aim at securing supply of radiation hard parts to the European space industry, towards development of A/MS supply chain with the ECSS PCA standard and thanks to user group support to 350nm CMOS technologies AMS/ON-SEMI/XFAB.

Particular focus shall be given to A/MS technology with radiation characterisation and modelling, with development of ad-hoc “generic” Single Event Transients (SET) simulation tool. For science missions (like the JUICE Jupiter mission) development of high radiation tolerance (Mrad) D+A/MS technology with DARE/UMC is expected, together with extension of voltage range of

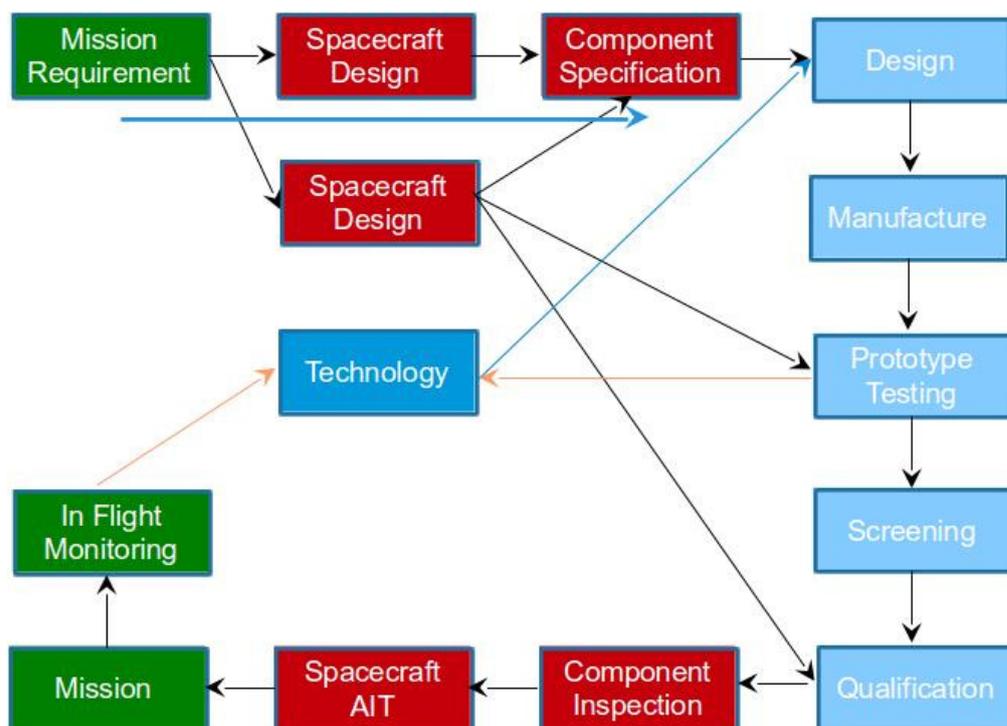


Figure 6. Development flow for Digital and A/MS ASICs in space projects.

DARE/UMC (to include CAN/LVDS interfaces on chip) and widening of A/MS building blocks libraries for DARE/UMC.

Development, qualification and deployment of ASIC technology to European Foundries: XFAB/ IHP/ LFoundry will be targeted to eventually provide full qualified (following standard methods approved by European Committee for Space Standardization — ECSS — [4]) supply chain to European electronic parts manufacturers and users (see [12, 13]). Full qualification of D+A/MS 250 nm and 130 nm SiGe BiCMOS technology from IHP and 150 nm SOI CMOS technology from ATMEL and digital 65 nm CMOS technology from ST will be necessary to maintain competitiveness for the high performance/low power devices (see [10, 11]).

Space grade 32bit microcontrollers are under development, to replace FPGAs in many designs allowing flexibility and full control of design changes. European reprogrammable, rad tolerant (SRAM) FPGA is under development from ATMEL.

ESA/ESTEC maintains and distributes under ESA licenses a small catalogue of digital IP cores, which comprise typical digital functions used in space applications (space communication Telemetry and Telecommand (TMTC), Error Detection and Correction (EDAC), SpaceWire, CAN, LEON2-FT sparv V8 processor, space On-Board Data Handling (OBDH), etc). ESA/ESTEC provides this “IP cores” service as an attempt to:

- counteract obsolescence and discontinuity of existing space standard ASICs, thus helping to guarantee the availability of some key functions in a technology independent format (“soft format”).

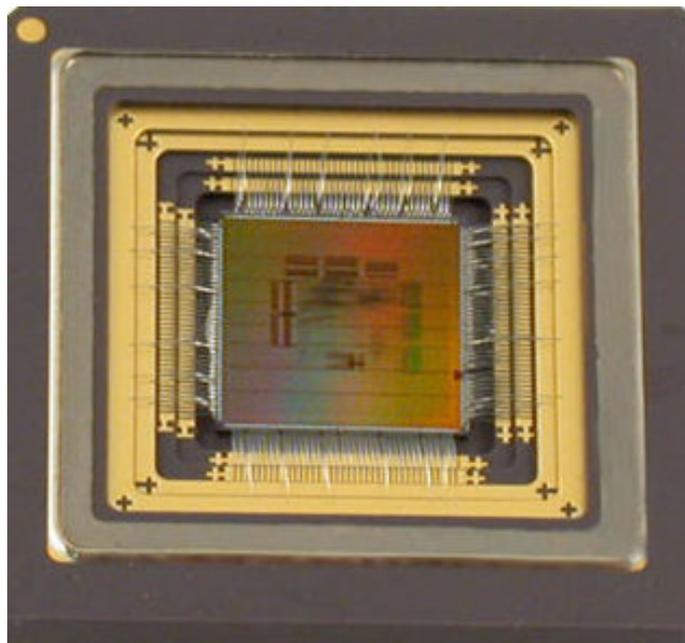


Figure 7. The LEON-2 processor (ATMEL AT697F).

- reduce costs of large IC developments (e.g. Systems-on-Chip) by re-using already designed and validated IC functions.
- promote and consolidate the use of standardized functions, protocols and/or architectures (e.g. SpaceWire, CAN, TMTC, etc).
- centralize IP users' feedback to improve quality of existing IPs and identify future needs.

The ESA IP cores can be licensed for space research and/or commercial use, under specific conditions (depending on the IP ownership) to companies based in ESA member and participant states.

References

- [1] ESA, *General information*, <http://www.esa.int>.
- [2] ESA, *Microelectronic research*, <http://www.esa.int/TEC/Microelectronics/>.
- [3] ESA, *Avionics architectures and related R&D*, <http://www.esa.int/TEC/OBCDH/>.
- [4] ECSS working groups, *ECSS - A Single Set of European Space Standards*
<http://www.ecss.nl/forums/ecss/dispatch.cgi/home/docProfile/100451/d20010730131425/No/t100451.htm>.
- [5] ESA, *The ESA Next Generation Microprocessor (NGMP)*, development based on LEON4-FT,
<http://microelectronics.esa.int/ngmp/ngmp.htm>.
- [6] M. Fernandez, R. Gioiosa, L. Fossati, M. Zulianello, E. Quiñones and F.J. Cazorla, *Assessing the Suitability of the NGMP Multi-core Processor in the Space Domain*, in the *12th International*

Conference on Embedded Software (EMSOFT), Tampere (Finland), October 7–12, 2012
http://people.ac.upc.edu/equinone/docs/emsoft_2012.pdf.

- [7] A.V. Sanchez, G. Furano, M. Ciccone, F. Guettache, C. Monteleone and C.Taylor, *Leveraging serial digital interfaces standardization: the RASTA reference architecture facility at ESA*, in *International SpaceWire Conference 2008*, <http://2008.spacewire-conference.org/downloads/Papers/Onboard%20Equipment%20%20Software/Viana%20Sanchez.pdf>
- [8] Astrium, *Description of the SCOC3 ASIC*,
<http://www.astrium.eads.net/en/equipment/scoc3.html>.
- [9] ESA, *The Space Environments and Effects Network of Technical Competences (SEENoTC)*,
<http://space-env.esa.int/index.php/SEENoTC.html>.
- [10] B. Bancelin, *Development of the ATMEL 150 nm CMOS Technology for Space*, in proceedings of the *4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications*, Noordwijk, The Netherlands, 26-28 August 2012.
- [11] L. Hili, L. Dugoujon, P. Roche, F. Malou and P. Perdu, *Deep sub micron 65nm program Perspectives for the next generation satellites*, in proceedings of the *2nd ESA Workshop on Advanced Flexible Telecom Payloads*, Noordwijk, The Netherlands, 17-19 April 2012.
- [12] R. Scholz, *IHPs SiGe BiCMOS technologies for RF and mixed-signal space applications*, in proceedings of the *4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications*, Noordwijk, The Netherlands, 26-28 August 2012.
- [13] F.E. Teply et al., *Radiation hardness evaluation of a 0.25 μm SiGe BiCMOS technology with LDMOS module*, in proceedings of the *Radiation and Its Effects on Components and Systems 2011*, Seville, Spain 19-23 September 2011
- [14] G. Thys, *Radiation Hardened Mixed-Signal IP with Dare Technology*, in proceedings of the *4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications*, Noordwijk, The Netherlands, 26-28 August 2012.
- [15] S. Redant et al., *Radiation test results on first silicon in the design against radiation effects (DARE) library*, *Nucl. Sci. T.* **52** (2005) 1550.