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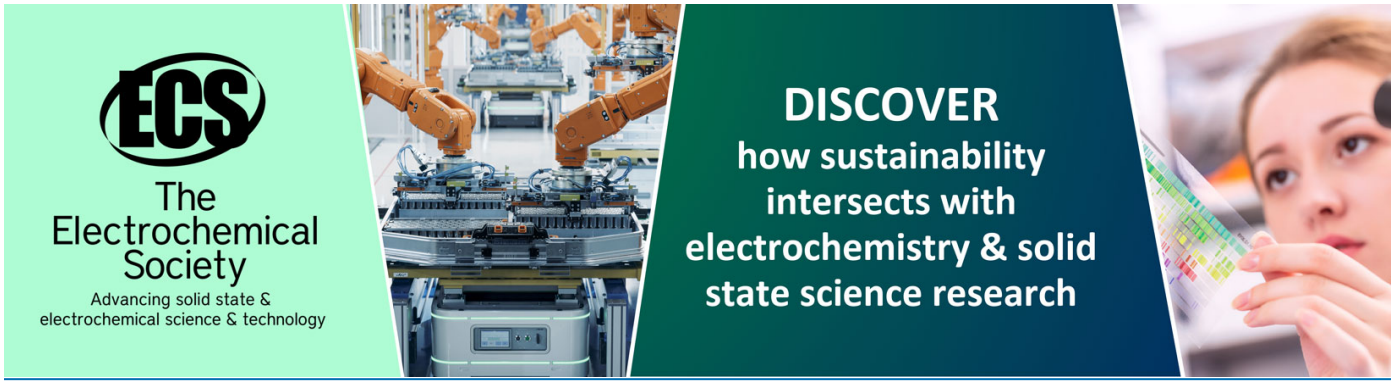

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Prototype linear voltage regulators for the ABC130 front-end chip for the ATLAS Inner Tracker Upgrade

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ABSTRACT: The power distribution systems considered for the ATLAS Inner Tracker Upgrade include linear voltage regulators on the front-end chips. In the paper we present two designs: a classical voltage regulator based on an NMOS transistor as the pass element, and an LDO voltage regulator employing a PMOS device. Both prototype regulators have been implemented in the 130 nm CMOS process and are foreseen to be integrated in the ABC130 front-end chip. In the paper the designs as well as the pre- and post-radiation test results for both prototypes are presented and discussed.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout

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1 Introduction

The lifetime of the present ATLAS Semiconductor Tracker will be limited due to the radiation damage to the silicon strip sensors as well as to the front-end electronics. The expected ten-fold increase of the nominal luminosity after the LHC High Luminosity Upgrade will results in proportional increase of radiation levels in the Inner Detector region. In order to provide the same pattern recognition capability at much higher density of particle tracks and to increase the radiation resistance of the new Inner Tracker a ten-fold higher granularity, approximately, will be required for the silicon strip detectors. Increasing granularity of the sensors will result in proportional increase of the number of front-end electronics channels located on the detector modules.

The concepts of the detector modules for the future Inner Tracker are well advanced and prototype modules have been built already [1, 2], though using an intermediate development version of the front-end chip ABCN25 [3]. The increase of the number of front-end channels puts stringent constraints on the power dissipation in the front-end chips and on the efficiency of the power distribution system, which introduces large amount of material into the tracker volume. Currently, two alternative power distribution systems are being developed; a system with serial powering of silicon strip detector modules [4] and a system with one or two DC-DC conversion stages placed on the detector modules [5]. For each of these two possible systems linear voltage regulators will be integrated in the front-end chip.

A new front-end chip ABC130 being designed in a 130 nm CMOS process is compatible with either of the two powering schemes. In this paper we report on two designs of the linear voltage regulators using the 130 nm CMOS process to be included in the ABC130 design. Both voltage regulators are meant to maintain a constant voltage of 1.2 V at the output. The nominal output current is assumed to be around 70 mA.

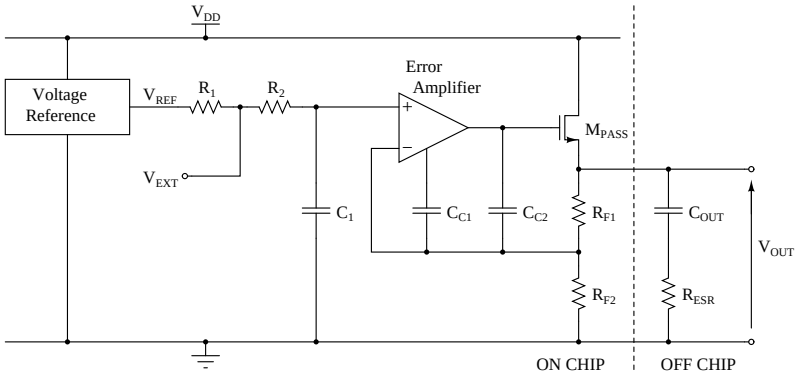

Figure 1. Schematic diagram of the linear voltage regulator prototype based on a zero-V_{th} *n*-channel pass transistor.

2 Low-dropout regulator using an *n*-channel MOS device for voltage regulation

2.1 Design of the NFET-based voltage regulator

The first of the two linear voltage regulators presented in this paper is based on a zero-V_{th} *n*-channel pass transistor. Figure 1 shows a schematic diagram of the proposed classical linear voltage regulator. The design consists of the following blocks: bandgap voltage reference circuitry with the RC filter (R_1, R_2 and C_1), error amplifier, pass transistor (M_{PASS}), resistive sensing network (R_{F1}, R_{F2}), compensation network (C_{C1}, C_{C2}) and external output capacitor C_{OUT} (with non-zero R_{ESR}).

The voltage reference circuit is expected to provide a constant voltage of 637 mV. In order to assure good reference voltage quality the output from the bandgap circuit is additionally filtered with a passive RC network consisting of two identical resistors ($R_1 = R_2 = 50\,\mathrm{k\Omega}$) and capacitor $C_1 = 1\,\mathrm{pF}$, fully integrated on the silicon die. The compensation network is necessary to obtain the stability of the presented voltage regulator and it is realised with two capacitors ($C_{C1} = 2\,\mathrm{pF}$ and $C_{C2} = 1.2\,\mathrm{pF}$). Both capacitors are also integrated on the chip. The sensing network is realised with two polysilicon resistors R_{F1} and R_{F2}. The ratio of these two resistors defines the output voltage according to the following formula:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_{F1}}{R_{F2}}\right), \tag{2.1}$$

where V_{OUT} is the output voltage and V_{REF} is the stable reference voltage provided by the bandgap circuitry. Output voltage of 1.2 V is obtained for R_{F1}/R_{F2} of 0.884. The resistor values have been arbitrary chosen to be $R_{F1} = 50\,\mathrm{k\Omega}$ and $R_{F2} = 56\,\mathrm{k\Omega}$. The load of the regulator includes a large capacitor $C_{OUT} = 100\,\mathrm{nF}$. This capacitor is too big to be implemented on the chip so it will be implemented as a small external SMD component, e.g. in the package 0603 or smaller. In the circuit used for simulation a resistor R_{ESR} of $10\,\mathrm{m\Omega}$ is added to take into account the effect of the Equivalent Series Resistance (ESR) of the capacitor. The value of R_{ESR} may vary significantly depending on the type of the capacitor technology and the external capacitors should be selected according to the R_{ESR}.

The error amplifier consists of three main blocks; the current reference circuit and two amplifying stages. A detailed circuit diagram of the error amplifier is shown in figure 2. The biasing cell

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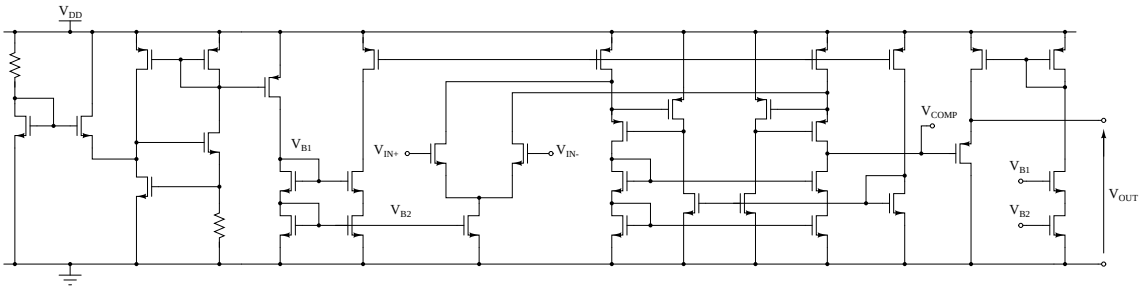

Figure 2. Schematic diagram of the error amplifier used in the linear voltage regulator based on the NMOS pass transistor.

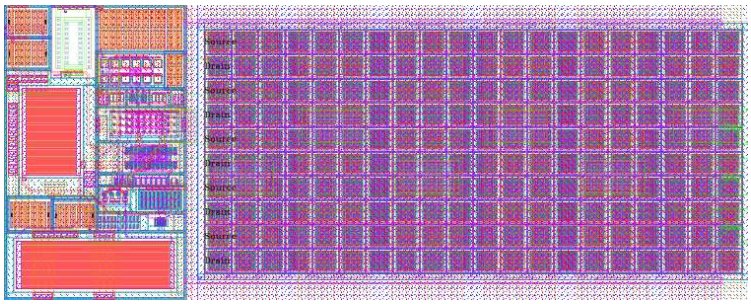

Figure 3. Layout of the linear voltage regulator employing a zero-V_{th} NMOS transistor as a pass device.

is realised using a threshold-referenced topology with a simple startup circuit. The V_{th}-referenced source technique [6] has been used to generate a constant current independent of the supply voltage. The first amplifying stage is implemented using a folded-cascode topology with the NFET input pair. Additionally, a significant boost of the voltage gain without loosing the amplifier's bandwidth has been achieved by applying the gain-boosting technique. The output stage is built as a classical source follower [7] based on a *p*-channel transistor. It provides a shift of the DC level and drives the large gate capacitance of the pass device.

The layout of the regulator is shown in figure 3. The design is compact and occupies an area of around 0.1 mm^2 (520 μm $\times$ 200 μm).

2.2 Test results of the NFET-based voltage regulator

In order to evaluate the performance of the voltage regulator the following characteristics have been measured: DC transfer characteristics, DC output characteristics, and transient response to a step of the load current. The irradiation tests have been performed using the CERN in-house X-ray generator. The prototype chips with the voltage regulators were mounted on PCBs and irradiated up to a Total Ionizing Dose (TID) of 200 Mrad within around 60 hours and then annealed at 100°C for 168 hours.

The very first pre-irradiation measurements showed that the reference voltage in all tested bandgap circuits was systematically lower by about 40 mV in comparison with the expected 637 mV. In addition, we observed that the value of the reference voltage increased monotonically with the TID. Therefore, the transfer and output characteristics shown in figure 4 were measured

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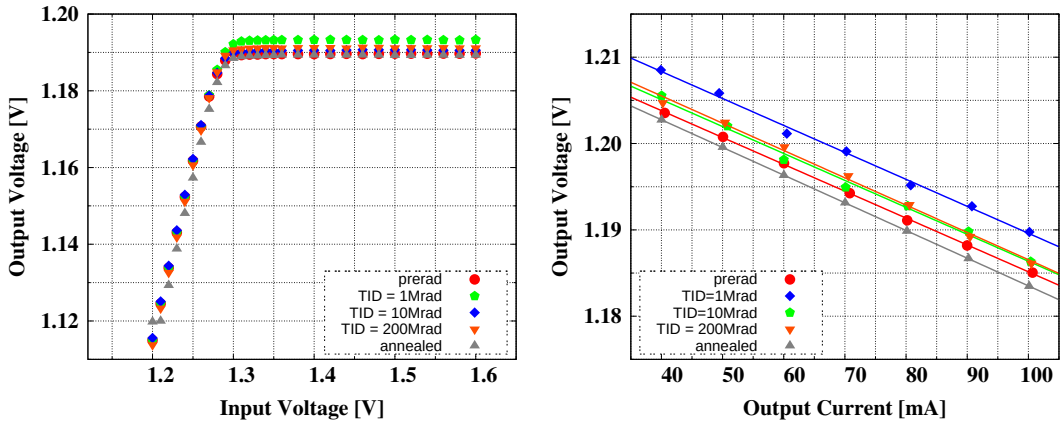

Figure 4. Transfer characteristics (left) and output characteristics (right) of the classical voltage regulator measured before the irradiation, after 1 Mrad, 10 Mrad, 200 Mrad of the TID, and after annealing.

with an external reference voltage in order to separate the radiation effects in the bandgap reference circuit and in the regulator itself.

The transfer characteristics was measured by sweeping the input voltage from 1.2 V to 1.6 V and measuring the output voltage. This measurement was repeated after each irradiation step and after annealing. The test was performed for the regulator loaded with a current of 70 mA. The slope of the transfer characteristics does not change noticeably after irradiation. The regulator provides a stable output voltage of 1.2 V for the input voltage ranging from 1.3 V to 1.6 V, the maximum supply voltage at which the thin gate oxide MOS transistors may be operated. The dropout voltage, the minimum source-to-drain voltage at which the pass transistor still regulates the output voltage, is 100 mV.

The output characteristics shown in figure 4 allow us to estimate the DC output resistance of the regulator. The characteristics were measured by applying different load to the output of the regulator and monitoring the output voltage. The output current was varied from 40 mA to 100 mA. The extracted DC output resistance is 370 mΩ and it does not change noticeably after irradiation. From simulation the output resistance was expected to be about 290 mΩ. The difference between the simulated and the measured output resistance may be partially explained by the resistance of long traces on silicon and on the PCB. In the final implementation the regulator will be integrated on the same silicon die as the analogue front-end electronics and the problem of parasitic resistances will be significantly reduced.

The transient response of the regulator to a step of the load current is presented in figure 5. In order to obtain these waveforms the test setup has been modified by adding a switched resistive load in parallel to the nominal load resistance enforcing the constant output current. For a 14.5 mA step of the output current the output voltage changes by 5.3 mV. Such a current step corresponds to the expected 20 % variation of the current consumption in the analogue front-end circuits of ABC130. The extracted output resistance is 360 mΩ, similar to the value extracted from the DC output characteristics.

The presented results confirm good transient performance of the regulator, which has been achieved by proper design of the error amplifier. In the simulations a unity-gain frequency of the

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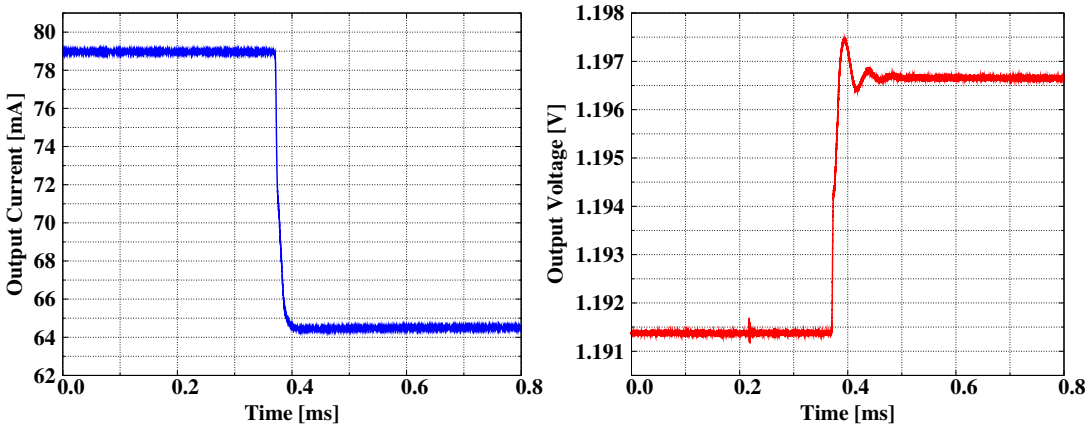

Figure 5. Measured transient response of the classical voltage regulator to a step of the load current.

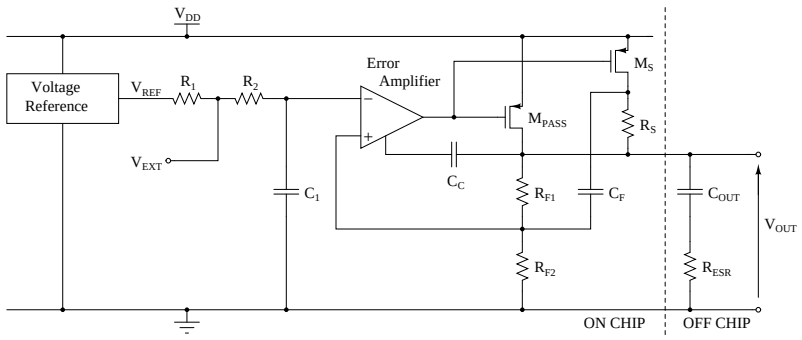

Figure 6. Schematic diagram of the linear voltage regulator prototype based on a *p*-channel pass transistor.

regulator of 126.5 MHz with a phase margin of 76° has been obtained. This guarantees a fast and smooth transient response without significant ringing.

3 Low-dropout regulator using a *p*-channel MOS device for voltage regulation

3.1 Design of the LDO voltage regulator

The second developed voltage regulator employs a PMOS transistor as a pass element. The output voltage has also been set to 1.2 V required for the analogue supply voltage of the ABC130 chip. A schematic diagram of the proposed voltage regulator is shown in figure 6. The entire circuit consists of the following blocks: bandgap voltage reference circuit, RC filter (R_1, R_2, C_1), error amplifier, pass PMOS transistor (M_{PASS}), sensing network (R_{F1}, R_{F2}), compensation network (M_S, C_F, C_C, R_S) and output capacitor C_{OUT}. The load capacitor is $C_{OUT} = 100$ nF. Such a capacitor has a non-zero ESR, which is very important for the circuit stability.

The bandgap circuit is the same as in the previously presented classical voltage regulator and the reference voltage can also be applied from an external source. The RC filter and the sensing network consisting of resistors $R_{F1} = 50\,\text{k}\Omega$ and $R_{F2} = 56\,\text{k}\Omega$ are identical as well. The W/L ratio of the PMOS pass transistor has been set to 15 mm/0.12 μm. In order to provide unconditional

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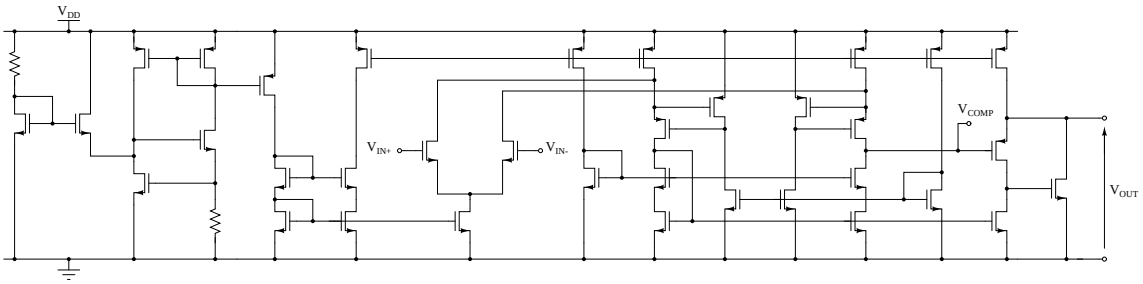

Figure 7. Schematic diagram of the error amplifier used in the linear voltage regulator based on the PMOS pass transistor.

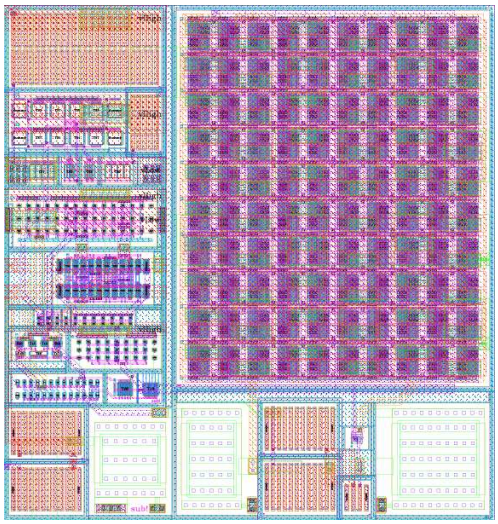

Figure 8. Layout of the linear voltage regulator employing a *p*-channel transistor as a pass device.

stability of the system a slow-rolloff frequency compensation has been introduced to the LDO circuit. The compensation network consists of the PMOS transistor M_S ($W_S/L_S = 1.0\,\mu m/0.16\,\mu m$), resistor $R_S = 6\,k\Omega$, feedback capacitor $C_F = 2\,pF$, and the compensation capacitor $C_C = 1.2\,pF$. The compensation scheme is based on the rolloff technique as described in [9]. This technique introduces a dominant half-pole whose magnitude rolls off as the square root of frequency, giving a phase shift of only 45°. A half-pole is realised by alternating poles and zeros with a constant frequency ratio. A detailed analysis of an LDO voltage regulator circuitry employing the slow-rolloff technique can be found in [10]. The most important point of this design is the stability of the circuit for a wide ESR range of the output capacitor.

The detailed circuit diagram of the error amplifier used in the LDO is shown in figure 7. The design is very similar to the one used in the classical voltage regulator. Small improvements have been made to the bias of the cascode current source. In order to decrease the output resistance of the second stage a super source follower has been used. The simulated value of the unity-gain frequency of the regulator is 60 MHz and the phase margin is close to 70°.
The layout of the LDO regulator is shown in figure 8. The presented design of the LDO voltage regulator is also very compact, with total area less than $0.04\,mm^2$ ($190\,\mu m \times 200\,\mu m$).

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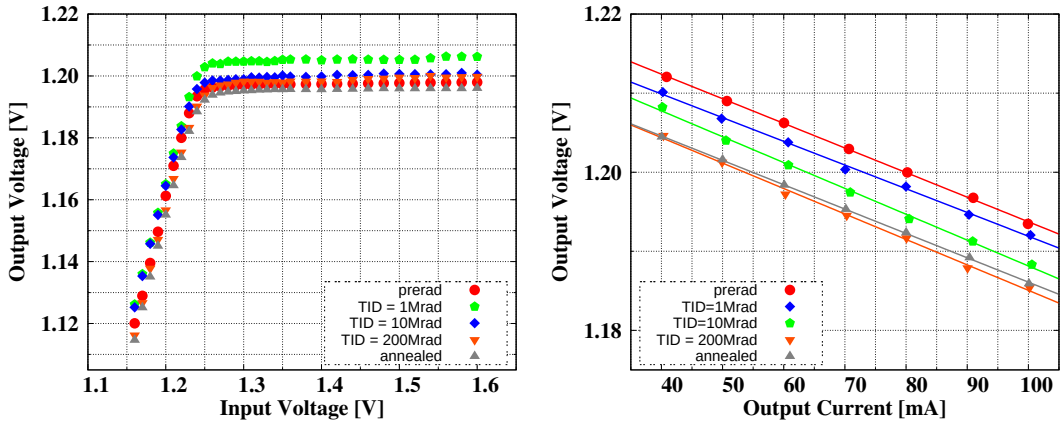

Figure 9. Transfer characteristics (left) and output characteristics (right) of the LDO voltage regulator measured before the irradiation, for the TID of 1 Mrad, 10 Mrad, 200 Mrad, and after annealing.

3.2 Test results of the LDO voltage regulator

Figure 9 shows the transfer characteristics measured for the LDO voltage regulator. The plots show the curves measured before irradiation, after 1 Mrad, 10 Mrad, 200 Mrad of the TID, and after annealing. The measurements were taken using an external reference voltage of 637 mV. The regulated output voltage for the stable V_{REF} remains close to 1.2 V after all the steps of irradiation. The measured dropout voltage is only 50 mV, so half of that of the previously discussed voltage regulator. This results in a wider input voltage range from 1.25 V to 1.6 V.

The output characteristics presented in figure 9 have been measured for a supply voltage of 1.5 V and an external reference voltage. The output resistance extracted from these curves is 260 mΩ and remains constant after irradiation independently of the TID. The measured output resistance for the LDO regulator is about two orders of magnitude higher than the value obtained from simulations. The discrepancy between simulation and measurement can be partially due to parasitic resistances in the test set-up and partially due to not accurate models provided by the technology vendors and used in the simulations. As has been already mentioned the parasitic resistances are expected to be reduced for the regulator integrated in the readout chip.

The transient response of the LDO to a step of the load current shown in figure 10 confirms good transient performance of the design. By using a simple switched current source a current step of $\Delta I_{OUT} \approx 14.5$ mA was applied. The output voltage fluctuation caused by the change of the load is $\Delta V_{OUT} \approx 5.4$ mV. The output resistance extracted from this measurement is around 370 mΩ, somewhat higher than extracted from the DC output characteristics.

4 Conclusions

The presented voltage regulators have been optimised according to the power supply requirements of the front-end electronics in the ABC130 chip being developed for the ATLAS Inner Tracker Upgrade. It has been demonstrated that efficient and radiation resistant voltage regulators can be implemented in the 130 nm CMOS process and can be integrated in the readout chip. Both investigated architectures, the one employing a zero-V_{th} *n*-channel transistor in the classical source

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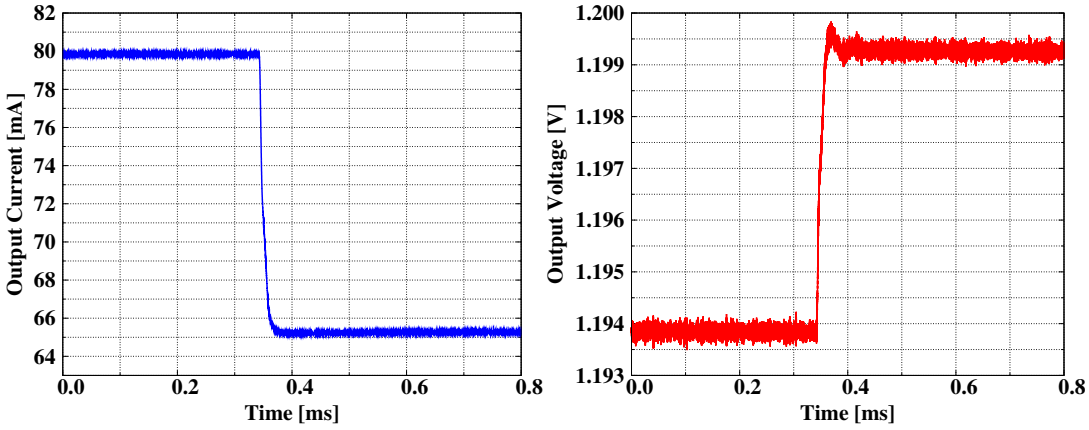

Figure 10. Measured transient response of the LDO voltage regulator to a current step applied at its output.

follower configuration and the other employing a *p*-channel transistor in the common source configuration provide very low dropout voltages of 100 mV and 50 mV, respectively. The tests of the prototypes have confirmed correct functionality of both voltage regulators. Both regulators meet the requirements concerning the level of the output voltage, output current range and voltage regulation. The irradiation tests up do 200 Mrad of the TID have proved satisfactory radiation resistance of the developed circuits, provided a stable external reference voltage is applied.

Acknowledgments

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