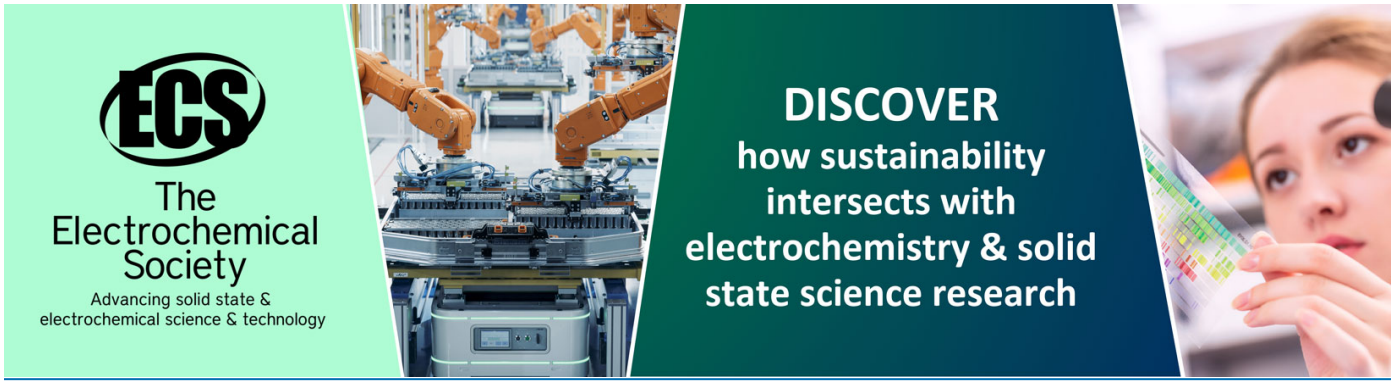
# A monolithic pixel sensor (TRAPPISTe-2) for particle physics instrumentation in OKI 0.2*μm* SOI technology





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# A monolithic pixel sensor (TRAPPISTe-2) for particle physics instrumentation in OKI 0.2$\mu m$ SOI technology

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ABSTRACT: A monolithic active pixel sensor for charged particle tracking has been developed within the frame of a research and development project called TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology). TRAPPISTe aims to study the feasibility of developing a monolithic pixel sensor with SOI technology. TRAPPISTe-2 is the second prototype in this series and was fabricated with an OKI 0.20$\mu$m fully depleted (FD-SOI) CMOS process. This device contains test transistors and amplifiers, as well as two pixel matrices with integrated 3-transistor and amplifier readout electronics. The results presented are based on the first electrical measurements performed on the test structures and laser measurements on the pixel matrices.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Particle tracking detectors

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## Contents



2012 JINST 7 C12028

## 1 Introduction

Silicon pixel detectors are currently used at the very center of high energy physics tracking systems. These sensors provide enough resolution to track subatomic particles while surviving in a very high radiation environment. Research into detectors for future tracking systems strives to improve the resolution and material budget of the detectors while still maintaining radiation hardness.

Current state-of-the-art silicon pixel detectors are hybrid detectors in which the sensor and readout electronics are fabricated separately and then bonded together afterwards. For pixel detectors, bonding is usually accomplished by bump bonding. This complicated procedure involves placing balls of solder at bonding sites in each pixel, aligning the sensor with corresponding bonding sites in the readout electronics and then melting the solder to form the bond. These hybrid techniques place limits on the minimum size of the pixels and on the minimum thickness of the detector as two wafers are required. Bump bonding is also a complex and expensive process that can represent the majority of the detector cost.

Monolithic detectors can provide a solution to improving the resolution and material budget of future detectors. In a monolithic detector, the sensor and readout electronics are fabricated together on the same wafer. This can lead to the development of thin detectors while avoiding the limitations and costs imposed by bump bonding. The TRAPPISTe (Tracking Particles for Particle Physics Instrumentation) project aims to study the feasibility of building such a monolithic detector in silicon-on-insulator (SOI) technology.

## 2 Silicon-on-insulator

SOI devices are built in a thin silicon active layer which sits atop a buried oxide layer. These two layers are developed on a thick handle wafer. The buried oxide layer provides insulation between

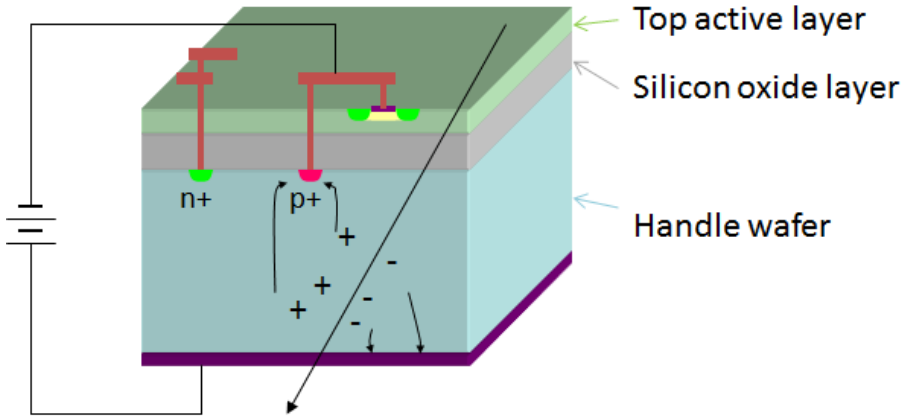


**Figure 1**. SOI wafer used as a monolithic detector. A sensor is created in the bottom handle layer and connected to the readout in the active layer with metal vias.

devices and also between the devices and the bottom bulk layer. This reduces parasitic capacitances and also allows for more compact layout, leading to reduced die area compared to a traditional bulk process. Due to the absence of parasitic structures in the bulk, SOI devices are radiation hard in regards to single event effects but the buried oxide is susceptible to total dose effects.

For standard SOI circuits, the bottom handle layer only serves as a mechanical substrate and is otherwise not used. To build a monolithic detector in an SOI wafer, an implant is created in the handle layer to create a detector. The readout electronics is developed in the top active layer and the two are connected together by metal vias through the buried oxide. In this way, a sensor and readout electronics can be realized in a single wafer without the need for external bonding.

Using SOI to build a monolithic detector offers the advantages of using SOI circuitry as well as the the possibility to optimize the device layers. The handle wafer can be chosen to be high resistivity silicon to build the sensor and the active layer can be made of lower resistivity silicon better suited for electronic devices. However, new process steps are required to develop these detectors and the proximity of the sensor and electronics can lead to interference between the two parts. In particular, the sensor needs to be biased to create the depletion region. The bias is applied as a voltage to the back plane of the SOI wafer. The resulting electric field in the handle wafer can affect the devices in the top layer. This is referred to as the backgate effect and can lead to undesirable changes in circuit operation.

## 3 TRAPPISTe

The TRAPPISTe project is a research and development project with a goal of developing a monolithic particle detector in SOI technology. The first TRAPPISTe devices were fabricated at the Université catholique de Louvain's WINFAB facility. WINFAB provides a $2\mu m$ FD-SOI process with one metal layer and a p-type handle layer 25Ωcm. With this technology a first TRAPPISTe-1 pixel matrix with 3-transistor readout was built and a charge amplifier study was performed [2].

TRAPPISTe-2 was developed as part of the SOIPIX collaboration [1]. The SOIPIX collaboration provides access to OKI Semiconductor technology through multi-project wafer runs. The OKI



2012 JINST 7 C12028

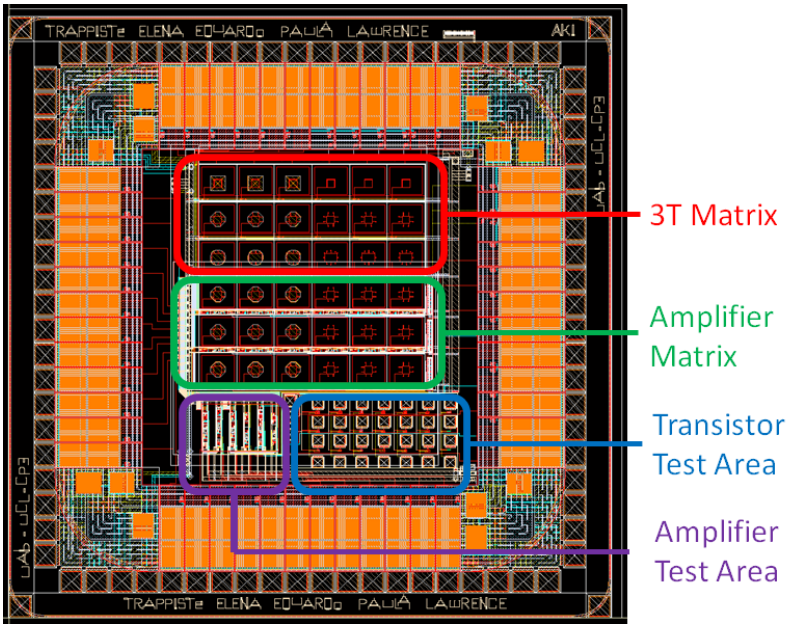


**Figure 2**. TRAPPISTe-2 layout containing test structures and pixel matrices.

process is a 0.2$\mu m$ with five metal layers. High resistivity n-type handle wafers of 10 000Ωcm were provided. Figure 2 shows the layout of the TRAPPISTe-2 chip. In the bottom section of the layout are test structures which are not connected to any sensor. A test transistor area contains individual transistors with access pads for measurement with a probe station. Next to the transistor area is an amplifier test area holding standalone amplifiers which are meant for electrical characterization.

The top part of the layout contains two monolithic pixel matrices. These matrices contain detector implants in the handle wafer which are connected to integrated readout electronics in the top active layer. The first pixel matrix contains a 3-transistor (3T) based readout structure and the second matrix contains a charge sensitive amplifier readout.

## 4 Transistor backgate effect

The transistors in the test area were characterized with a probe station to observe the backgate effect. Figures 3 and 4 show the shift in transistor operation for core source-tied nMOS and pMOS transistors. The nMOS transistor is particularly affected by the voltage applied to the back plane. At a back voltage of 20V, the transistor is already on even for a gate voltage of 0V. As a result, proper circuit operation is only possible at low back voltages. This limitation in back voltage is an important consideration for a monolithic detector as the back voltage is used to deplete the sensor in the handle wafer. A low back voltage results in a smaller depletion region and less charge collected.

## 5 3T matrix

The 3T matrix is 6 column by 3 row matrix comprised of 150 $\mu m\times$ 150 $\mu m$ pixels with integrated three transistor readout circuits. The 3T readout is based on a standard architecture shown in



2012 JINST 7 C12028

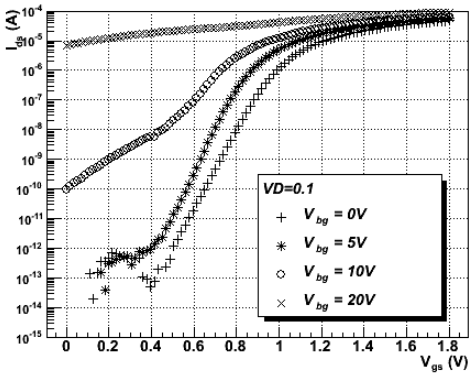


**Figure 3**. NMOS transistor voltage shift at different back voltages.

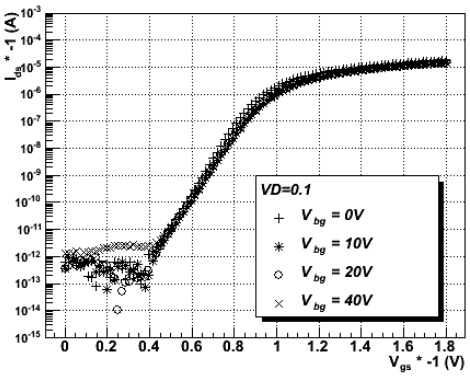


**Figure 4**. PMOS transistor voltage shift at different back voltages.

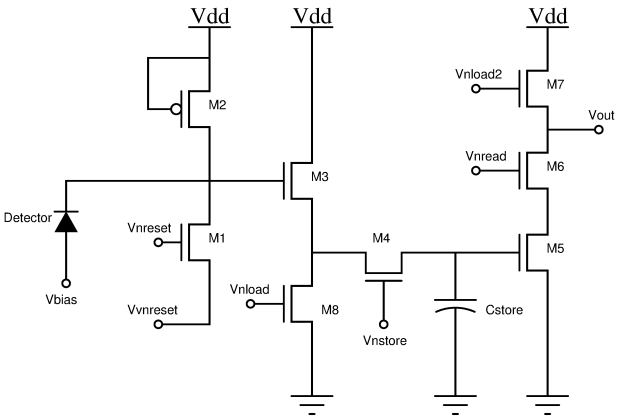


**Figure 5**. 3T readout circuit with storage capacitor.

figure 5. A reset transistor M1 places a bias voltage on the detector node. The signal at the detector node is buffered by transistor M3 and the selection transistor M4 is used to store the signal onto a 37.5fF storage capacitor. The stored signal can be read out onto the pixel output by the read transistor M6. The readout procedure is controlled by a shift register that activates one column at a time for readout.

Electrical characterization was performed on the 3T circuits. DC transfer curves were measured by sweeping the input voltage of the readout circuit and recording the output at different back voltages. The curves exhibit a shift in operation point as the back voltage is increased up to 5V of back voltage after which the circuit operation remains stable up to 12V (figure 6).

The 3T matrix was tested with a laser to verify its response to charge stimulation. An infrared laser of 1060nm wavelength was focused on each pixel with the use of a micrometer precision moving stage. Each pixel was reset to a known reset voltage before the laser was pulsed. After a reset, the change in the pixel output with and without the laser present was compared. Although the applied back voltage was low resulting in a limited depletion zone, there was a significant change in the targeted pixel. Figures 7 and 8 show the change in output when the laser is centered on pixel number 2 and pixel number 6 respectively, showing that the laser position can be tracked.

2012 JINST 7 C12028

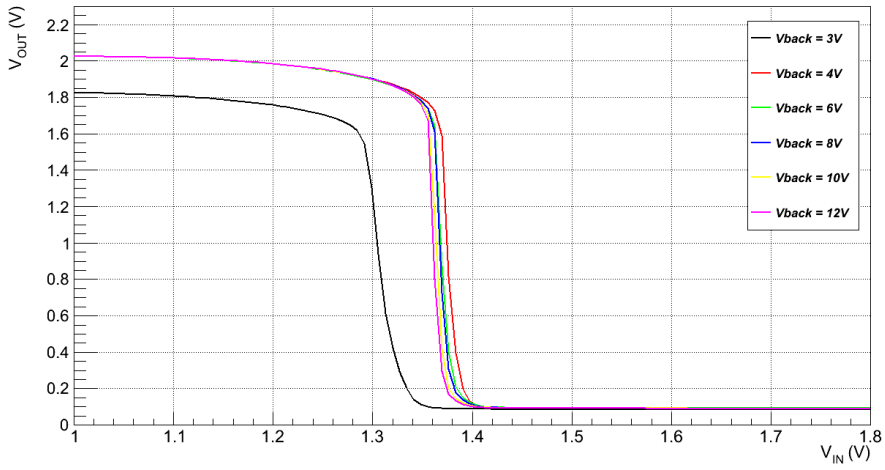


**Figure 6**. 3T transfer curve with varying back voltage.

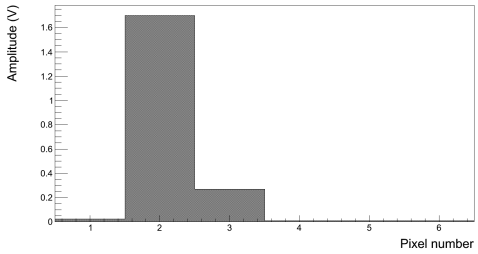


**Figure 7**. Pixel output change with laser targeted on Pixel 2.

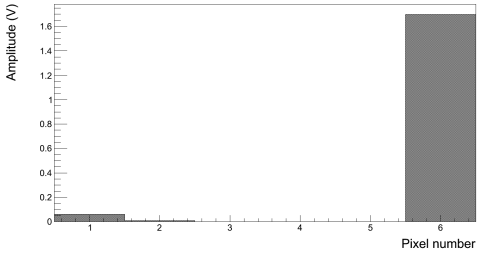


**Figure 8**. Pixel output change with laser targeted on Pixel 6.

## 6 Charge sensitive amplifier matrix

A charge sensitive amplifier was designed based on a $g_m/I_D$ methodology. The amplifier is based on a folded cascode core architecture with bias transistors as shown in figure 9. The charge generated in the detector is integrated onto the feedback capacitor CF and a transistor MF is implemented as a feedback resistor. The design of the amplifier follows a $g_m/I_D$ methodology that sizes the amplifier transistors based on the detector and performance specifications. The methodology was first validated with TRAPPISTe-1 [3] and the same design was followed in TRAPPISTe-2.

Stand alone amplifiers were produced as well as a small matrix with integrated sensor implants and amplifiers. The stand alone amplifiers were not connected to any sensor implant. They were tested with a pulse generator and a test capacitor placed in series at the amplifier input to generate an input charge. Figure 10 shows the output response of the amplifier to about 24 000 electrons at different back voltages. One can notice the decrease in signal amplitude and change in signal risetime as the back voltage increases. The amplifier can only operate at low back voltages which limits the depletion width in a monolithic detector.

Despite the decrease in signal amplitude with increasing back voltage, the integrated detector and amplifier pixel matrix was responsive to a laser source. The amplifier matrix contains six columns of $150 \times 150\,\mu m^2$ pixels with integrated amplifiers. An infrared laser source was focused on a particular pixel and the sensor in the handle wafer was depleted with an applied back voltage.



2012 JINST 7 C12028

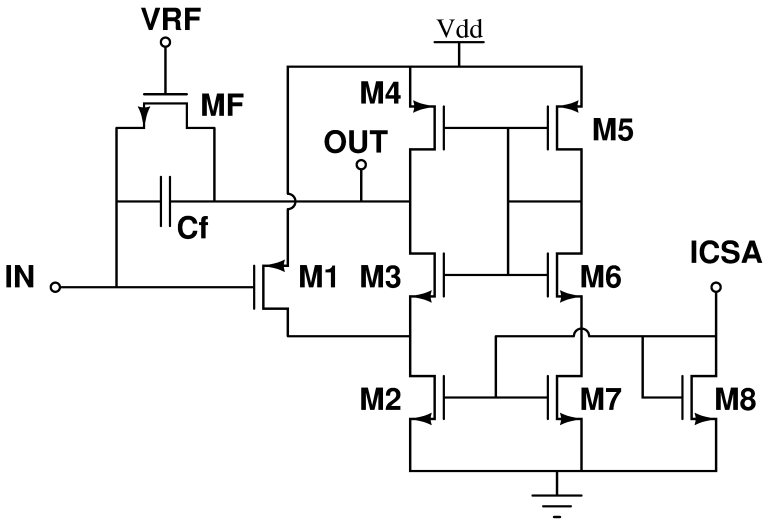


**Figure 9**. Charge sensitive amplifier architecture based on a folded cascode core.

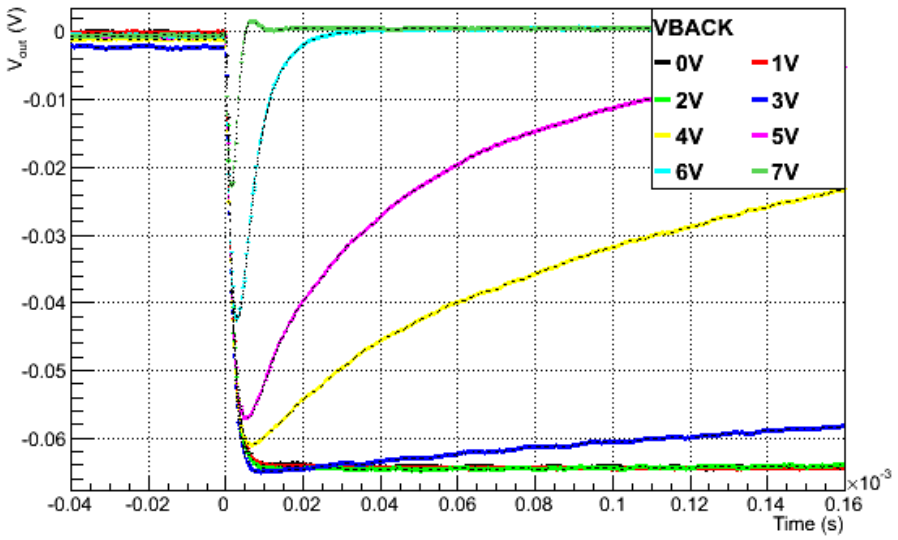


**Figure 10**. Measured transient output of the CSA at different back voltages.

A plot of the amplitude versus the back voltage at constant laser intensity is shown in figure 11 showing the interplay between the increasing depletion width and backgate effect. Initially, the increase in back voltage and depletion zone results in an increase in the output signal as more charge is collected and amplified. However, at around 5V of back voltage, the amplitude begins to decrease as the amplifier performance degrades due to the back gate effect.

Setting the back gate voltage to 5V to achieve the maximum voltage gain, the laser was focused on different pixels to see if it could be tracked across the pixel matrix. For a 10 000 $\Omega cm$ resistivity substrate, this results in a depletion width of 100 $\mu m$. Figures 12 and 13 show the response of the six pixels in the targeted row when the laser is focused on the pixel in the first column and third column respectively. In spite of the low depletion voltage, the targeted pixel can be identified by the three times larger amplitude response.



2012 JINST 7 C12028

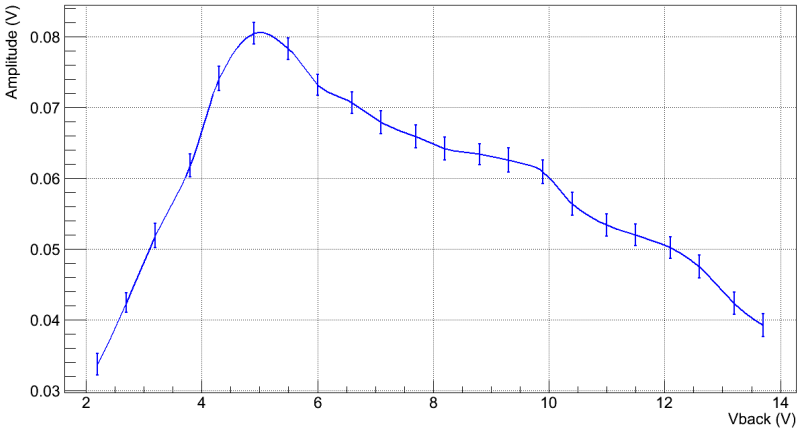


**Figure 11**. Measured output amplitude of integrated amplifier with laser source at different back voltages.

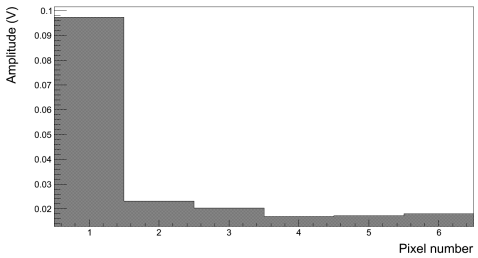


**Figure 12**. Amplifier pixel output with laser targeted on Pixel 1.

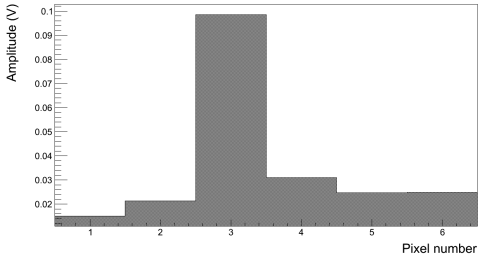


**Figure 13**. Amplifier pixel output with laser targeted on Pixel 3.

## 7 Conclusion

TRAPPISTe-2, a prototype monolithic particle detector using silicon-on-insulator technology, has been developed in an OKI $0.2\mu m$ FD-SOI process. A detector implant is made in the bottom handle wafer and connected to readout electronics in the top active layer. The two parts are insulated from each other by a buried oxide layer.

Measurements on test transistors and amplifiers show that circuit operation is adversely affected by the backgate effect. When a voltage is applied to the chip back plane, which is required to deplete the sensor in the handle wafer, a potential is generated at the buried oxide underneath the circuits in the top active layer. This potential is referred to as the backgate voltage and affects the operation of the circuits. Future TRAPPISTe devices will incorporate process techniques such as buried implants to shield the sensitive electronics from the backgate effect [4].

The backgate effect places a limit on the voltage that can be used to deplete the sensor resulting in a smaller depletion region and limiting the amount of charge collected. Laser tests on the TRAPPISTe-2 chip show that as the back voltage is increased initially from 0V to 5V, the readout electronics show an increase in charge collected as the depletion area is widened and the backgate effect is minimal. After 5V however, the backgate effect dominates and the amplifier response degrades. Despite the low applied back voltage, the monolithic pixel is responsive to laser excitation and it is possible to track the position of the laser with the pixel matrix. This shows promise for future TRAPPISTe devices which will employ techniques to mitigate the backgate effect.



2012 JINST 7 C12028

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2012 JINST 7 C12028