

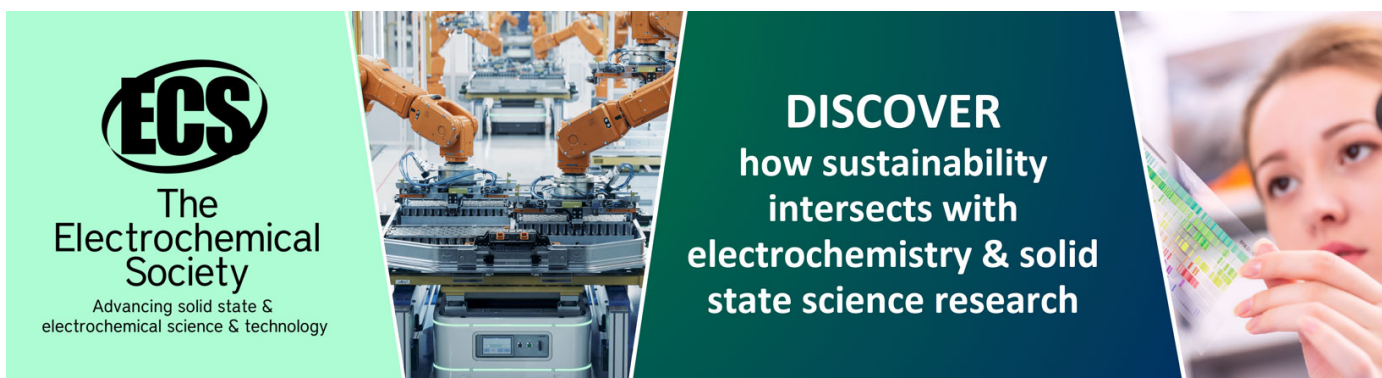
Testing and firmware development for the ATLAS IBL BOC prototype

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Testing and firmware development for the ATLAS IBL BOC prototype

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ABSTRACT: For the coming upgrade pixel detector of the ATLAS experiment at the Large Hadron Collider a redesign of the current data readout is necessary. To communicate with the additional 448 front-end chips assembled in the Insertable B-Layer (IBL) new FPGA based readout cards consisting of a Back of Crate card (BOC) and a Read Out Driver (ROD) have been developed. This paper describes the firmware and hardware development of the new BOC prototype. Firmware tests, like electrical and optical loopback and communication tests with the new IBL front-end modules and the ROD will also be presented.

KEYWORDS: Optical detector readout concepts; Data acquisition circuits; Data acquisition concepts

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Contents

1	Introduction	1
2	IBL BOC card	1
3	Firmware development	2
3.1	BCF firmware	2
3.2	BMF firmware	4
3.2.1	TX path	5
3.2.2	RX path	6
4	Testing	6
4.1	Powering tests and first configuration	6
4.2	Path tests	6
4.2.1	TX path	6
4.2.2	RX path	8
4.3	Optical FE-I4 readout	8
5	Conclusions	8

1 Introduction

The Large Hadron Collider (LHC) at CERN is the largest and highest-energy particle accelerator in the world. One of the four experiments at the LHC is ATLAS. The pixel detector is a subsystem of the ATLAS detector [1] and generates a large quantity of data to be used for identification and reconstruction of primary and secondary vertices.

During the shut-down 2013/14 a new pixel layer called the Insertable B-Layer (IBL) will be installed together with a new beam pipe. This innermost layer of the pixel detector will provide 448 front-end chips (FE-I4) [2] serving about 12 million pixel cells [3]. To meet the communication requirements of these chips the readout system must be updated. On the off-detector side the Read Out Driver (ROD) and the Back of Crate card (BOC) are responsible for data acquisition and processing. Figure 1 shows an overview of the complete IBL readout chain. The BOC card is responsible for the detector timing and the signal conversion between detector, higher-level readout and ROD card. BOC and ROD card were completely redesigned and are equipped with state-of-the-art FPGA technology.

2 IBL BOC card

The new IBL BOC card which is shown in figure 2 is based on the previous Pixel BOC version and FPGAs are used for the signal processing on the card. Three modern state-of-the-art Xilinx Spartan-6 FPGAs [4] are mounted on the IBL BOC card, which make it very flexible for future tasks due to the possibility of easy reprogramming.

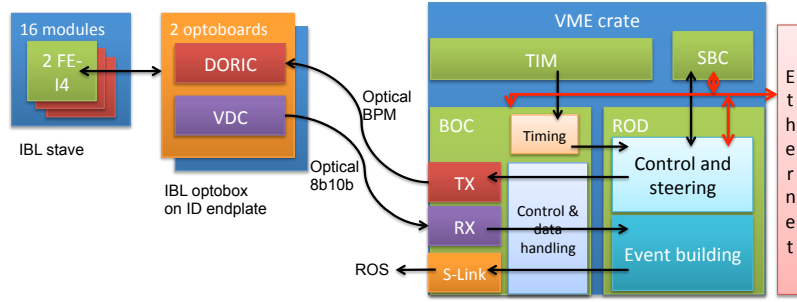


Figure 1. Schematic showing the complete IBL readout chain.

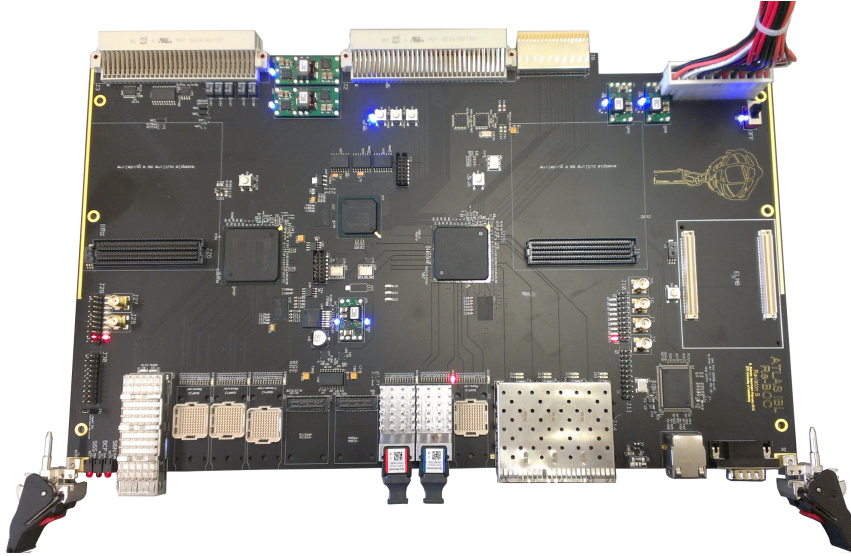


Figure 2. Picture of the new revision B IBL BOC card prototype.

The block diagram in figure 3 shows all connections between the FPGAs and their peripherals. The BOC Control FPGA (BCF) provides the control logic for all modules on the card and the Ethernet interface. The two BOC Main FPGAs (BMF) are responsible for the signal processing on the card. This includes the signal conversion between the electrical interface to the ROD card as well as the optical interface to the detector and the higher level readout. The optoelectric conversion of the signals to and from the detector is done by commercial SNAP12 or custom-made TX-plugins [5]. The connection to the higher-level readout is made with commercial (Q)SFP modules. (Q)SFP and SNAP12 modules are standardised and widely used in the telecommunication market.

3 Firmware development

3.1 BCF firmware

The BCF firmware contains the central control units of the IBL BOC card. It can be controlled either over the Setup Bus from the ROD card or over Ethernet from any network capable PC. A block diagram of the BCF firmware is shown in figure 4.

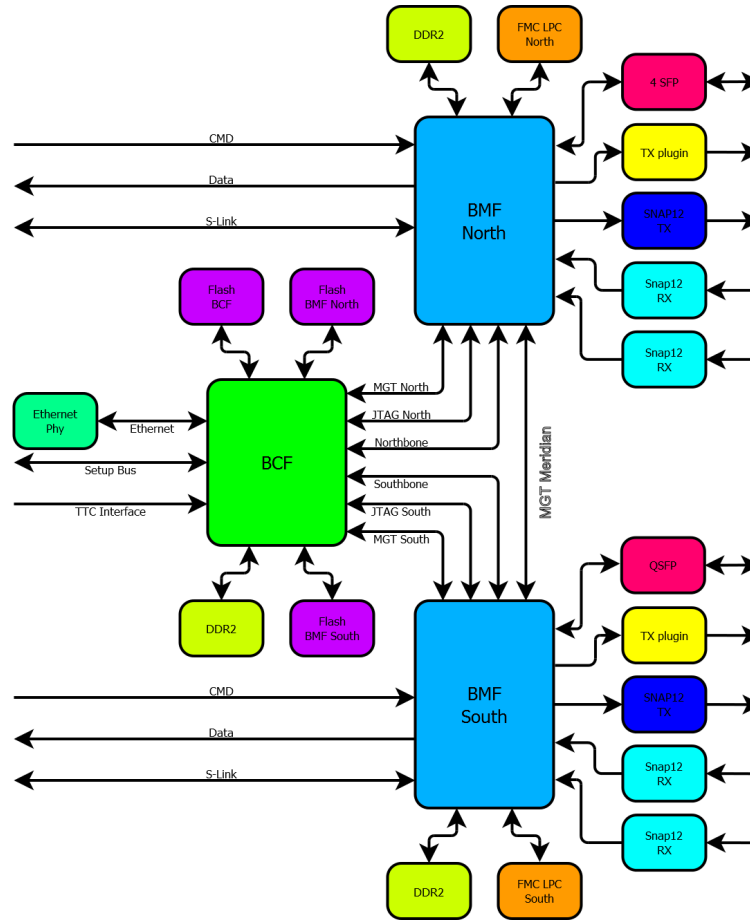


Figure 3. Block diagram of all components and their connections on the IBL BOC card.

The central part of the firmware consists of the internal Wishbone bus [6]. The router and arbiter of this bus allow several bus masters to connect to the slaves. The Wishbone bus is an open source standard and it is used for its flexibility and simplicity.

Access to this internal bus can be accomplished over the Setup Bus, which is the main control interface, as well as over an internal Microblaze processor, which is running on the BCF. The Microblaze processor handles the Ethernet communication. It is planned to use it for diagnostic features and self testing of the card.

The Setup Bus is an asynchronous bus with 8-bit data and 16-bit address width, therefore a maximum of 64k memory can be accessed over this bus. The Setup Bus is the main control interface between the IBL BOC card and the ROD card.

A register bank controlling several hardware modules is connected to the internal bus system. An important hardware module is the “ProgUnit”, which controls the programming of the BMF. After power-up the ProgUnit loads the bitstream of the BMF firmware from an on-board flash memory into the BMF. This concept allows easy firmware upgrade and recovery. New signal processing firmware can be loaded via the VME interface.

Another hardware module controls the clock generation and distribution on the BOC card. It will be used to align the BOC system clock to the LHC clock.

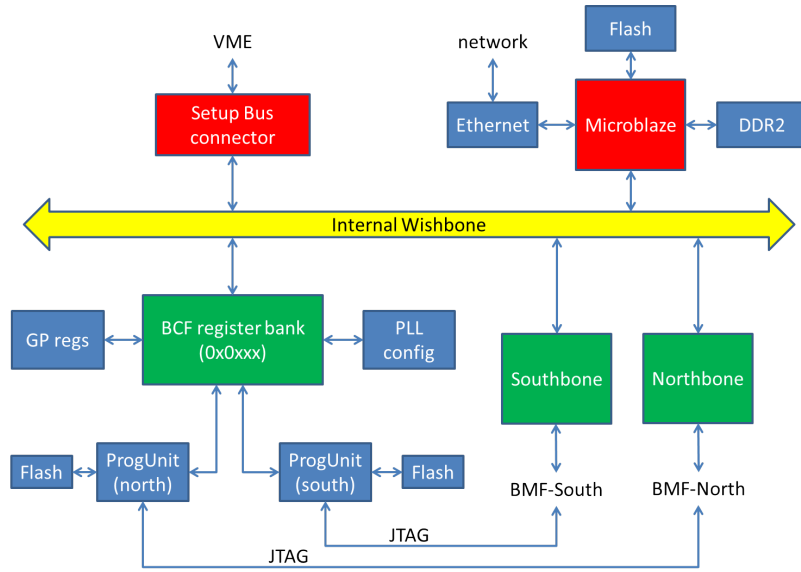


Figure 4. Block diagram of the BCF firmware modules.

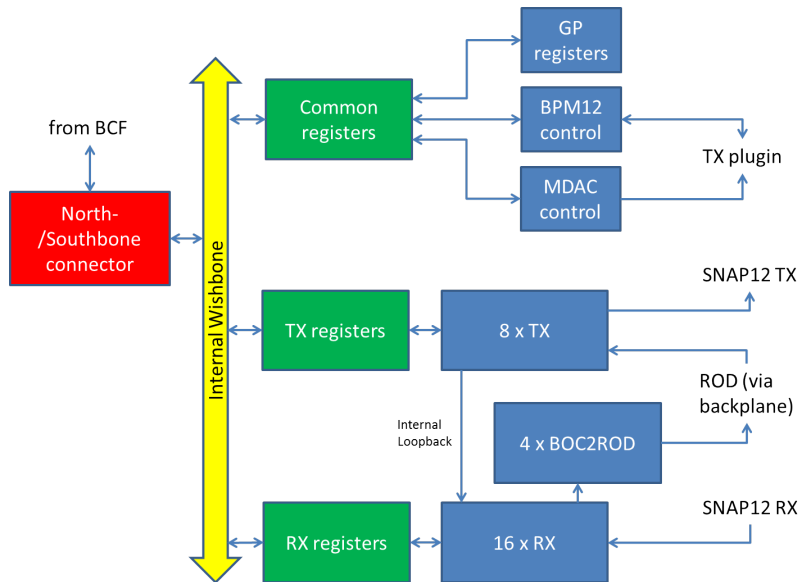


Figure 5. Block diagram of the BMF firmware modules without the S-LINK parts of the firmware.

3.2 BMF firmware

The BMF firmware is optimized for high speed data processing and monitoring. Each BMF is responsible for 8 TX and 16 RX channels to/from the detector as well as the S-LINK interface to the higher-level readout. Figures 5 and 6 show the block diagram of the BMF and the TX/RX channels.

As in the BCF, all hardware modules are controlled over register banks. The common register bank has registers to control the old TX-plugin and provides some version information like firmware version and build-date. The TX and RX register banks have status and control registers for all channels.

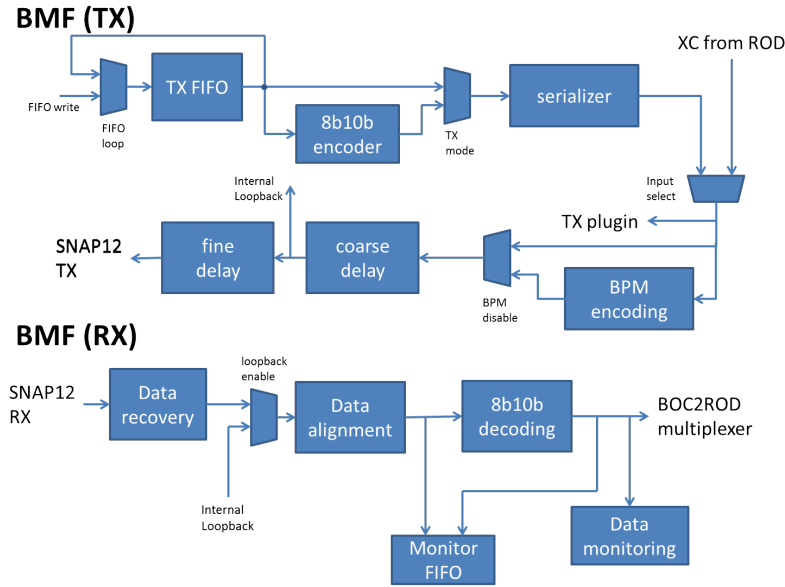


Figure 6. Block diagram of the RX and TX paths in the BMF firmware.

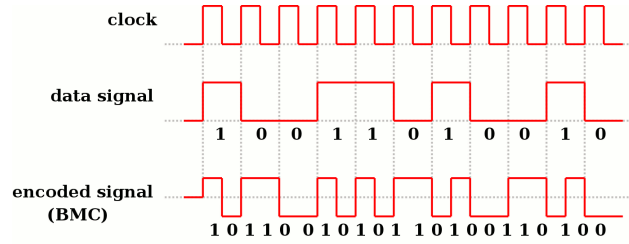


Figure 7. Example showing the BPM encoding.

3.2.1 TX path

The TX path is responsible for the detector timing and control. The 40 MHz LHC system clock and the serial data are encoded into a single bi-phase mark (BPM) data stream per module. An example how the BPM encoding works is shown in figure 7. Each bit starts with a transition. A '1' in the data stream corresponds to a second transition in the middle of the bit, whereas a '0' has no transition. The coarse and fine delay blocks are used to adjust the timing of the detector modules with respect to the bunch crossing, to compensate propagation delays.

In the normal operation mode the TX path takes the data from the ROD. For standalone and debugging purposes a transmission FIFO has been implemented to inject data if no ROD is available. Also a serial 160 MBit/s 8b10b-encoded data stream (see next section) for loopback tests can be generated.

The most tricky part in the TX path is the implementation of the fine delay. It is used to delay the outgoing signals in steps of around 30 ps. There are several methods of implementing this fine delay. The first method uses the internal propagation delays of combinatorial logic inside the FPGA (multiplexer chain). The second method uses IODELAY blocks which are available in the FPGA I/O blocks. Both methods have been implemented and need to be tested.

3.2.2 RX path

The new front-end chips use an 160 MBit/s 8b10b-encoded serial data stream. This encoding is DC-balanced and allows easy data recovery. Special transmission symbols (called k-word) are used to indicate states such as idle, start-of-frame or end-of-frame. These symbols are unique and help to align the incoming data on the BOC card.

First, the incoming data is 4-times oversampled, to do an edge detection and data recovery. The algorithm of the data recovery is described in a Xilinx application note [7]. Then the data stream is parallelized and a word alignment is performed. The decoded data of 4 modules is collected and sent over the 12-bit wide BOC-to-ROD-interface. It has 8 data bits, 2 address bits and 2 control bits (valid, k-word). The interface to the ROD has four of these 12-bit wide busses and is running at 80 MHz allowing a maximum data rate of 5 GBit/s between the cards.

4 Testing

All tests have been performed in a test setup containing the IBL BOC and ROD card in a VME crate, an optoboard and a FE-I4 single chip card. A block diagram of the setup is shown in figure 1. The tests can be divided into several subtests. The following sections will describe the results of these tests.

4.1 Powering tests and first configuration

After receiving the first prototype of the IBL BOC card the first powering tests were done to check if all hardware components on the card were working as expected. Afterwards the FPGAs have been programmed with the firmware and first communication tests have been performed.

4.2 Path tests

The path tests following the successful communication tests are divided into tests of TX and RX path.

4.2.1 TX path

The TX path has been tested to check if the BPM encoding works successfully and the signal shape meets the requirements. This is important because the Optoboard [8], which converts between optical and electrical interfaces in the detector, has some requirements to the signal quality. The duty-cycle of the signal should be between 45 and 55 percent. Also the signal power on the optics needs to be verified.

Figure 8 shows the duty-cycle of the signals to the detector. It was measured with an oscilloscope for all 8 TX channels on the IBL BOC card at the zero-delay setting. Both fine delay implementations distort the duty-cycle notably. For the IODELAY-implementation it is outside the specified range. The routing inside the FPGA was clearly identified as the reason for this distortion. Firmware versions without fine delay implementation can use registered outputs (IOB flip-flops). This results in a clean 50 percent duty-cycle. If the fine delay is being implemented there are a lot of FPGA-internal routing resources inbetween the last flip-flop and the output pad of the FPGA, which have a high impact on the duty-cycle.

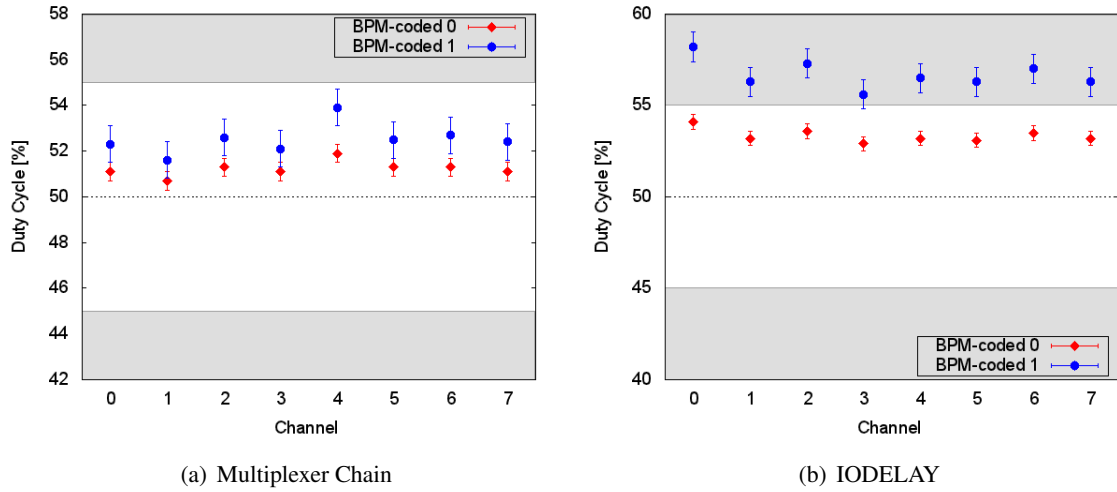


Figure 8. Duty-cycle of the transmitted signals with implemented fine delay block for all channels at the zero-delay setting.

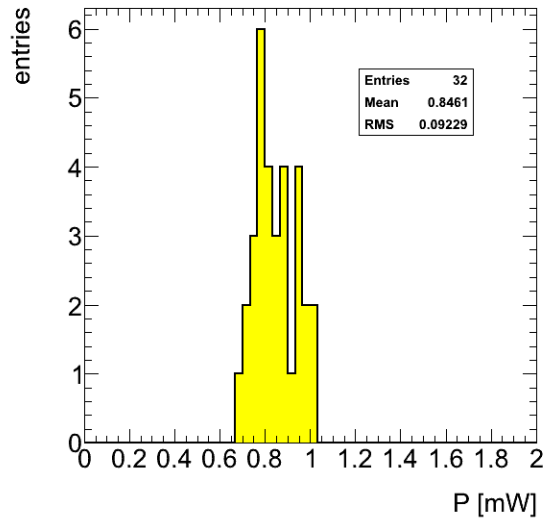


Figure 9. Output power of the SNAP12 transmitters measured with an optical power meter.

To ensure the correct decoding of data, the Optoboard needs at least -6 dBm of input power. As the attenuation of the optical fibers increases due to irradiation, the output power of the optical plugins is an essential parameter. Figure 9 shows the output power of the SNAP12 transmitters. The minimal output power is around 0.65 mW which corresponds to -1.9 dBm. So the maximum attenuation of the fiber can be 4.1 dB. In [9] a radiation-induced attenuation of 0.04 dB was estimated. Together with the length-induced attenuation of around 0.5 dB it is below the allowed attenuation of the fiber.

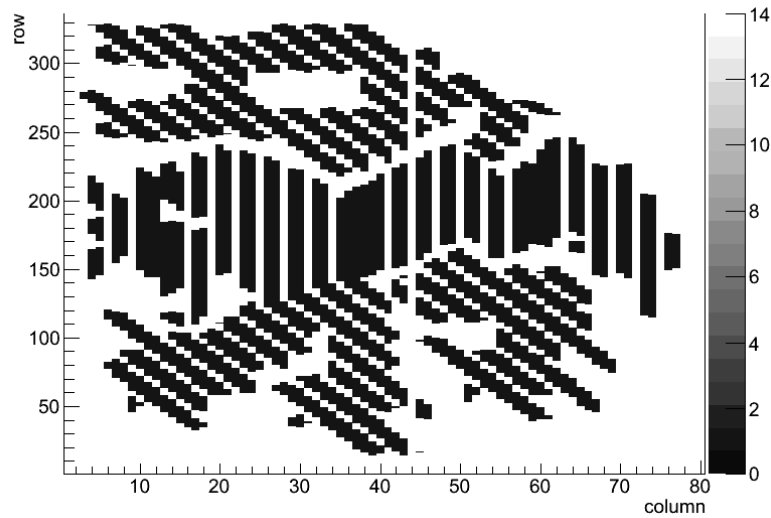


Figure 10. Digital scan showing the 90° rotated logo of the University of Wuppertal.

4.2.2 RX path

The RX path was tested by generating an 8b10b data stream in the TX path. The RX path can now be tested with a FPGA-internal loopback as well as with an external loopback over an optical fiber to test all RX functions of the card. Both tests have been successful. Then a bit-error-rate measurement for the BOC-to-ROD-interface has been performed. Over 2 Terabyte of data have been exchanged between BOC and ROD without any error. This results in a bit error rate less than $5 \cdot 10^{-14}$.

4.3 Optical FE-I4 readout

The last test of the card was a readout test over the full optical and electrical chain consisting of BOC, Optoboard and FE-I4. This is done with the same setup that will run in the IBL detector. Figure 10 is the result of a digital scan showing a lion as the logo of the University of Wuppertal. It was generated by configuring the FE-I4 to fire certain pixel cells and read out these cells after a trigger command. With this test the complete communication with the FE-I4 has been tested and the IBL BOC card can operate together with the FE-I4.

5 Conclusions

As a conclusion the IBL BOC card is on a good way. The firmware development has nearly finished and the most important parts of the firmware have been extensively tested. But there are many possible improvements to do. The current fine delay implementations are not a good choice regarding the duty-cycle of the signal to the detector. So new implementations of the fine delay have to be found and tested. The measurements of the SNAP12 output power help to make a decision if the SNAP12 plugins can be used as optical transmitters.

Acknowledgments

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