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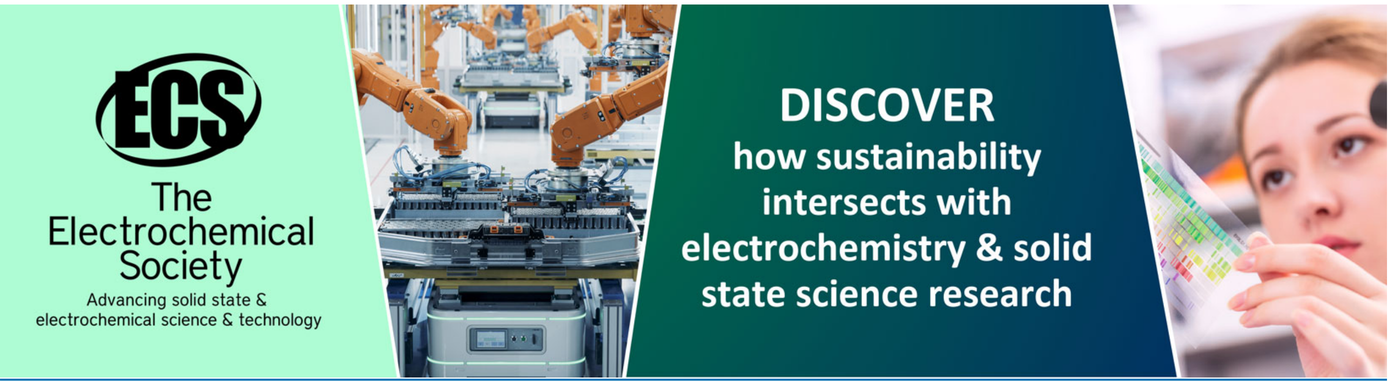

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A 0.18μm CMOS low-power radiation sensor for UWB wireless transmission

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ABSTRACT: The paper describes the design of a floating gate MOS sensor embedded in a readout CMOS element, used as a radiation monitor. A maximum sensitivity of 1 mV/rad is estimated within an absorbed dose range from 1 to 10 krad. The paper shows in particular the design of a microelectronic circuit that includes the floating gate sensor, an oscillator, a modulator, a transmitter and an integrated antenna. A prototype of the circuit has recently been simulated, fabricated and tested exploiting a commercial 180 nm, 4 metal CMOS technology. Some simulation results are presented along with a measurement of the readout circuit response to an input voltage swing. Given the small estimated area of the complete chip prototype, that is less than 1 mm^2, the chip fits a large variety of applications, from spot radiation monitoring systems in medicine to punctual measurements or radiation level in High-Energy Physics experiments.

KEYWORDS: Microdosimetry and nanodosimetry; VLSI circuits; Analogue electronic circuits; Pixelated detectors and associated VLSI electronics

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Contents

1 Introduction

The readout circuit for the sensor is designed to asynchronously trigger an all-digital Ultra-Wide Band (UWB) transmitter operating in a 0–5 GHz band, with a repetition frequency dependent on the radiation level. Particularly, for medical applications, a 403 MHz band has been chosen to let the circuit be implantable in-vivo inside a patient. In fact, by using this band, the human body — mostly composed of water — shows the least attenuation of radio waves.

The floating gate MOS sensor has been recently characterized for a 2V variation of the threshold voltage, when powered at 3.3 V. Irradiation tests were performed providing an equivalent dose of 100 rad at a time and the floating gate was reprogrammed each time after the charge was removed from the gate by the absorbed radiation. In this way the process was repeated up to an equivalent total irradiation dose of 10 krad. Within this range, a maximum sensitivity of 1 mV/rad was estimated. The figure 1 shows the 3D layout of the sensor, used for physical simulations, and the paper also shows the design of a readout circuit that includes a modulator and a transmitter. Figures 2 to 4 show a prototype that will be interfaced with an external power supply and to an antenna for pulse transmissions, to provide a preliminary proof-of-concept validation. An integrated antenna was also designed and implemented into this prototype to further testing purposes. Given the small estimated area of the complete chip prototype, comprising the antenna, i.e. less than 1 mm^2, the chip might fit a large variety of applications, from spot radiation monitoring systems (High-Energy Physics experiments might benefit of this concept) to the more common medical fields.

The chip architecture allows to test separately the sensor cell or to connect it to the readout circuit for a validation of the entire circuit. The chip is fabricated using the TowerJazz semiconductor commercial 180 nm technology.

This design has been split into two prototypes that implement different solutions for the internal blocks. Moreover, only the second submission includes a prototype of an integrated antenna. Figure 5 shows some measurements of the first prototype modulator along with a simulation of an upgraded version of the same circuit, which was included in the second submission.

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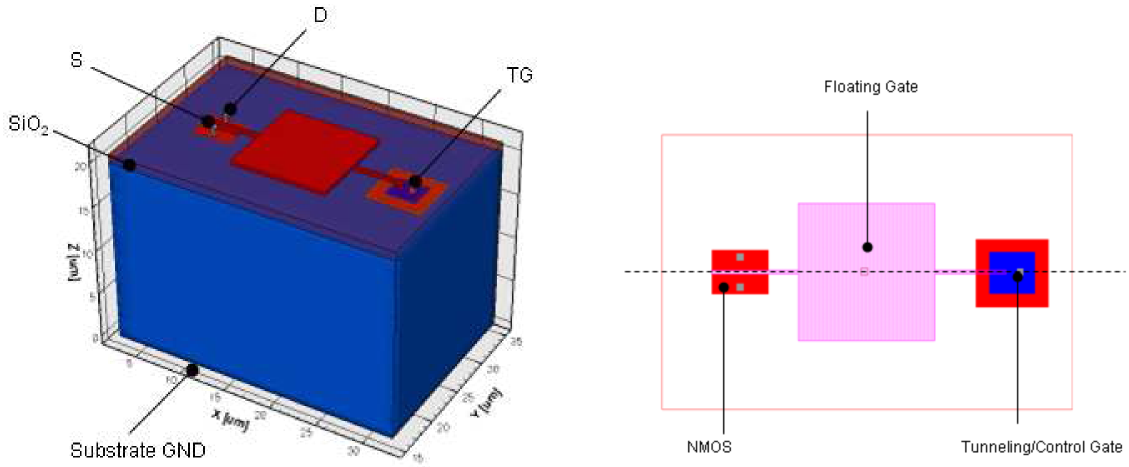

Figure 1. Design of the layout and 3D view of the dosimeter using a floating gate over an NMOS transistor. The Tunneling Gate (TG), Drain (D), Source (S) are also shown.

Other designs, chip fabrications and measurements on similar circuits were recently executed at the "Istituto Italiano di Tecnologia", Center for Space Human Robotics in Turin, Italy, to demonstrate the feasibility of the proposed event-driven asynchronous Ultra-Low Power UWB transmission [1–3]. In addition, the use of floating gate devices as radiation sensors [4–7] has been in-depth investigated in the past by the Science and Technology Facility Council of the Rutherford Appleton Laboratory (RAL), U.K., using commercial FET components [8–12].

2 The floating gate concept

The radiation detection principle of the floating gates shows some similarities to those of standard MOSFET [4–7]. In MOSFETs based dosimeters, the amount of accumulated dose is indirectly measured via the shift of the threshold voltage. A high value of the threshold voltage shift is related to a high density of charge trapped within the SiO_2 oxide interposed between the control gate and the bulk. Consequently, a high sensitivity to radiation dose is normally achieved via a thick gate oxide. A large bias is normally needed to increase the sensitivity but this must be balanced with the need of integrating on the same technology the sensing elements and the readout electronics. In addition, the threshold voltage shift in conventional MOS transistors cannot be easily annealed. Conversely, floating gate devices can be fabricated using a standard CMOS technology featuring double polysilicon layers and can be operated with zero bias during irradiation [9]. This is especially advantageous in terms of fabrication cost, low power applications and is compatible with monolithic fabrication processes. The operating principle of a floating gate dosimeter is the discharge of the floating gate through the absorbed radiation. The floating gate is initially pre-charged by the injection of electrons — holes — via a tunnelling process. Then, depending on the sign and amount of charge stored in the floating gate, the electric field in the surrounding SiO_2 is modified in intensity and direction. Hence, the charge created in the SiO_2 interface by the ionizing radiation discharges the floating gate and causes a backshift of the MOS's threshold voltage. This voltage shift is indirectly related to the amount of deposited radiation dose. The sensitivity, linearity

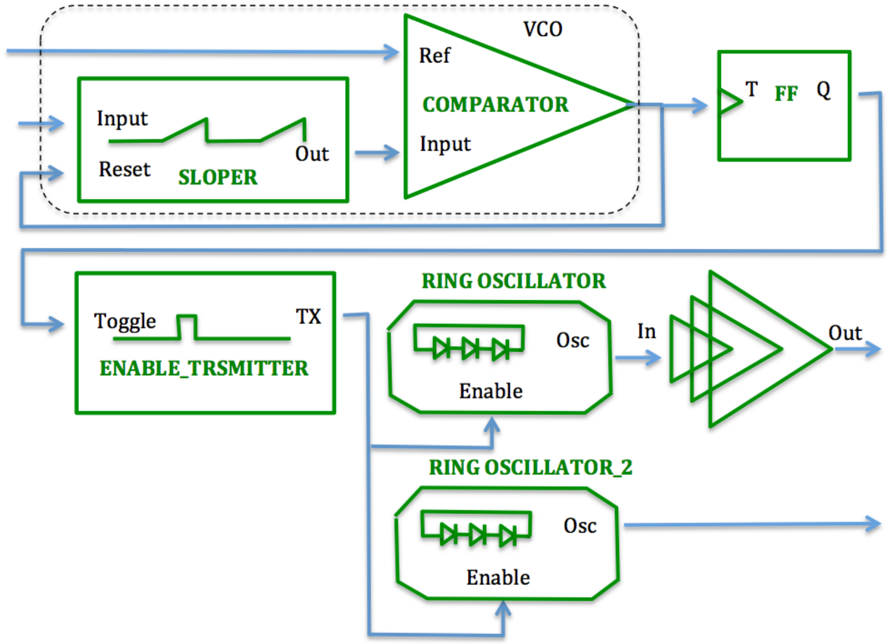

Figure 2. Basic block diagram of the Sigma-Delta modulator used as a readout circuit for the floating gate sensor cell.

and noise characteristics of the sensor depend on several factors such as geometry, fabrication process, size and biasing. The sensor device proposed and simulated here consists of a single NMOS transistor.

3 The Sigma-Delta architecture

It is here described the design of a Sigma-Delta-like modulator used as a readout circuit to interface with the analog output voltage level of the sensitive cell. The sensor output voltage is then converted to a frequency shift of a free running Voltage Controlled Oscillator (VCO).

The entire circuit is based on 3.3 V MOS transistors, powered at 3.3 V, to uniform the design of the readout circuit at the floating gate device, which requires a specific thin-oxide thickness proper of the 3.3 V transistors.

Figure 2 shows the basic blocks of the Sigma-Delta modulator:

- a VCO, which is composed of an integrator — here named Sloper — and a comparator. The Sloper creates a ramp, starting from the sensor's output value, up to an external reference voltage, here set at 2 V. When the Sloper reaches the reference level the Comparator triggers a reset signal for the Sloper that restarts, again integrating from the sensor's signal level. Hence, the VCO frequency depends on the sensor, and this information - frequency — is transmitted;

- a Toggle circuit which reads out the output saw-tooth signal of the comparator and generates a more stable square waveform with a frequency range of the order of hundreds of kHz;

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- an Enable_Transmitter circuit which creates a 100 ns wide monostable signal to enable the Ring_Oscillator(s);

- two Ring_Oscillators that oscillate respectively at 400 and 460 MHz, when enabled. Only one block is the reference oscillator that drives the Transmitter for the antenna coupling. The two oscillators have an equivalent schematic but two different layouts. The first one — reference — has more balanced internal interconnections while the second block is more compact despite using two internal interconnection metal layers. As the ring oscillators are critical and crucial blocks for the entire design, we wanted to investigate and test different solutions;

- a 400 MHz Transmitter to drive a load composed of a 10 pF capacitor and a 50 ohm resistor in parallel.

Circuit simulations show a voltage swing of about 2 V when the block is powered at 3.3 V, thus we expect it can drive a real antenna, whatever it is placed, inside or outside the chip. Figure 3 shows a simulation of the Sigma-Delta circuit composed of two main plots where the bottom one is just a time zoom of the top plot. The waves (A) and (G) on the two plots show the signal on the antenna, being simulated as a static load. It is evident that the amplitude of the transmitted signal is reduced to 1.5 V. The waveforms (B) and (H) represent the enable signal from the Enable_Transmitter circuit that allows the UWB transmission. The third couple of waveforms (C) and (I) show the outputs of the Toggle circuit, i.e. a squared wave of the VCO. The waveforms (D) and (J) show the output of the Comparator circuit, which resets the Sloper. Eventually, the Sloper's output is visible in the waveforms (E) and (K): this is the saw-tooth integrator output. In addition, the total current is shown in the bottom waves (F) and (L) confirming that, after being averaged, the total consumption of the circuit might fit low-power wireless applications. In fact, the current oscillates from 0 to 30 mA for only a very short fraction of the time. Hence, depending of the repetition time of the pulses, the average current might be easily below 1 mA and, by considering a voltage supply of 3.3V, this leads to a rough estimation of some hundreds of uW as average power consumption.

Figure 4 shows the entire layout of the second version of the chip with a visible antenna — yellow ring connected to two pads on the right — outside the pad area. Eight different combinations of antennas and sensor geometries have been submitted in a 2.5 by 5 mm^2 silicon area: right side of the figure.

4 The expected sensitivity

Figure 5 shows, on the left side, a plot of preliminary tests that have already been done using the first prototype of the readout circuit. It is apparent that in the input range (VIN Sloper input in figure 1) from 0 to 2 V the VCO circuit varies the output frequency quite linearly. The right side of the figure shows the spread of the Toggle frequency while keeping VIN stable. In particular the two distributions for VIN = 0 V and VIN = 2 V are centered on different values of frequency, confirming that the output frequency depends on the VIN level. The VCO and the Toggle circuits produce a square wave with a frequency that decreases as the VIN increases. In addition, the

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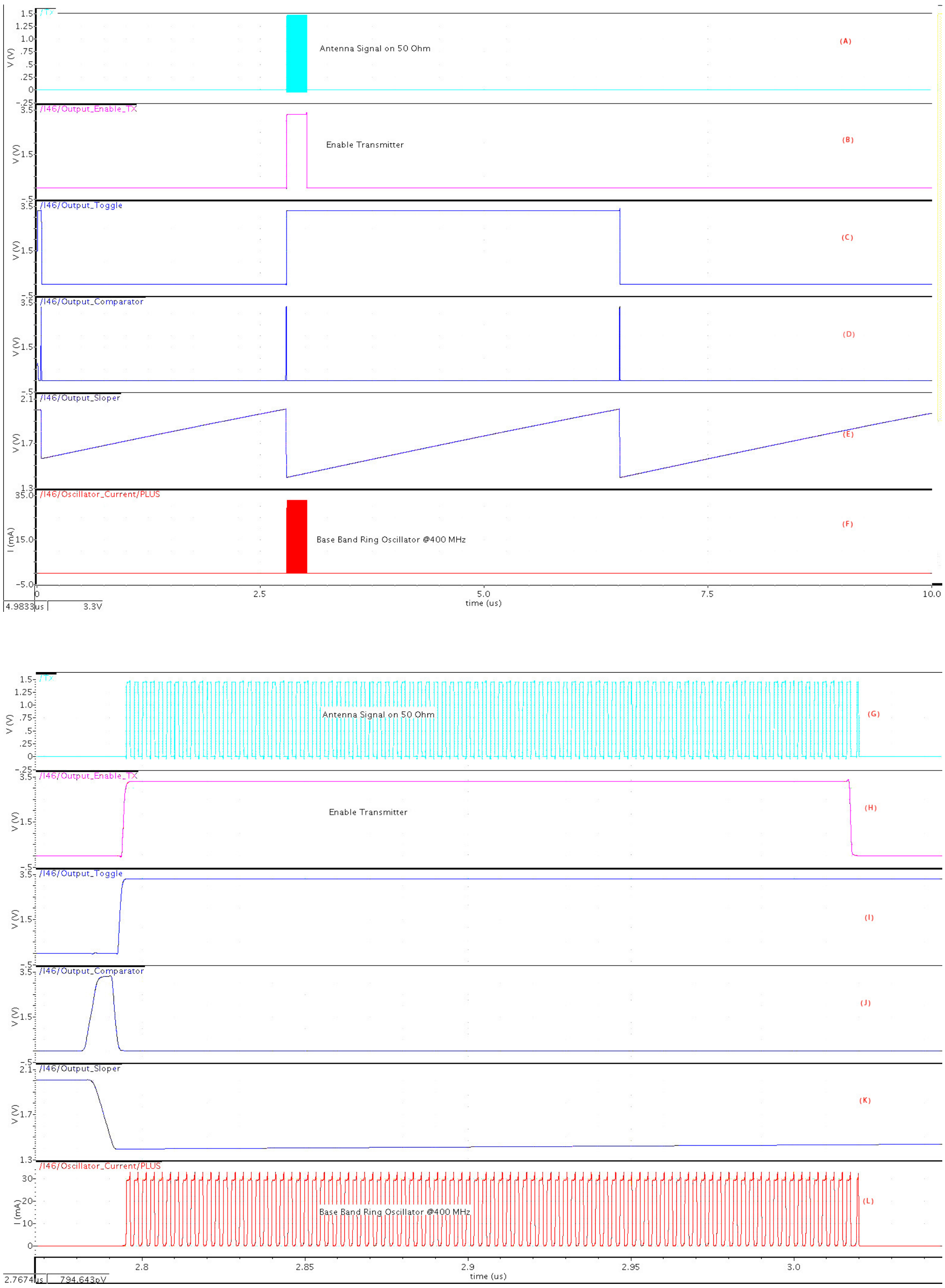

Figure 3. Waves of the Sigma-Delta circuit. Bottom plot is a zoom of the top one.

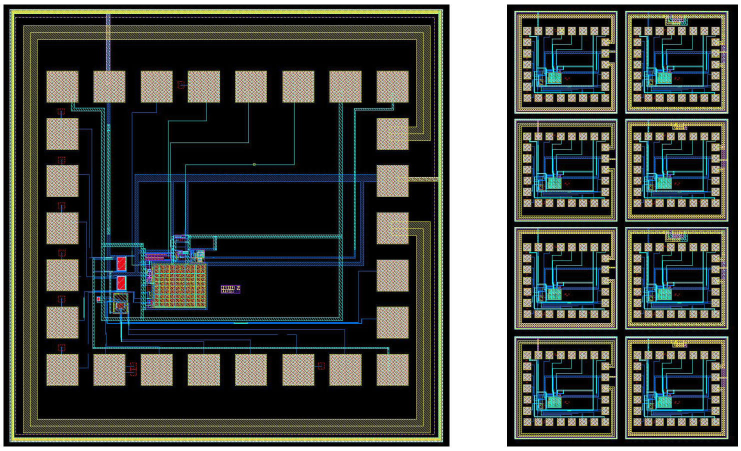

Figure 4. Layout of the full prototype with an integrated antenna visible as a yellow ring outside the pad area, in the left side of the figure. 8 different combinations of antenna and sensor geometry have been submitted altogether in a 2.5 by 5 mm^2 silicon area: right side of the figure.

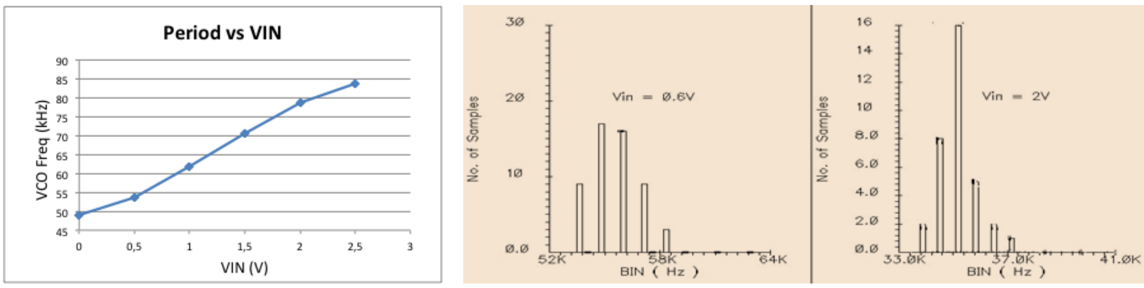

Figure 5. Spread of the VCO output frequency. Left plot shows how the VCO frequency varies depending on the VIN at the modulator input, and it is a measure carried out on the first prototype of the chip. Right side shows two histograms on the distribution on the frequency, at a constant VIN, due to process variation and temperature.

Gaussian distribution appears as the VCO output frequency moves due to the noise. Thus, only the average value of these distributions is of interest and hence a receiver circuit — here not considered — will be required to average the receiver data and to filter out the noise. Tests on the entire circuit connected to antennas are still ongoing since a fine tune of the parasitic components must be performed to enhance the transmission.

Preliminary results confirm the feasibility process of an integrated antenna but these are not complete to draw conclusions.

5 Conclusion

The complete compatibility of this standard CMOS process suggests the use of this technology for monolithic implementations of radiation sensors and microelectronic readout. Also, the integrated antenna exploits wireless communications. A natural application for this work is in the field of in-vivo biomedical treatments, even if spot monitors in High Energy Physics Experiments [13] might be a niche challenge for future particle colliders [14–16].

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A reasonable estimation of the sensitivity of the device is that over a 2 V of input swing the frequency of the VCO varies of about 20 kHz. Then, as previous works of this collaboration [8–12] have shown, the floating gate devices shift the threshold voltage of about 1 mV as a consequence of an absorbed dose of about 0.5–1 rad.

We expect an overall absorption dose of 1 krad matching the 2 V variation of the input voltage. We have also proved that the floating gate sensor device can be reprogrammed and reused several times so that it can stand an integrated absorbed dose of 10 krad.

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