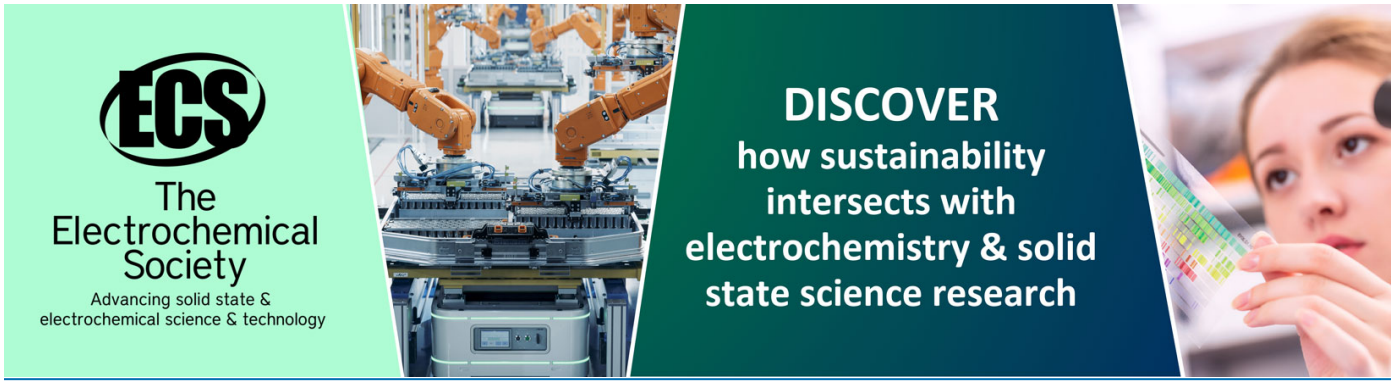
Radiation tolerance of readout electronics for Belle II



PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *November 14, 2011*
REVISED: *December 27, 2011*
ACCEPTED: *January 24, 2012*
PUBLISHED: *February 9, 2012*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2011,
26–30 SEPTEMBER 2011,
VIENNA, AUSTRIA

Radiation tolerance of readout electronics for Belle II

T. Higuchi,[a,1] **M. Nakao**[a] **and E. Nakano**[b]

[a]*High Energy Accelerator Research Organization (KEK),*
1-1 Oho, Tsukuba, Ibaraki 305-0801 Japan
[b]*Osaka City University,*
3-3-138 Sugimoto, Sumiyoshi-ward, Osaka-city, Osaka 558-8585 Japan

E-mail: higuchit@post.kek.jp

ABSTRACT: We plan to start the Belle II experiment in 2015 and to continue data taking for more than ten years. Because some of the front-end electronics cards of Belle II are located inside the detector, radiation effects onto their components will be a severe problem. Using experimental exposure facilities of neutrons and γ rays, we study the radiation effects from these particles to the Virtex-5 FPGA, optical transceivers, and voltage regulators. The Virtex-5 FPGA is found to keep its operation after irradiation of more than 20-year-equivalent neutron flux of Belle II and 88-year-equivalent γ-ray dose. We observe single event upsets (SEUs) and multiple bit upsets (MBUs) in the Virtex-5 FPGA in the neutron irradiation. We also find almost doubled SEU counts in the Virtex-5 FPGA bombarded from its tail side than its head side. We extrapolate the observed SEU and MBU counts in the Virtex-5 FPGA to the entire readout system of the Belle II central drift chamber, and expect the SEU and MBU rates as one SEU per four minutes and one MBU per 11.5 hours, respectively. The optical transceivers are found to keep its operation after integration of 12-year-equivalent neutron flux, while they are killed by about 3-year-equivalent γ-ray dose, which should be solved in the future research. The voltage regulators are found to keep its operation for more than 10-year-equivalent γ-ray dose.

KEYWORDS: Radiation-hard electronics; Front-end electronics for detector readout

[1]Corresponding author.

doi:10.1088/1748-0221/7/02/C02022

Contents

2012 JINST 7 C02022

1 Introduction

Despite the tremendous success in describing the basic forces of nature, many fundamental questions still remain unanswered within the Standard Model (SM). In order to search for an answer to the questions, which is presumably new physics beyond the SM, we start the SuperKEKB/Belle II experiment [1] in KEK, Japan, which is an upgraded B-factory experiment from KEKB/Belle [2, 3]. We plan to start the Belle II experiment in 2015 and to continue data taking for more than ten years. The Belle II detector will be a large-solid-angle magnetic spectrometer consisting of inner vertex detectors with pixels (PXD) and silicon strips (SVD), a central drift chamber (CDC), a barrel-like arrangement of time-of-propagation counters (TOP), an array of ring-image Cherenkov counters (ARICH), an electromagnetic calorimeter (ECL), and a K_L^0-and-muon detector (KLM).

Belle II detector signals are digitized in the front-end electronics card inside (CDC, TOP, and ARICH) or nearby (SVD, ECL, and KLM) the detector. The digitized signals, except for the PXD, are collected by FPGAs on the front-end electronics cards, and are transmitted over unified data transmission scheme from the detector to front-end instrumentation entity for sub-detector specific electronics (FINESSE) cards mounted on common pipeline platform for electronics readout (COPPER) modules [4], which are located $\sim$ 10 m away from the detector.

As the front-end electronics of the CDC, TOP, and ARICH are located inside the detector, radiation effects onto their components will be a severe problem. By extrapolating neutron and γ-ray background measured at the Belle detector to the SuperKEKB luminosity and beam currents, we expect annual neutron flux and γ-ray dose from the beam background at the Belle II detector to be $\sim 10^{11}/\mathrm{cm}^2$ and $\sim$ 100 Gy, respectively, at the full accelerator performance. Background estimation by a preliminary Monte Carlo simulation is consistent to this expectation within a small

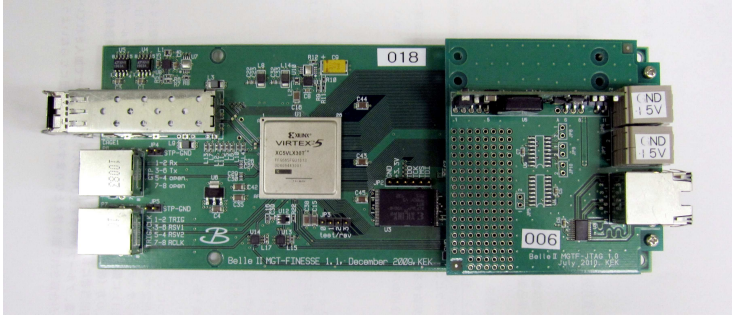


Figure 1. The snapshot of the front-end electronics card (MGTF) for the radiation studies.

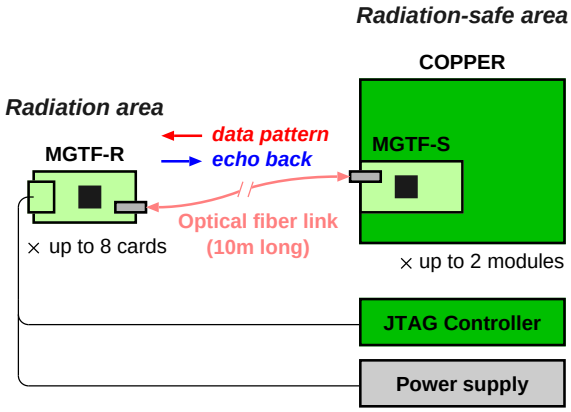


Figure 2. The connection layout of the experimental components for the radiation-effect study.

factor. In order to investigate the radiation effect to the front-end card components especially for the FPGA and optical transceiver, we bombard multi-gigabit transceiver FINESSE (MGTF) cards, which are equipped with a Virtex-5 FPGA and an optical transceiver as well as the actual front-end electronics, with neutrons and γ-rays using experimental exposure facilities.

In the following sections, we give a description about the experimental setup of the radiation-effect study in section 2, then, we report results of neutron- and γ-ray-irradiation studies in section 3 and section 4, respectively, and finally we summarize our report in section 5.

2 Experimental setup

In this section, we give description about the MGTF card for the radiation-effect study, connection layout of experimental components, data path, and damage detection, all of which are common for both neutron- and γ-ray-irradiation studies.

2.1 MGTF card

Figure 1 shows a snapshot of the MGTF card. The card dimension is 186 mm$\times$76 mm. The card equips a Virtex-5 FPGA (XC5VLX30T) at its central region and an SFP optical transceiver slot

2012 JINST 7 C02022

at its left edge in the figure. We use AVAGO optical transceiver (AFBR-57R5APZ) or FINISAR optical transceiver (FTLF8524P2BNV) for the radiation-effect studies. A mezzanine structure of the right part in the figure of the MGTF card equips a transceiver and a RJ-45 connector for JTAG signals translated into LVDS, and a DC-DC converter and terminals for power supply.

2.2 Experimental layout

Figure 2 shows a connection layout of experimental components for the radiation-effect study. We locate two identical MGTF cards: one in the radiation area (MGTF-R card), and the other on the COPPER module in the radiation-safe area (MGTF-S card). The two MGTF cards are linked with each other by a 10-meter-long optical fiber. The MGTF-R card is powered by an external power supply. The Virtex-5 FPGA on the MGTF-R card can be controlled from a JTAG controller device through the JTAG cables to download a firmware. The power supply and JTAG controller devices are located in the radiation-safe area.

2.3 Data flow and damage detection

At the cold start (or after the reset) of the MGTF-R card, the firmware is downloaded from the JTAG controller device. After initialization, the MGTF-S card transmits a predefined 144-kB data pattern to the MGTF-R card through the optical fiber over a simple homemade protocol based on RocketIO with 8b10b encoding and clock correction, and the MGTF-R card stores the data pattern in the block memory of the FPGA. Then, the MGTF-R card returns the data pattern back to the MGTF-S card with adding a four-byte FPGA-status record. This returning action is repeated 250 times. Every returned data pattern and status record from the MGTF-R card are examined by the COPPER module to diagnose the radiation effects.

3 Radiation effect by neutrons

The radiation effect by neutrons to the electronics components can be classified into two; one is a permanent damage that cannot be recovered any more, and the other is an instantaneous data error in the FPGA caused by ionizing particles. In the following subsections, we describe experimental results about the permanent damages and data errors by the neutron irradiation.

3.1 Permanent damages

The permanent damages in the FPGA and optical transceivers are quantified by bombarding the MGTF-R cards with neutrons. To see possible damage dependence on the neutron energy, we carried out two experiments with different neutron energies.

The first experiment is carried out using an experimental nuclear reactor of the University of Tokyo, which generates fast neutrons with the neutron energy $E_n \sim 0.3\,\mathrm{MeV}$. The neutron flux is almost independent of the distance from the source because of a collimator in front of the reactor. We stack eight MGTF-R cards and arrange them in such a way that the front side faces the neutron source for four of them, and the rear side faces for the other. Four AVAGO transceivers and four FINISAR transceivers are installed to each SFP slot of the eight MGTF-R cards. We bombard

2012 JINST 7 C02022

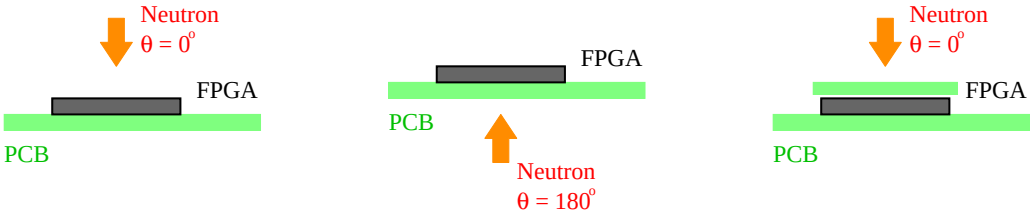


Figure 3. The left and center figures show the cases of neutron incident angle of $\theta = 0^\circ$ and $\theta = 180^\circ$, respectively. The right figure shows the $\theta = 0^\circ$ case with a small PCB piece adhered onto the FPGA.

the stacked MGTF-R cards with $12 \times 10^{11}/\mathrm{cm}^2$ neutrons in total, which corresponds to 12-year-equivalent neutron flux. After the irradiation, we find no permanent damage in the Virtex-5 FPGAs nor optical transceivers.[1]

The second experiment is carried out using a tandem electrostatic accelerator of the University of Kobe. A collision of an accelerated deuteron to 3 MeV with ^{9}Be target generates a neutron with the energy Q value of 4.36 MeV by the reaction of $^9\mathrm{Be} + d \rightarrow {}^{10}\mathrm{B} + n$. We bombard the same arrangement of the MGTF-R cards with the same optical transceivers as we use in the first experiment. The total neutron flux to the Virtex-5 FPGA and optical transceiver on the MGTF-R card depends on a distance from the target and an azimuthal angle from the beam. Using an absolute neutron flux measured by a dose meter located behind the experimental setup, we estimate the Virtex-5 FPGA and optical transceiver receive up to 4.8-year- and 2.3-year-equivalent neutron flux, respectively. After the irradiation, we find no permanent damage in the Virtex-5 FPGAs nor optical transceivers, as well.

3.2 Data errors

In the permanent-damage experiments, we find a number of data errors in the FPGA: single event upsets (SEUs) or multiple bit upsets (MBUs). In addition, we find asymmetric SEU counts between the cases with neutron incident angle $\theta = 0^\circ$ and $\theta = 180^\circ$, which we name a "head-tail asymmetry". To investigate the data-error rate and head-tail asymmetry, we carried out systematic experiment on the data errors using the experimental nuclear reactor.

We classify the data errors into two: errors in the configuration data region and those in the block RAM region. The errors in the configuration data region are quantified by the total number of automatically cured SEUs by the SEU recovery macro described in Xilinx XAPP864 [5] through the operational time of the FPGA. Self-unrecoverable errors (UREs) including the MBUs in the configuration data region, which requires a firmware download to reset, are also taken into account to the errors in the configuration data region. The errors in the block RAM region are quantified by counting a number of mutations in the returned 144-kB data pattern examined by the COPPER module. A single-bit mutation in the pattern is regarded as the SEU, and multiple-bit mutations are regarded as the MBU.

[1] Slight damages in the optical transceivers are found right after the irradiation program. The FINISAR transceivers loses light output and AVAGO transceivers get unstable in the data transfer. All of them get recovered after power cycling.

2012 JINST 7 C02022

Table 1. List of the total count of the data errors in the configuration data region and block RAM region of the Virtex-5 FPGA together the error rate as a function of the neutron incident angle. Numbers in parenthesis in the URE column corresponds to the URE identified as the MBU.

Incident angle	Configuration data region				
	Total time [min]	#SEU	SEU rate [/min]	#URE	URE rate [/hour]
$\theta = 0^\circ$	138	540	3.90	4 (1)	1.73 (0.43)
$\theta = 90^\circ$	108	583	5.40	11 (7)	6.11 (3.89)
$\theta = 180^\circ$	135	1276	9.49	6 (2)	2.68 (0.89)
Incident angle	Block RAM region				
	Total time [min]	#SEU	SEU rate [/min]	#MBU	MBU rate [/hour]
$\theta = 0^\circ$	130	177	1.36	10	4.60
$\theta = 90^\circ$	110	158	1.43	12	6.54
$\theta = 180^\circ$	115	195	1.70	25	13.06

The head-tail asymmetry is studied with varying the neutron incident angle to the MGTF-R cards to one of 0° (head), 90° (side), and 180° (tail). A possible FPGA dependence in the SEU and URE counts is averaged out by summing up SEU and URE counts of six different MGTF-R cards. We disassemble the eight-stacked MGTF-R cards used in the permanent-damage experiments, and using six cards out of the eight we reassemble three pairs of the cards. We bombard every pair with neutrons for up to 20-30 minutes for each incident angle variation, where the 30-minute irradiation corresponds to 3.3-year-equivalent neutron flux.

Table 1 lists the total count of the data errors in the configuration data region and block RAM region of the Virtex-5 FPGA together with the error rate as a function of the neutron incident angle. Numbers in parenthesis in the URE column corresponds to the URE identified as the MBU. The total time in the table corresponds to a sum of the net operational time of the FPGAs. From the table, we calculate the head-tail asymmetry of the configuration data region and block RAM region of the Virtex-5 FPGA defined by $R \equiv [\text{SEU-rate}]_{180^\circ}/[\text{SEU-rate}]_{0^\circ}$ as $R^{\text{V5,config}} = 2.43 \pm 0.07$ and $R^{\text{V5,RAM}} = 1.25 \pm 0.09$, respectively. The averaged head-tail asymmetry over the two regions is $R^{\text{V5}} = 2.13 \pm 0.06$, by which we conclude that the neutron irradiation to the Virtex-5 FPGA with $\theta = 180^\circ$ causes ~ 2 times more SEUs than $\theta = 0^\circ$. To estimate a possible effect from the printed circuit board (PCB) to the head-tail asymmetry, we adhere a small PCB piece with a soldering pattern to the FPGA head side and count the number of SEUs in the 30-minute neutron irradiation from the FPGA head (figure 3 (right)). The observed SEU rates of the configuration data region and block RAM region are 3.88/min and 1.40/min, respectively, which are similar to those of the $\theta = 0^\circ$ case without the PCB. We conclude that the PCB has only negligible effect to the SEU rate and the origin of the head-tail asymmetry is expected inside the FPGA itself.

We estimate the SEU rate for the entire Belle II CDC front-end electronics using the observed SEU counts. Our observation of 5.26 SEUs per minute per one Virtex-5 XC5VLX30T FPGA in the $\theta = 0^\circ$ case corresponds to 473 SEUs per 10-year-equivalent neutron irradiation per FPGA. In the Belle II CDC, we use 302 Virtex-5 XC5VLX155T FPGAs, which is equivalent to 1560 Virtex-5

2012 JINST 7 C02022

XC5VLX30T FPGAs considering the logic size. Then, we expect one SEU per ~ 4 minutes for the entire Belle II CDC front-end electronics. Here, we assume we annually take data for 200 days in total. Using the similar discussion, we estimate the URE rate of the Belle II CDC as one URE per ~ 11.5 hours. We note that this is for the case with uniform neutron flux, while in the real configuration, the neutron flux becomes lower toward the outer radius.

As well as the permanent-damage experiments, we find no permanent damage in the FPGAs after this experiment. In this experiment, the most irradiated FPGA receive yet another 10-year-equivalent neutron flux. We conclude that the Virtex-5 FPGA is tolerant to more than the 20-year-equivalent neutron flux.

We also investigate the head-tail asymmetry of the Spartan-6 FPGA. Because of regulation in the experimental setup, we only measure the head-tail asymmetry of the SEU rate in the configuration data region. The observed head-tail asymmetry is flipped from the Virtex-5 as $[R^{\mathrm{S6,config}}]^{-1} = 1.37 \pm 0.30$. The possible reason of the flip is the diode orientation in the FPGA; the Virtex-5 is a flip-chip FPGA and the Spartan-6 is a wire-bonded FPGA. We also find the SEU rate of the Spartan-6 FPGA in the $\theta = 180^\circ$ case is 1.7 times higher than that of the Virtex-5 FPGA in the $\theta = 0^\circ$ case.

4 Radiation effect by γ rays

The radiation effect of the γ rays are studied using γ-ray exposure facility of Tokyo Institute of Technology, which provides 1.17 MeV and 1.33 MeV γ rays from a ^{60}Co source. We bombard Virtex-5 FPGAs, optical transceivers, and voltage regulators on the MGTF-R cards with appropriately shielding of other parts by lead bricks.

We find no data error in the FPGA at all after the exposure of at most 88-year-equivalent γ rays. The other Virtex-5 FPGA bombarded with 73-year-equivalent γ rays also shows no data error. We observe SEU neither.

In contrast to the FPGA, the optical transceivers we tested are found to be very sensitive to γ rays. We bombard two AFBR-57R5APZ and two FTLF8524P2BNV, and find all of them are killed by around 3-year-equivalent γ-ray dose. The killed transceivers neither emit nor receive the IR light any more. They also make no response to communication via the I^2C bus. We are searching for a radiation-tolerant optical transceiver in the market to avoid this problem, and are planning further radiation-effect studies on candidate transceivers.

The voltage regulators, which are expected γ-ray sensitive, are found to survive at least 10-year-equivalent (planned Belle II operation period) dose. We bombard Linear Technology LTC3026, LT1963, and LT1761 regulators. Even the weakest regulator, the LT1761, is found still operating until 26-year-equivalent dose.

5 Summary

We study radiation effect of neutrons and γ rays to the Virtex-5 FPGA, optical transceivers, and voltage regulators, which will be used in the front-end detector readout cards of Belle II. The Virtex-5 FPGA is found to keep its operation after irradiation of more than 20-year-equivalent neutron flux and 88-year-equivalent γ-ray dose. We observe SEUs and MBUs in the Virtex-5

2012 JINST 7 C02022

FPGA in the neutron irradiation, which are extrapolated to the entire Belle II CDC readout system as one SEU per six minutes and one MBU per two days, respectively. The optical transceivers are found killed by about 3-year-equivalent γ-ray dose, which should be solved in the future research. The voltage regulators are found to keep its operation for more than 10-year-equivalent γ-ray dose.

Acknowledgments

We acknowledge Prof. Kitamura, Dr. Ochi, and Mr. Miyazaki (the University of Kobe); Mr. Nakagawa (the University of Tokyo); and Prof. Kuze and Mr. Yoda (Tokyo Institute of Technology) for their excellent managements and operations of the tandem accelerator, experimental nuclear reactor, and γ-ray exposure facility, respectively. This work is partially supported by JSPS Grant-in-Aid for Young Scientists (B) (Grant Number 23740220).

References

[1] sBELLE DESIGN GROUP collaboration, I. Adachi et al., *sBelle Design Study Report*, arXiv:0810.4084.

[2] S. Kurokawa and E. Kikutani, *Overview of the KEKB accelerators*, *Nucl. Instrum. Meth.* **A 499** (2003) 1.

[3] A. Abashian et al., *The Belle Detector*, *Nucl. Instrum. Meth.* **A 479** (2002) 117.

[4] M. Nakao, T. Higuchi, R. Itoh and S. Y. Suzuki, *Data acquisition system for Belle II*, 2010 *JINST* **5** C12004.

[5] Xilinx, *SEU strategies for Virtex-5 devices*, *XAPP864* (2001).

2012 JINST 7 C02022