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The data acquisition card for the Large Pixel Detector at the European-XFEL

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ABSTRACT: The Front End Module (FEM) is a custom on-detector FPGA based digital data acquisition card for the Large Pixel Detector (LPD) currently under construction for the European X-ray Free Electron Laser (Eu-XFEL) facility in Hamburg. The data acquisition systems at the Eu-XFEL facility will have to cope with beam timing and data rates comparable to those in particle physics experiments and employs similar components and techniques. The prototype Large Pixel Detector under construction at the STFC Rutherford Appleton Laboratory contains one Megapixel sensor elements and is constructed out of 16 identical supermodules. A FEM card is mounted on the rear of each supermodule and provides readout and control functions. Each FEM is linked to the central data acquisition by a 10 Gbps optical fibre data link running 10Gb UDP/IP protocols. In normal operation the LPD detector will generate 10 GBytes/sec of processed data for every one Megapixel of sensor area. This paper describes the design of the FEM and experience with the first prototype cards.

KEYWORDS: Data acquisition circuits; Front-end electronics for detector readout

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Contents

1 Introduction

The prototype Large Pixel Detector [1] under construction at the STFC Rutherford Appleton Laboratory for the European-XFEL (Eu-XFEL) in Hamburg [2] contains one Megapixel of sensor elements. The detector is constructed out of 16 identical supermodules. A custom Front End Module (FEM), mounted on the rear of each supermodule, provides readout and control functions. The Eu-XFEL machine timing is such that every 100 milliseconds a train of up to 2,700 X-ray pulses will be produced with an inter-pulse separation of 220 nanoseconds. This leaves more than 99 ms when there is no signal and this is used for readout of the front-end systems. Not all 2,700 pulse locations will be populated with photons on each of the experimental areas. LPD is constructed to selectively readout up to 512 pulses.

The LPD data acquisition, and its interfaces to the common Eu-XFEL DAQ system, is shown in figure 1. The FEM card is mounted on the rear of each supermodule and is linked to the central data acquisition (Train Builder) system [3] by a 10 Gbps fibre optic link using 10GbE UDP/IP protocols [4]. Each FEM reads out 128 Front End ASICs. In order to cope with the large dynamic signal range at XFEL the ASICs have 3 different gain stages for each pixel. Every FEM receives up to $\sim$ 1,500 MBytes/sec of raw data (corresponding to a maximum of 512 pulses which can be stored in the ASIC pipeline for each train), consisting of the 3 gain values per pixel per pulse. An FPGA based algorithm selects the optimal gain value in each pixel for each pulse which reduces the output to $\sim$ 640 MBytes/sec of processed data.

A total of 16 FEMs are needed to instrument one Megapixel. In final operation the LPD detector will therefore generate a total of 10 GBytes of processed data for each Megapixel of sensors (table 1). The Train Builder system is housed in Advanced Telecoms ATCA industry standard crates and will assemble the partial images from a number of FEMs and for complete pulse trains. The resultant full data sets are fed on to a farm of PCs for final data analysis.

Each FEM is also connected to the common Eu-XFEL Clock and Control (C&C) systems [5] by dedicated fast electrical links which provide fast timing and pulse selection information. An electrical GbE connection allows the run control systems to configure and monitor the detector using TCP/IP protocols. The C&C system is implemented in a MicroTCA industry standard crate.

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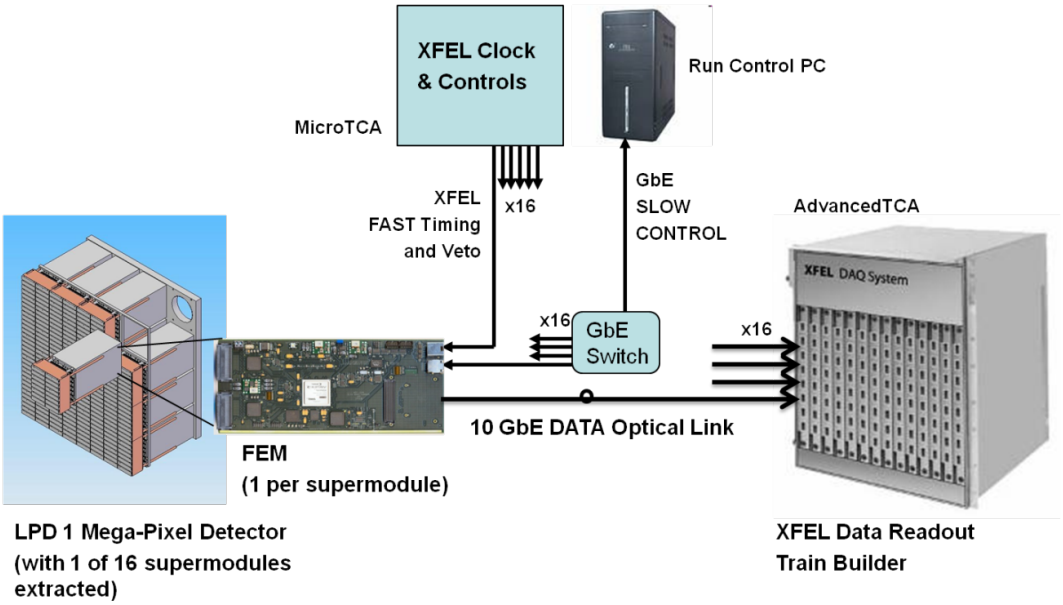

Figure 1. LPD Data Acquisition and Eu-XFEL System Interfaces.

Table 1. LPD data rates.

Nr ASICs per FEM	128	
Nr Pixels per ASIC	512	
Nr Samples per Pulse train	512	
Nr Pulse trains per second	10	
Max Raw Data Input to each FEM	$\sim 1,500$	MBytes/sec
Max Processed Data Output from each FEM	~ 640	MBytes/sec
Number of FEMs per 1 MPixel Detector	16	
Total Processed Data output per 1 MPixel Detector (from 16 FEMs)	10	GBytes/sec

The Train Builder and C&C systems will be used by all the 2D pixel detectors at Eu-XFEL. Each FEM has its own links to the DAQ, timing and experimental controls systems and can operate independently. The LPD DAQ system has also been designed to operate in standalone mode for local tests and situations when the common DAQ systems are not available.

2 Front-End Module (FEM) components

Side 1 of the FEM is shown in figure 2. At the rear of each card is a pair of dense (240 way) high performance connectors which carry the clock, fast and slow control and data readout signals for the 128 ASICs which instrument each supermodule. The FEM plugs into a custom backplane at the rear of each supermodule which also provides power to the FEM. Fast signals are distributed on LVDS transmission lines to the ASICs via feedthrough modules on the rear of the backplane.

A pair of Xilinx Spartan3 FPGAs (3S400AN) is used to distribute the large number of I/O signals to the ASICs. A large Xilinx Virtex5 FPGA (FX100T) provides the main control and

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Figure 2. FEM side 1.

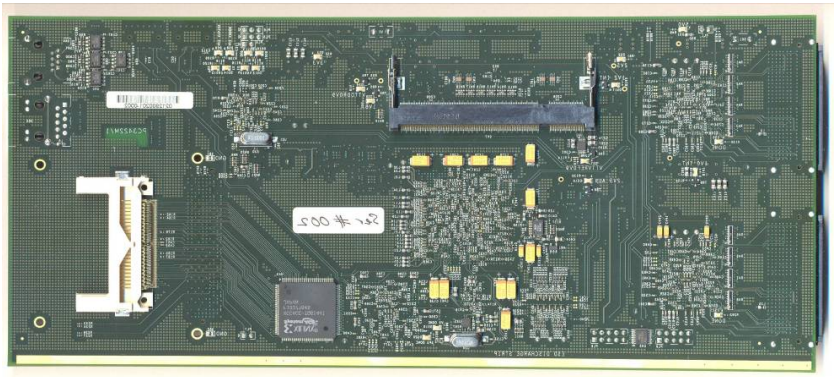

Figure 3. FEM side 2.

data processing engine for the FEM. The Virtex5 contains dual PowerPC440 embedded processor cores. One of these is used to manage the DDR2 memory controller DMA engines and the other runs a lightweight TCP/IP stack to communicate with the run control system. External SRAM and FLASH devices provide storage for the software OS running on the embedded processors in the Virtex5. A third Spartan3 FPGA (with embedded Flash memory) is used as a configuration controller and boot device.

At the front of the card is an ANSI/VITA57 standard high density FMC connector, which houses a dual 10 Gbps SFP+ optical data link FMC mezzanine card developed by DESY for the Train Builder DAQ system [6]. Only one of the SFP+ pair is populated on the FEM side of the link. The FMC is interfaced to the Virtex5 by 8 Multi-Gigabit transceiver lanes (4 lanes per link). The FMC is also connected to the Virtex5 by multiple fast LVDS channels allowing Camera Link compatible FMCs with copper links to be used for other applications.

An external PHY connects the Virtex5 to an electrical GbE link which interfaces with the run control system. A second RJ45 connector links the FEM by a standard CAT5 cable to the C&C distribution card (housed in a local MicroTCA crate) which provides the FEM with the XFEL master clock @ 99MHz, encoded machine timing signals and fast pulse synchronous veto information.

Side 2 of the FEM (figure 3) houses a socket for a DDR2 SODIMM connected to the V5 FPGA. This memory can provide up to 2 GBytes of fast data buffer storage. There is also a System ACE controller and associated Compact Flash card to provide configuration storage for the FPGA bit files and embedded software code. The PCB is 2mm thick and contains 16 layers of which 8 are signal layers.

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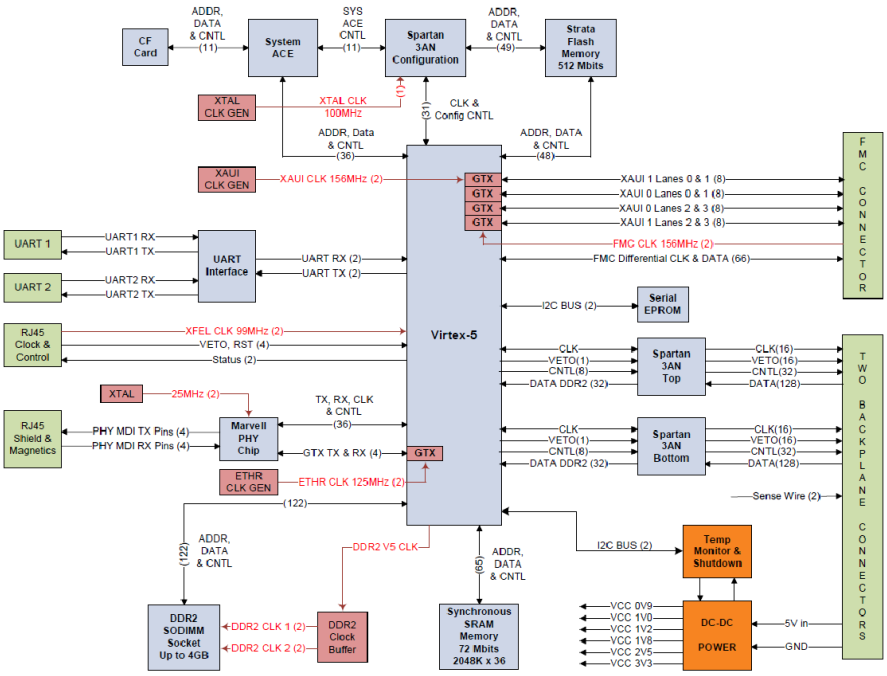

Figure 4. FEM architecture.

3 Front-End Module operation and FPGA firmware

Figure 4 shows the architecture of the FEM card. The interface logic to the 128 ASICs is contained in the Virtex5 FPGA. In normal operation the FEM continuously delivers the 99 MHz clock from the C&C system to the ASICs. On receipt of a timing command from the C&C indicating the start of a train of X-ray pulses, the FEM broadcasts a series of fast commands to all ASICs to prepare them for capturing data from the train. During the train the FEM receives and distributes fast veto signals at the 4.5 MHz X-ray pulse rate which instructs the ASICs which of up to 512 of the 2,700 pulses should be stored in the ASIC analogue memory pipelines. Following the train the FEM issues a readout sequence to the ASICs and data is streamed in parallel from all 128 ASICs to the FEM during the 99 msec inter-train interval. The cycle then repeats at the 10 Hz machine rate.

There are 512 pixel channels in each ASIC. Each channel is instrumented with an integrating preamplifier which copes with 1 to 100k photons per pixel per X-ray pulse. The preamplifiers are followed by 3 different gain stages to cope with the large signal dynamic range. The analogue outputs are stored on capacitors at the 220 nanosecond pulse rate. The long inter-train spacing is then used to convert the data at 12 bits using 16 on chip ADCs working at 8 Megasamples per second each.

The 128 ASIC data outputs are passed through the Spartan3 I/O devices to the main Virtex5 FPGA. In order to reduce the data volume, the Virtex5 implements an algorithm (in VHDL) to select the optimal signal to noise sample from the 3 gain settings from each pixel for each pulse. Only the optimal values are output to the 10G link. Up to this stage the entire LPD DAQ system is synchronous with the master clock on all channels.

Within the Virtex5 the processed data is transmitted on a Xilinx LocalLink standard interface

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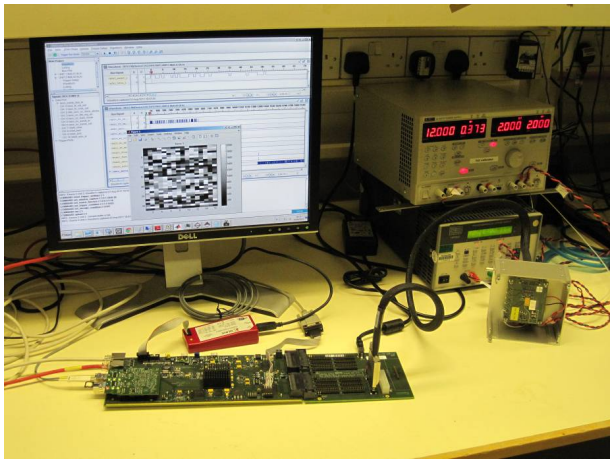

Figure 5. Test stand with FEM (equipped with 10 Gb link card) and ASIC test module.

to the Virtex5 PPC memory interface module where it is buffered in external DDR2 memory under DMA engine control. By programming the DMA engines appropriately the data images may be reordered in memory into proper pulse arrival time order to correct for the disordering introduced by the operation of the ASIC veto pipeline logic.

The data from the DDR2 is then transmitted by DMA via LocalLink to a 10Gb UDP/IP VHDL module which is based on the standard Xilinx XAUI core. This module interfaces to the 10G FMC data link card using the Virtex5 Multi-Gigabit Transceivers. The data is transmitted to the central Train Builder system where it is merged with the data from the other LPD FEMs to create movies of the images from the train for the entire detector.

Prior to data taking, the FEM programs the ASICs with the necessary constants e.g. bias settings provided by the experimental controls. Final data processing is foreseen to be carried out on a farm of commodity PCs running floating point based image processing algorithms with access to full calibration constants. The processed data sets will then be stored on the Eu-XFEL archival infrastructure [7].

4 Status and testing

Four prototype FEM cards were manufactured in Q1/2011. They all passed JTAG boundary scan tests without error. Standalone bench tests show that the cards are performing to their specifications. For example benchmark measurements with the Virtex5 PPC memory controller interface gave a data rate of over 900 MBytes/sec compared with the 640 MBytes/sec required. Initial tests of the 10Gb UDP/IP interface have achieved over 1,000 MBytes/sec. The FEMs are now being used to develop FPGA firmware and to evaluate the performance of the LPD detector modules.

Figure 5 shows a FEM connected to a test box containing a single ASIC. An extender card (used for JTAG testing) plugs on to the FEM backplane connectors and links by cable to the ASIC module. The FEM sends pre-programmed sequences of ASIC fast commands and vetoes. The FEM is also equipped with a DESY 10Gb optical FMC mezzanine card for data readout which is

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linked to a standard 10Gb network card in a PC. The 10Gb UDP/IP VHDL firmware block is used to transmit ASIC data. A captured ASIC image can be seen on the screen.

A separate card (not shown) is used to emulate the C&C system and is connected to the FEM to provide the ASIC clock. A further 20 FEMs are now being manufactured in preparation for testing with larger detector systems.

Acknowledgments

We would like to thank all our colleagues in the LPD collaboration who have developed the sensors, ASICs, PCBs, mechanics and cooling and the software for the detector. We also thank in particular Manfred Zimmer and Igor Sheviakov (DESY) for developing the 10Gb optical FMC card and Chris Youngman (Eu-XFEL) for coordinating the Eu-XFEL DAQ project. We would also like to thank Eu-XFEL GmbH for continued financial support of the LPD project.

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