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A high frame rate, 16 million pixels, radiation hard CMOS sensor

N. Guerrini, a, R. Turchetta, a G. Van Hoften, b R. Henderson, c G. McMullan c and A.R. Faruqi c

a STFC-Rutherford Appleton Laboratory, Harwell Science and Innovation Campus, Didcot, OX11 0QX, Oxfordshire, UK.
b FEI - Achtseweg Noord 5, Bldg 5651 GG Eindhoven, The Netherlands
c MRC Laboratory of Molecular Biology, Hills Road, Cambridge, U.K.

E-mail: nicola.guerrini@stfc.ac.uk

ABSTRACT: CMOS sensors provide the possibility of designing detectors for a large variety of applications with all the benefits and flexibility of the widely used CMOS process. In this paper we describe a novel CMOS sensor designed for transmission electron microscopy. The overall design consists of a large $61 \times 63 \text{ mm}^2$ silicon area containing 16 million pixels arranged in a $4K \times 4K$ array, with radiation hard geometry. All this is combined with a very fast readout, the possibility of region of interest (ROI) readout, pixel binning with consequent frame rate increase and a dynamic range close to 12 bits. The high frame rate has been achieved using 32 parallel analogue outputs each one operating at up to 20 MHz.

Binning of pixels can be controlled externally and the flexibility of the design allows several possibilities, such as $2 \times 2$ or $4 \times 4$ binning. Other binning configurations where the number of rows and the number of columns are not equal, such as $2 \times 1$ or $2 \times 4$, are also possible.

Having control of the CMOS design allowed us to optimise the pixel design, in particular with regard to its radiation hardness, and to make optimum choices in the design of other regions of the final sensor. An early prototype was also designed with a variety of geometries in order to optimise the readout structure and these are presented. The sensor was manufactured in a 0.35 $\mu m$ standard CMOS process.

KEYWORDS: VLSI circuits; Solid state detectors; Radiation-hard detectors

1 Corresponding author.
1 Introduction

For a long time film has been the only possibility as a recording medium for particles direct detection in general and TEM (Transmission Electron Microscopy) in particular. The need for immediate access to the recorded information was addressed indirectly by charge-coupled detectors (CCD) coupled to phosphor-coated fibre optics. This solution achieves a good signal-to-noise ratio at low spatial frequencies but, because of the light scattering in the phosphor and fibre optics, the resolution is degraded at higher spatial frequencies.

CMOS technology is widely used for image sensors at present in many other applications. This is because CMOS sensors offer several advantages when compared to film or CCD sensors [1].

Film and CCDs are currently the two principal choices in transmission electron microscopy. Film has the best spatial resolution but is an analogue recording medium, and requires storage support. Film also needs time for development and suffers from poor S/N when exposure is weak. CCDs must be used in an indirect detection mode because they are susceptible to radiation damage. Since CCDs have a conveniently fast readout and no registration error they can be used for electron tomography but the phosphor coupling limits their spatial resolution.

CMOS sensors provide an alternative to CCDs as a digital detector, because the radiation hardness inherent to CMOS makes them suitable for direct detection of electrons or other charged particles. CMOS should then work in a direct detection mode with good spatial resolution and good single electron sensitivity [2–4].

Several papers have been published on the performance of CMOS sensors in the electron microscope, but all have been prototypes. The production sensor presented in this paper satisfies the full set of requirements for a TEM sensor, which can be summarised as follows:

- 4K by 4K pixel array.
- Readout rate in excess of video rate.
  - High spatial resolution, in terms of Modulation transfer Function (MTF) at Nyquist frequency
  - High Detective Quantum Efficiency (DQE)
  - Full well capacity (∼50 primary electrons).
• Low Noise (<0.05 primary electrons).
• Good radiation resistance. Lifetime of at least $30 \cdot 10^6$ primary electrons per pixel at 300 keV
• Region-Of-Interest (ROI) readout.
• Pixel binning.

Details of the detectors developed by our group are described in the following sections.

2 Sensor architecture

After considering the trade-offs between high spatial resolution and readout rate, and taking charge sharing between pixels into account, the pitch of the sensor was set at $14 \, \mu\text{m}$ [5]. This, combined with the $4K \times 4K$ format, meant the image plane would have a size well above that of a reticle, which is the maximum printable area for the photolithographic process, so “stitching” needs to be used [6].

The reticle is shown figure 1(a) and the fabricated sensor is obtained by stepping and repeating individual blocks until the desired size is achieved, as in figure 1(b).

The sensor architecture is based on a fully analogue readout chain. This decreases power consumption and increases the overall sensor yield. A simplified scheme of the analogue readout chain is shown in figure 2.

The very large silicon area of the sensor posed challenges in terms of signal routing and signal timing. In fact, signals travelling from one end of the sensor to the other will present a significant delay of hundreds of nanoseconds. The goal of a frame rate in excess of video rate can be achieved, however, by implementing a multi-channel parallel readout.

The row and column selection circuits have been optimised and take into account the aforementioned delays to allow overall the fast readout required. Particular attention has been also been paid to the output stages, due to the demanding performance required.
The designed output stage, based on a three stage folded cascoded amplifier, has an input and output dynamic range larger than 2V, a GBW (Gain Band Width) product higher than 190 MHz and a phase margin in excess of 60°.

The routing of biasing currents to blocks placed at very large distances represents another challenge related to the large scale device. In these cases it is best practice to route the actual current rather than voltage [7]. In fact, in the case of very large distances the resistance of the substrate can play an important role in generating differences in the biasing currents due to VGS (gate-source voltage) variations (see figure 3).

Biasing currents have been routed across the sensor as shown in figure 4. By keeping the transistors in each current mirror (indicated by a dotted red line) as close as possible, transistor matching is improved and the biasing variations on the entire chip are reduced.

2.1 Radiation hardness

This sensor is intended for direct detection, so radiation hardness is a key element of the design.

Every block has been designed according to radiation hardness requirements, using enclosed geometry layout (ELT) and substrate contacts.
Radiation creates a positive charge at the silicon-oxide interface. Thin oxide is known to be radiation resistant [8], but at the edge of the transistors, the polysilicon gate runs on thick oxide, creating the well-known “bird’s beak” effect, see figure 5.

In the presence of radiation induced positive charge this transistor can be turned on permanently thus short-circuiting the source and drain of the MOS transistors.

Such a problem can be easily solved by designing transistors with a “never ending gate” of ELT (Enclosed Layout Transistor), as in figure 6 [9].

Tests under electron beam irradiation showed that the fabricated sensor was still operating after being irradiated with 2-300 million electrons per pixel (Me/px).
3 Sensor performance

The analogue readout is based on parallel channels, each channel operating with large voltage swings, to avoid limiting the dynamic range. The resulting output speed allows imaging at video rate (or slightly faster).

The sensor design allows binning of 2 and 4 rows, resulting in possible configurations up to 4x binning. This gives the user a large variety of choices in terms of speed vs. resolution. In fact, the readout speed is increased by a factor proportional to the number of rows binned.

The demanding requirements set in the introduction have been met in designing a sensor with the following characteristics:

- $61 \times 63 \text{ mm}^2$ silicon area
- $4K \times 4K$ array (16 million pixels)
- Analogue output readout
- Frame rate in excess of video rate.
- Radiation hard characteristics.
- Pixel binning and region of interest readout

The sensor presented above is currently used in the FEI Falcon™ Direct Electron Detector [10], whose main performance is summarised below:

- Incident electron voltage up to 300 keV.
- Binning 1x, 2x and 4x.
- DQE 0.3 @ 0.5 Nyquist, 300 keV.
- Readout noise lower than 0.1pe/px (primary electrons per pixel)
- Acquisition time 2.5s per image at binning 1, for a 40 frame summation
- Dynamic range 16 bits
- Radiation hardness of several 100’s of million electrons/px
Finally, some results obtained with the FEI Falcon™ Direct Electron Detector are shown.

In figures 9 and 10 the results (images on the left and FFT on the right) for gold reflections at low dose are presented.

It is clear even to the eye that images taken with the FALCON system are sharper than the ones with a CCD.

Another experiment has been conducted on a real life science specimen, a sample of TMV (Tobacco Mosaic Virus). TMV is a long tube-like protein formed by a helix of proteins with a pitch of 23Å. The images taken with the FALCON provide more high resolution features than the comparable CCD images, shown together in figures 11 and 12. In particular, the FFT of the images show the 11 and 23 Å features more clearly using FALCON in figure 11(b).

4 Conclusions

A large area, 4K by 4K, 14 µm pixel rad-hard sensor was successfully designed in a standard 0.35 µm CMOS process. The sensor performance makes it suitable for use as a direct detector in transmission electron microscopes. It operates at a speed in excess of video rate. This means this sensor outperforms existing large area sensors in terms of pixel rate, see for example [11]. The
sensor is radiation hard and has region of interest (ROI) readout as well as pixel binning and can be adopted in a large range of possible applications.

It is now at the heart of a commercial camera which we hope will revolutionise the TEM field [10].

References


