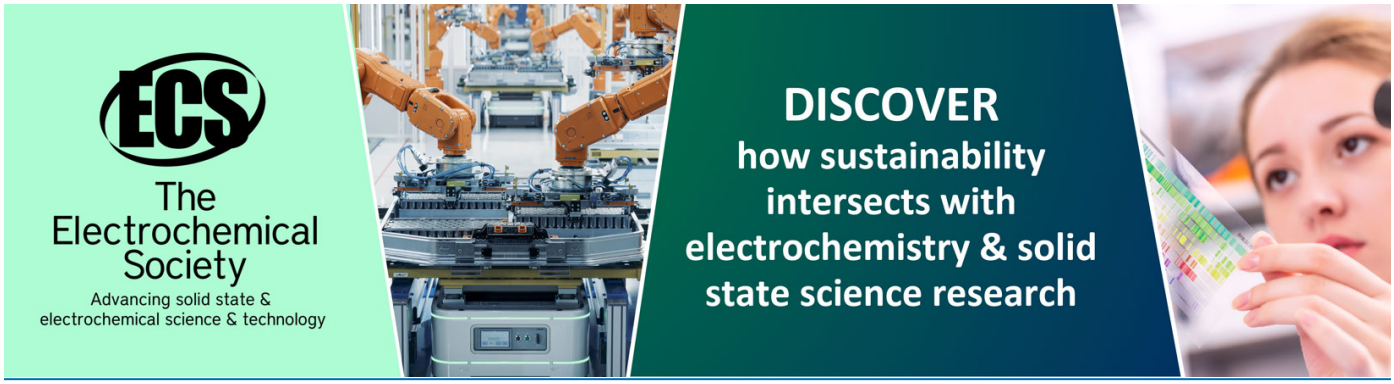
Progress and advances in Serial Powering of silicon modules for the ATLAS Tracker Upgrade



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Progress and advances in Serial Powering of silicon modules for the ATLAS Tracker Upgrade

J. Matheson[1]

STFC Rutherford Appleton Laboratory,
Chilton, Didcot, Oxfordshire OX11 0AE, U.K.

E-mail: John.Matheson@stfc.ac.uk

ABSTRACT: Future detector systems will face technical difficulties with the supply of electrical power to a multitude of sub-detectors. The Serial Powering (SP) scheme is an elegant solution which leads to a great reduction in cable mass, whilst increasing efficiency and reducing cost. In recent years, substantial developments in SP have been made by the ATLAS Tracker Upgrade Community. Initial demonstrator modules and supermodules (known as Staves) used the ABCD chip, with shunt regulators made from discrete components. Continuous development of the SP architecture has led to shunt regulation within the latest ABCN-25 ASICs themselves. From a system point of view, studies of protection schemes and current sources have advanced greatly. We report recent progress, including first results from a serially powered Stavelet using the ABCN-25 chip.

KEYWORDS: Particle tracking detectors; Large detector systems for particle and astroparticle physics; Particle tracking detectors (Solid-state detectors)

[1]On behalf of the ATLAS Tracker Upgrade Serial Powering Collaboration

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1 Introduction

1.1 The ATLAS tracker upgrade

In ATLAS, particles arising from beam collisions are tracked within a magnetic field by the Semiconductor Tracker (SCT). The SCT is instrumented by silicon microstrip modules, with 128-channel readout ASICs (ABCDs). Independent powering is used, with each of the 4088 modules having its own cabling. This cabling occupies significant space and adds mass to the SCT. With the present design, more than 60% of the power supplied to the SCT is lost as heat in the cable resistance, reducing efficiency and increasing the load on the cooling system.

It is planned to increase the luminosity of the LHC, increasing the occupancy in ATLAS. The SCT will be replaced by the ATLAS Tracker Upgrade (ATU), with a factor of 10 increase in channel count. The baseline design for the ATU is the Stave [1], which is based on a rectangular carbon fibre support, with a bus cable on each face. The bus cable takes power to, and signals to and from, the detector modules. Modules are mounted on top of the bus cables. Each module is based on a microstrip detector, 96mm square, with four columns of 1280 strips. Two readout hybrids are glued to each detector, each hybrid carrying two columns of 10 ASICs.

One cable per module for low voltage distribution would mean a prohibitive increase in material. Parallel powering of modules would lead to increased current and unacceptable power losses. Power must therefore be supplied at higher voltage and lower current. This might be achieved using DC-DC converters [2], or serial powering (SP), which is the baseline solution.

The use of SP results in some differences cf. traditional schemes. Some of these are outlined below. Further details are available from [3]. It is intended to build a full-size 24-module SP Stave prototype in the next year, after construction and testing of 4-module prototypes, termed Stavelets.

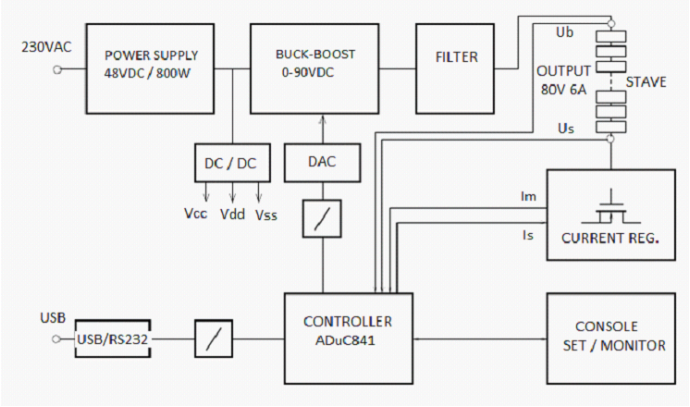

Figure 1. Architecture of the custom current source.

2 Serial powering in practice

2.1 Constant current power supply

Serial powering relies on all the readout hybrids being connected in a serial chain and powered by a constant current power supply. This must supply a voltage equal to the sum of the individual hybrid supply voltages, plus any voltage drops in the cabling.

It must be able to deliver a stable current equal to the maximum expected demand for a single hybrid. A diagram of the ATU custom current source [4] is shown in figure 1. This was designed and built at ACSR (Academy of Sciences of the Czech Republic).

There are two feedback loops in this design. The fast feedback loop uses a power FET as a current regulator, varying its conductance to give constant current through the Stave. The slow feedback loop uses an Analog Devices ADuC841 microcontroller, to monitor and tune the output voltage of the power supply, so that it is no larger than that required for correct Stave operation. This avoids dissipation of excess heat in the power FET, if a hybrid is switched out of the chain (e.g. by the detector control system (DCS)). This will be discussed in a later section.

2.2 Shunt regulation

The current drawn by the readout ASICs depends on their operational mode. The constant current supply is set to the maximum expected hybrid current and shunt regulation is used to keep the voltage across the hybrid constant. The latest generation of prototype readout ASIC is made in the IBM 250nm process and termed ABCN-25 [5]. Already, this ASIC contains custom circuitry for the implementation of shunt regulation.

There are two shunt regulation options within the ABCN-25, termed M-shunt and W-shunt. The M-shunt option uses two shunt transistors in each ASIC, controlled by a voltage from an external circuit. The W-shunt option uses both shunt and control circuitry within the ASIC itself.

Shunt regulation may also be implemented outside the readout ASIC, using discrete components or an additional ASIC. The SPI [6] is one possible ASIC solution.

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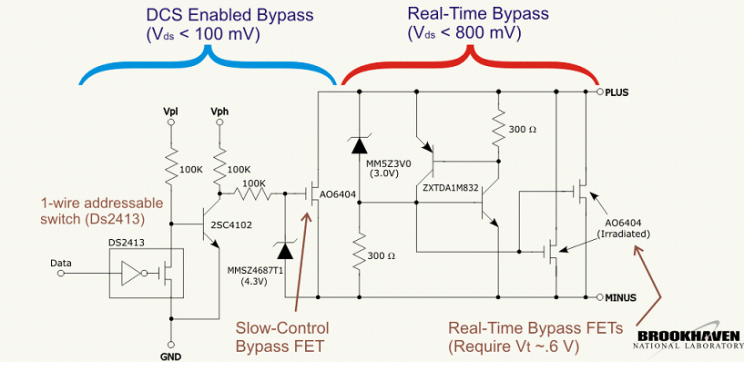

Figure 2. Circuit of the Power Protection Board.

2.3 AC coupling of signals

The hybrids in a SP chain float at different potentials, so incoming clock and command and outgoing data lines are all ac-coupled. This requires blocking capacitors on the hybrid and the end of stave (EOS) card.

2.4 Protection scheme

A concern with the SP scheme is that an open-circuit failure of a hybrid may cause the failure of an entire Stave side. It is also desirable to be able to turn individual hybrids off and on remotely. What is needed is an alternative current path in parallel with each hybrid, with the possibility of both local, autonomous activation and remote activation.

The Power Protection Board (PPB), developed at Brookhaven National Laboratory (BNL), meets these requirements. It carries two separate bypass circuits, as shown in figure 2. The real-time bypass uses a voltage reference to detect whether the voltage across a hybrid has risen above a threshold, i.e. if it is open circuit. This turns on the PNP-NPN bipolar transistor latch, which turns on the MOSFET pair. This drops the hybrid voltage to around 800mV; it is not lower because the real-time bypass derives its power from the hybrid supply. The DCS bypass uses an addressable switch IC to turn on a MOSFET. The voltage to drive the MOSFET gate is not derived from the hybrid supply, allowing the hybrid voltage to be dropped below 100mV. The real-time bypass protects against chain failure and the DCS-enabled bypass is used to isolate faulty hybrids. The DCS-enabled bypass allows powering hybrids on an individual basis and can be used to re-set the real-time bypass by pulling the hybrid voltage below the bipolar transistor latch voltage.

System tests of PPBs have been made using a chain of dummy hybrids [7]. The real-time bypass will short out a failed hybrid, without triggering any neighbouring latch. The DCS-enabled bypass can be used to turn the hybrids in the chain on or off, in any order.

3 The ABCN-25 Test Stavelet

3.1 Architecture

The first Stavelet has been assembled at Rutherford Appleton Laboratory (RAL), using modules provided by Liverpool University. This is a test vehicle, to examine options for: grounding and shielding, bus cable layout, and serial powering. A photograph is shown in figure 3.

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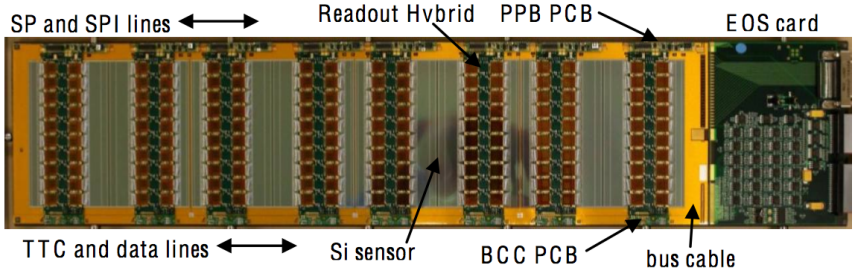

Figure 3. Photograph of the first ABCN-25 Stavelet.

The PPBs are visible along the top edge of the Stavelet. Each PPB carries a connector, which gives access to the hybrid power lines and the two M-shunt control lines. This allows the use of power regulation plug-in PCBs for testing different SP options. A multi-drop bus runs below the PPBs to allow addressing of the Fermilab SPI chip, which will be one of the options tested. For initial testing, a single-channel version of the M-shunt is included on the hybrid.

Along the bottom edge of the Stavelet, add-on PCBs carry Buffer Control Chips (BCC) [8] for each hybrid. These multiplex the outputs from the two columns of ABCN-25s onto a single bus cable line pair. They also implement a clock multiplier to derive an 80MHz clock for the ABCN-25 readout from the 40MHz LHC bunch crossing clock.

3.2 Stavelet test results

The Stavelet was powered using the current source, with shunt regulation provided by the on-hybrid M-shunt. Triggers were sent to the ABCN-25s, using the on-chip calibration system to generate input charges of 1.5, 2.0 and 2.5fC. Gain and ENC were measured for each channel over the 16 columns of chips. Mean gain for each column lay in the range 104–107mV/fC, cf. the design value of 110mV/fC. The ENC is shown in figure 4. Whilst work continues to optimise the Stavelet noise performance, it is already within the ATU specification of 750 RMS electrons. The performance of the ASICs is very similar to that measured on individual modules. Small anomalies were seen; Hybrid 2 Column 0 shows some dead channels and Hybrid 3 Column 1 shows a faulty calibration line. Zero noise appears on a few dead channels. These problems would be eliminated during production by ASIC screening. Channels with noise near 400 ENC have failed bonds. A correlation between chip column number and measured noise was found for some hybrids and has been explained further in [9].

Figure 5 shows IR images of the Stavelet in operation. On the left, the ASICs show the greatest heat dissipation. As hybrids are turned off by the DCS system, the ASICs cool down and heat dissipation instead becomes visible on the PPBs, at the position of the bypass MOSFETs. Gain and ENC were measured for the Stavelet, running every second hybrid only. Gain was unaffected, whilst a small reduction in noise was seen. We have attributed the latter to a lower overall temperature, but it will be studied in more detail.

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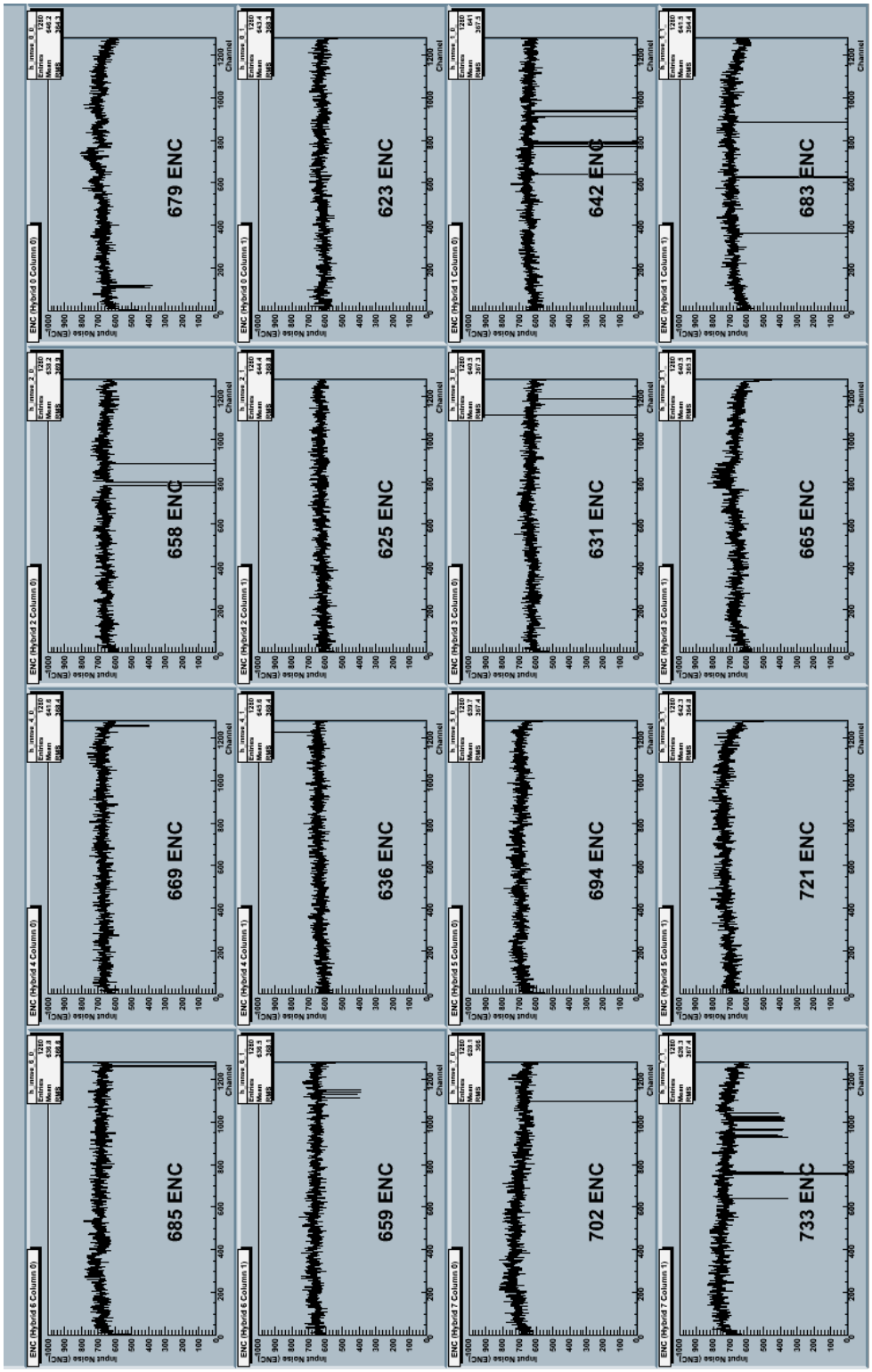

Figure 4. Noise figures for all channels — first Stavelet.

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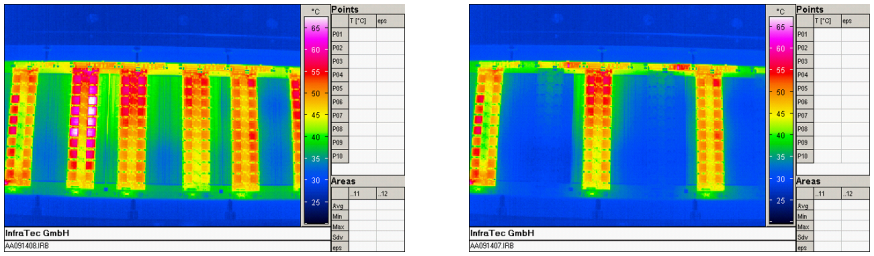

Figure 5. IR images of the Stavelet showing PPB in operation.

4 Conclusions

The first SP test Stavelet has been built and is being tested, using a custom current source. A fast bypass circuit protects against SP chain failure and a DCS bypass allows individual powering of hybrids. First results demonstrate readout of the modules, with gain and ENC as expected. Performance is not impaired by running the Stavelet with hybrids bypassed. This demonstrates that switching hybrids on or off is possible with SP, addressing a criticism which was previously aimed at such systems. Further Stavelets will be constructed and the experience gained will be used to design a 24-module, double-sided Stave for the Tracker Upgrade.

Acknowledgments

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