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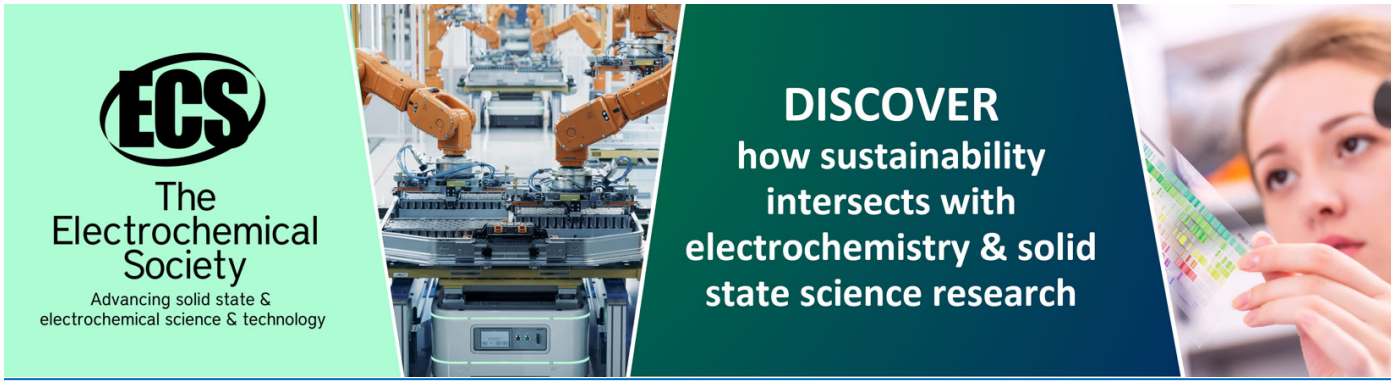

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *November 12, 2010*
ACCEPTED: *November 30, 2010*
PUBLISHED: *December 20, 2010*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

Development of a MicroTCA Carrier Hub for CMS at HL-LHC

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ABSTRACT: We are developing a MicroTCA Carrier Hub card which provides timing, control and data acquisition functions in a MicroTCA crate for HL-LHC readout electronics. This module may be mounted in the primary or redundant MCH slot in a MicroTCA crate, and distributes low-jitter LHC RF clock and encoded fast timing signals to up to 12 AMC modules. In addition, it receives buffer status signals and DAQ data at up to 600 MBytes/sec from each AMC. The prototype module is built on a commercial MCH base board with a custom mezzanine board stack. The latest Xilinx® Virtex®-6 FPGA are used to provide a clear upgrade path. Prototype modules have been developed for a CMS HCAL test beam in summer 2010. We describe the specifications of the module, its application in a MicroTCA system beyond CMS HCAL, and our experience in commissioning the module for the test beam.

KEYWORDS: Data acquisition circuits; Modular electronics

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doi:10.1088/1748-0221/5/12/C12042

Contents

1 Introduction

The CMS HCAL (Hadron Calorimeter) will be amongst the first subsystems of CMS to undergo upgrade. The current photodetectors will be replaced, with a corresponding increase of about 4x in channel count. It has been decided that as part of the upgrade the off-detector electronics will be migrated from VMEbus to MicroTCA [1]. According to the current schedule, an initial test with full prototypes operated in parallel with the existing VME system will be conducted beginning at the end of 2012. The upgrade will be completed in 2015.

2 HCAL readout crate requirements

An HCAL readout crate must provide the following functions:

- Accommodate 12 readout modules with several front-panel parallel optical components
- Initialization and monitoring (register access)
- Provide a per-BX low-latency trigger and control path
- Provide for about 1 GB/s DAQ data readout and transmission.

In the existing VME system, all but the first requirement are provided by front panel cables, resulting in a dense cable plant. We propose to develop a common standard based on a custom MCH which will provide the above functions for HCAL and hopefully other subdetectors in CMS, using only the MicroTCA backplane for intra-crate connectivity. For more details on the existing VME system, see CMS note [2] and forthcoming article [3].

A diagram of a proposed HCAL readout crate implemented in MicroTCA is shown in figure 1. 12 double-width, full-height AMC called μHTR (MicroTCA HCAL Trigger and Readout)

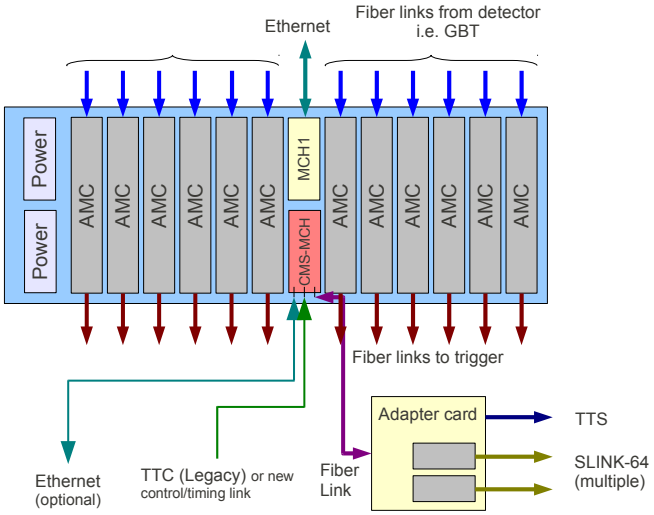

Figure 1: HCAL Readout Crate.

receive up to 18 front-end links using two SNAP-12 parallel optical receivers. The μHTR compute trigger sums which are transimitted on about 4 fibers per module to the calorimeter trigger. See references [4] and [5] for details on the front-end system and the μHTR.

In addition to the 12 μHTR, the crate houses two MCH (MicroTCA Carrier Hub) modules. The first (MCH1 in the diagram) is a commercial MCH which provides shelf (crate) management functions via IPMI [6] and GbE (Gigabit Ethernet) ports to all AMC modules. The second MCH (CMS-MCH in the diagram) is a custom module which is the main subject of this paper.

3 Custom MCH

We have developed a custom MCH based initially on a commercial base board from NAT [7]. Our custom MCH (also known as the HCAL DTC (DAQ and Timing Card) performs all essential functions for an HCAL readout crate. It consists of a stack of four PCBs in compliance with the MicroTCA standard. Figure 2 illustrates the MCH mechanics.

3.1 Functional description

This board (supplied by NAT in the prototype module) provides power and communications for the remainder of the MCH boards, including the following: Module management using IPMI; Payload power to the mezzanines; GbE switch with ports routed to AMCs and the mezzanines; an SPI (serial peripheral interface) bus.

This section describes in more detail the functioning of the custom portions of the MCH. Refer to figure 3 for a block diagram of the CMS-MCH.

Module management functions are provided by an Atmel ATMega16 [8] microcontroller. This microcontroller responds to IPMI queries from the MCH base board, and reports back the required module identification to the MMC (Module Management Controller) on the base board. In

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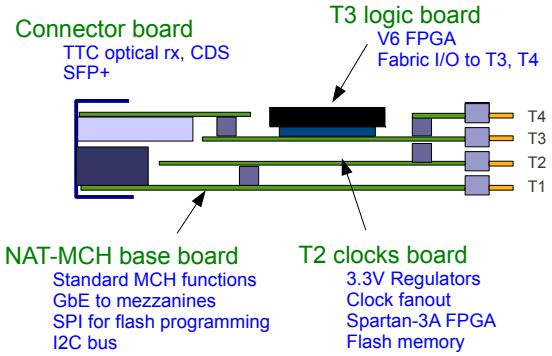

Figure 2: MCH Board Stack.

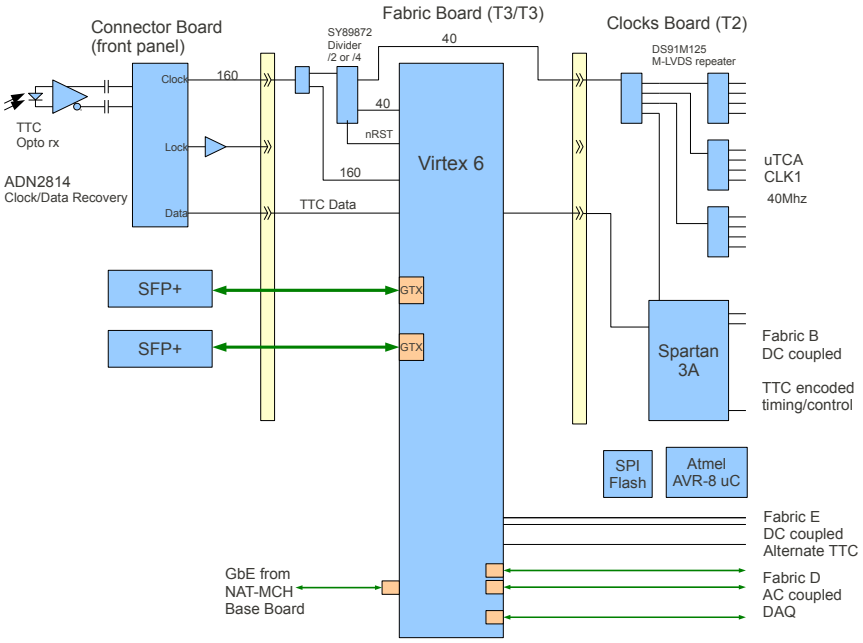

Figure 3: CMS-MCH BLock Diagram.

addition, a simple parallel bus interface to the Spartan 3 FPGA [9] is provided to allow register read/write access to the custom portions of the MCH.

Flash Memory programming is provided by means of an SPI (serial peripheral interface) bus driven by the base board. This allows for direct programming of a SPI flash memory device which directly configures the Spartan-3A FPGA. Additional space in the flash memory is used to hold configuration data for the Virtex-6 FPGA [10] on the T4 board.

Fast Timing information is received from the LHC TTC (trigger timing and controls) system [11] by an optical receiver on the connector board. The TTC is a biphase mark encoded

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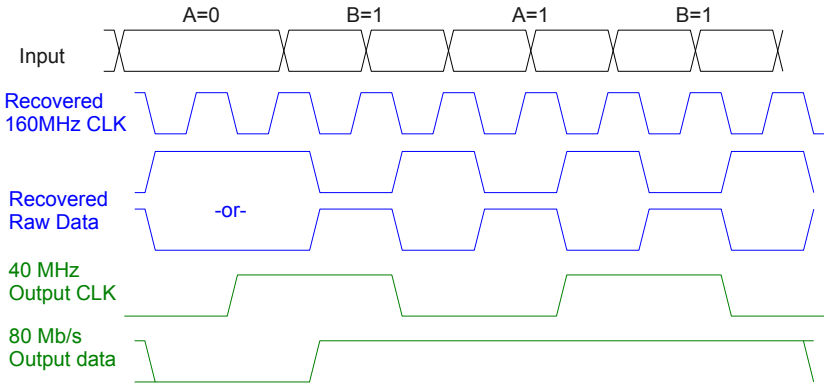

Figure 4: TTC Timing Waveforms.

bitstream carrying 80 Mb/s of data. The encoding is described in detail in the TTC documentation, but essentially two channels (A and B) are encoded serially, with a fixed clock transitions at 80 MHz and an optional transition in the middle of each clock period to indicate a logical '1'. The A channel is reserved for Level 1 triggers, while the B channel carries serialized commands such as an LHC orbit mark and event number reset. An Analog Devices ADN2814 [12] clock/data separator IC is used to extract the 160 MHz carrier clock and 80 Mb/s data from the TTC stream. An SY89872 Programmable Clock Divider [13] divides the 160 MHz clock by 4 to produce a 40 MHz clock for distribution to the AMCs.

The 40 MHz clock is sent both to the Virtex-6 FPGA and to a distribution tree on the T2 board. The Virtex-6 additionally receives the 160 MHz clock and the separated 80 Mb/s data stream. The Virtex-6 decodes the TTC stream, acquires word alignment, and provides a reset signal to the clock/data separator to ensure the correct phase of the 40 MHz clock with respect to the data.

Finally, the decoded TTC data is distributed to the AMC cards twice: first, by the Spartan-3A FPGA on the T2 board to MicroTCA fabric B, and simultaneously to MicroTCA fabric E by the Virtex-6. It is expected that one of these options will be eliminated in a future revision.

Figure 4 shows sample waveforms. At the top is the encoded data stream received from the TTC system. The next 3 waveforms show the recovered 160 MHz clock and the recovered data (two possible polarities) as output by the SY89872. The bottom two waveforms show the 40 MHz clock and decoded data as broadcast to the AMC cards by the CMS-MCH.

Data Acquisition functions will be provided by the Virtex-6 FPGA. (as of this writing these functions are not implemented). Data will be received from each AMC module at about 6 Gb/s on MicroTCA fabric D in response to each Level 1 trigger. The event fragments will be buffered in a DDR3 SDRAM, and transmitted to the CMS DAQ via a fiber link interfaced via an SFP transceiver.

3.2 Firmware

Simple firmware has been written to support required functions for an HCAL test beam effort in the summer of 2010. The firmware provides required IPMI functions and IPMI-based register access to a number of control and status registers, including numerous monitoring and error counters.

2010 JINST 5 C12042

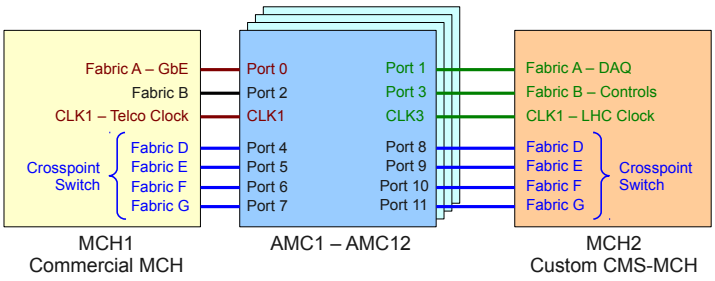

Figure 5: Proposed MicroTCA Port Use in CMS Crates

Additionally, full support for decoding and distribution of 40 MHz LHC clock and TTC timing commands is provided.

4 Software

Initial checkout of the DTC was performed using a combination of the on-board monitor of the NAT base board and the open-source `ipmitool` application. A C-callable library was constructed from `ipmitool` and contains methods for reading from and writing to registers specifically on the DTC. A dedicated command-line application called `dtctool` was then written to provide convenient, scriptable access to DTC functions. Finally, an initial set of methods to provide hardware support within the HCAL data acquisition framework was written.

5 Plans

A working group has been established to define a common MicroTCA platform for use across the CMS experiment. The CMS-MCH design will evolve as required to meet the standards established by this working group. As of this writing, we envision the following changes:

The four-board stack will be reduced to a two-board stack, with the NAT-MCH base board replaced by a custom design which functions as a 13th AMC rather than a full MCH. The base board will contain two SFP+ optical transceiver sites along with the TTC optical receiver. GbE access is provided by a cross-over link from MCH1. DAQ links will be provided on Fabric A (port 1) to the AMC cards. Finally, a tongue 2 board will provide timing and controls information on Fabric B (port 3) to the AMC cards.

Figure 5 illustrates the proposed MicroTCA port use as proposed by the working group. Fabrics A, B are used as described above. Fabrics D-G may be used for communication between AMC modules, by means of crosspoint switches located in MCH1 and MCH2.

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2010 JINST 5 C12042

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2010 JINST 5 C12042