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GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro-Pattern Gaseous Detectors

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ABSTRACT: GOSSIPO-3 is a demonstrator of a front-end chip designed in IBM 130 nm CMOS in collaboration between Nikhef (Amsterdam) and the Physics Department of the University of Bonn for the read-out of Micro-Pattern Gas Detectors. The prototype features charge sensitive amplifiers, discriminators, a high resolution Time to Digital Converter (TDC), two different Low Drop Out (LDO) voltage regulators for supply voltage control of the Time to Digital Converter, biasing circuits and control logic on a $2 \times 1$ mm$^2$ die. The chip can be operated in a time measuring mode or an event counting mode. Following the prototype announcement at the TWEPP 2009, measurement data on gain, noise performance, channel to channel ToT spread and LDO load step responses is now available. The measurement results confirm the high gain and low noise (ENC = 25 e$^-$) predicted by simulations. Stable and reproducible time bin sizes of the TDC are also confirmed.

KEYWORDS: Micropattern gaseous detectors (MSGC, GEM, THGEM, RETHGEM, MICROMEGAS, InGrid, etc); CMOS readout of gaseous detectors; Front-end electronics for detector readout; Particle tracking detectors (Gaseous detectors)

Dedicated to Ernesto.
You will be missed.

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1 Introduction

1.1 Micro-Pattern Gaseous Detectors

A modern Micro-Pattern Gaseous Detector (MPGD) consists of a gas volume and a silicon read-out chip with an array of pixels. The gas volume acts as the sensor of the detector. Particles passing the gas volume cause ionisation of gas atoms. The generated free electrons drift towards the read-out plane in an electric field. There is a special grid structure (called InGrid) 50 µm on top of the silicon read-out chip, biased at a potential of 400 V. In the gap between the grid and the chip an electron avalanche is generated from every entering electron [1]. A 3D particle track of a passing particle can be reconstructed by its projection into the read-out plane. The third coordinate is reconstructed with the help of the time of arrival information measured by the silicon read-out chip.

The advantages of this kind of detector are that there is no sensor leakage current and that the parasitic detector input capacitance is usually less than 10 fF, which results in low-noise detector electronics. The use of the special avalanche grid structure on top of the silicon surface with its gas amplification guarantees an extremely high gain and what is called the high single-electron efficiency of the detector. The timing-resolution (z-coordinate) of an ideal MPGD is only limited by the longitudinal diffusion of the drifting electrons.

1.2 The GOSSIPO-3 demonstrator

GOSSIPO-3 is a small prototype of a read-out chip for an MPGD. It has been implemented in an IBM 130 nm standard CMOS technology with 8 metal layers (cf. figure 1). The pixel size is 60 x 60 µm². The chip offers simultaneous measurements of the Time of Arrival (ToA) and of the Time over Threshold (ToT), a charge measurement technique. Alternatively, the chip can be operated in a hit-counting mode. The precision arrival time measurements are done with a TDC in every pixel.
The most prominent design goals have been to create a very low-power read-out chip with only a few micro-watts power consumption per pixel and with about 100 µs dynamic range of the ToA in order to allow for long drift times while preserving the ToA accuracy of 1.7 ns. The time bin size of the TDC corresponds to $1.7 \text{ ns} = 1/580 \text{ MHz}$, which is the oscillation frequency of the Voltage Controlled Oscillator (VCO) in the TDC. The VCO is a ring oscillator which is enabled when the discriminator senses a hit. The ToA measurement is done with a 40 MHz 12 bit counter (gives high dynamic range) and a fast 580 MHz 4 bit counter (gives precision) (cf. figure 2). Additionally ToT information is meant to be collected with an 8 bit 40 MHz counter with an accuracy of better than 50 ns or an equivalent charge of less than 200 $e^-$. 

GOSSIPO-3 makes use of a common-stop timing scheme presented in figure 3 that has been introduced in [2] and [3]. A passing particle fires the external trigger. At some point later the discriminator registers hits by electrons arriving at the read-out plane. This is the time when the fast counter with 580 MHz clock speed starts counting. The fast counter continues counting until the next rising edge of the slow clock. With this edge the fast counter stops and the slow counter starts counting at 40 MHz clock speed until the common stop signal is received and the chip prepares for the read-out of the data. The ToT is counted as long as the discriminator output signal is high with 25 ns time bin size.

The demonstrator contains three analogue front-ends consisting of preamplifiers and discriminators. The three outputs of the discriminators have been made available on pads for monitoring. One of the three preamplifier outputs is buffered and externally available for monitoring. Additionally the demonstrator contains one complete pixel cell including preamplifier, discriminator, TDC, ToA and ToT counters and digital control logic.

The supply voltage of the VCO in the TDC and thus the frequency of the VCO oscillation is controlled by Low Drop Out Regulators (LDOs) (cf. figure 4). The LDOs use 10 µF external SMD capacitors for stabilization of the output voltage. Furthermore, the demonstrator carries an InGrid preamplifier which is meant to collect the total charge gathered on the grid on top of a silicon pixel array of a future full size chip. The on-chip biasing structures can be overwritten externally if necessary.
Our experience is that the task of measuring drift times in gaseous detectors can be solved best by a Timepix-like algorithm as shown in the timing diagram below. This approach implies:

\[ \text{drift time} = t_{\text{drift}} = t_{\text{sensitive}} - \left( n_{\text{scf}}sc^{-1} + n_{\text{ffc}}fc^{-1} \right) \]

\( n: \) counts; \( f: \) frequency; \( sc: \) slow clock; \( fc: \) fast clock

Figure 3. Common-stop timing scheme.

**2 Measurement results**

**2.1 Front-end**

For measurements on the front-end performance, voltage pulses have been applied to a test pad. The pad structure has capacitive coupling to the preamplifier input. The architecture of the preamplifier has been elaborated in [2]. The injection coupling capacitance is about the same size as the preamplifier feedback capacitance. The gain of the preamplifier is determined by the ratio of the effective feedback capacitance and the injection capacitance and proved to be well reproducible. However, measurements indicate a variation in the time constant of the feedback discharge. Figure 5 illustrates the ToT measured for 3 different chips vs. the input charge injected. Whereas the ToT response is linear for every individual chip, only one of the measurements matches the results predicted by simulation. The variation of the feedback discharge time constant results in a variation of the ToT of up to 50%. Monte Carlo simulations indicate that process mismatch of the small feedback FET \((w/l = 2.4 \mu m/0.48 \mu m)\) constant current source in the preamplifier is responsible for the variation. Enlarging the feedback FET reduces the mismatch but as the parasitic capacitance across the FET represents the effective integrating capacitor of the preamplifier and determines the gain of the preamplifier, enlarging the FET is a trade-off between mismatch and the gain and noise performance of the front-end. The preamplifier noise performance measured after buffering is 4 mV RMS. The noise RMS voltage corresponds to \( ENC = 25 e^- \). This encouraging result is confirmed by post-layout simulations.

The slew rate of the preamplifier depends on the amount of charge injected into the preamplifier. Therefore the time needed to reach the threshold level of the discriminator varies. This variation is called time walk of the front-end electronics and is illustrated in figure 6. For higher amounts of charge injected, the time delay asymptotically approaches 6 ns. In post-layout simulations neglecting the digital pad drivers and pads, the delay reduces to about 2 ns. In a final full-size read-out chip no pad drivers will buffer the discriminator output but digital logic will process the hit information internally. A reduced delay simplifies offline calibration efforts.

**2.2 LDO regulators**

Two different types of LDOs are integrated on the demonstrator. As both LDOs differ in size but not in the general architecture they are referred to as small and large LDO.

In order to estimate the amount of current needed when the pixel VCOs start running, after a particle crosses the detector, several parameters need to be considered: the power consumption of a
single TDC VCO in an array of pixels, the total number of pixels of a full size chip in the experiment and the occupancy expectations for the detector. For the target application with a 256 x 256 pixel array, the average current step is calculated to be 24 mA (at average occupancy expectation of 0.37% of the pixels) and the maximum expected load step is 44 mA (at high occupancy expectation of 0.67% of the pixels). In correspondence with the VCO frequency control characteristic, it is found that a voltage drop $\Delta V_{MAX} = 31$ mV can be tolerated for the duration of the 25 ns maximum run time of the fast counter. A voltage drop of $\Delta V = \Delta V_{MAX}$ for 25 ns will result in a TDC counting error of a single time bin. Figure 7 depicts the step response of the LDO output voltage to a sudden load change of 40 mA. After a first drop the output voltage returns to its nominal value of 1.1 V violating the $\Delta V = 31$ mV threshold only for nanoseconds. The maximum output voltage of the LDOs is 1.1 V. It is considered the most critical operating point of the LDOs as the available voltage overhead for the regulating transistor in the LDO is smallest. In order to guarantee the correct oscillation frequency of the VCO in all process corners and with temperature variations from 27°C to 80°C, the LDOs need to cover a total output voltage range from 625 mV to 1025 mV. It can be seen that the LDOs recover faster than the specified 25 ns limit. In figure 8 the settling time of the LDOs for different load steps is illustrated further. The output resistance of both LDOs is below 6 Ω for reasonable load $I_{LOAD} \leq 50$ mA. The overall timing performance of the small LDO is superior to the performance of the large LDO although both LDOs fulfill the specifications. For the measurements shown in figure 7 and figure 8, a switchable load resistor has been connected externally to the LDO output. The inductance of the wire bonds and the package deteriorate the timing performance of the LDOs.

In the rare and unexpected case of extremely high occupancies $>1\%$ the LDOs cannot provide enough output current to uphold the necessary VCO supply voltage and the TOA accuracy is reduced to the 25 ns period of the slow counter. In the case of a spontaneous occupancy reduction on the other hand the LDO output behaviour does not affect the TOA accuracy as all fast counters stop synchronously on the next rising edge of the global slow clock.

Figure 5. Measured ToT vs. input charge in simulation and measurement for 3 different chips.

Figure 6. Measured timewalk (internal time delay from charge injection to when the comparator output is 'high') vs. injected charge.
In order to investigate the TDC performance we inserted the comparator hit signal directly to the digital part (cf. figure 9) and to the analogue input (cf. figure 10) of the pixel with certain delays set in 0.1 ns steps. Each delay pulse is repeated 1000 times. In theory we expect the delay scan to show a step length that is exactly the TDC time bin size of 1.7 ns. Besides, every single pulse of the 1000 repeated pulses with the same delay is expected to be counted in the same time bin in an ideal TDC. In the measurements, we see that there is a certain overlap, a transition region, between the steps and we see that some hits are associated with the neighbouring bin. The transition region increases from 10% of the TDC time bin size in the digital delay scan to 25% in the analogue delay scan for an individual chip. TDC bin zero has only half the size of the other time bins. This has been done intentionally in order to compensate the start-up delay of the TDC VCO.
3 Conclusions

The GOSSIPO-3 demonstrator chip has been fabricated, operated and measured successfully. The internal delay from the time the charge has been injected to the time the comparator signals a hit observed in the measurements is found to be dominated by the pad drivers. The effective feedback capacitance of 1 fF of the integrating preamplifier provides a high charge conversion gain. The measured RMS noise of 4 mV translates into an ENC as low as $25 e^-$. The source of the variation in the ToT measurements has been traced back to process variations due to the small size of the feedback device. This variation can be reduced by enlarging the feedback device, but leads to degraded gain performance and noise performance. The excellent high gain and low noise of the analogue front-end justifies the offline calibration effort for the ToT correction. Both LDO regulators implemented fulfill the specifications set by requirements derived for a stable 580 MHz fast counting clock in order to preserve the ToA accuracy of one TDC time bin. Additionally a good match between the simulation results for the large CMOS devices in the LDOs and the measurement results has been observed. The TDC delay scan exhibits a maximum transition region between neighboring time bins of 25% under worst case conditions for an individual chip. The reproducibility of a stable local pixel oscillator frequency and of a stable TDC time bin size for multiple chips has also been proven.

Acknowledgments

This work has been supported by the Helmholtz-Alliance 'Physics at the Terascale'.

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