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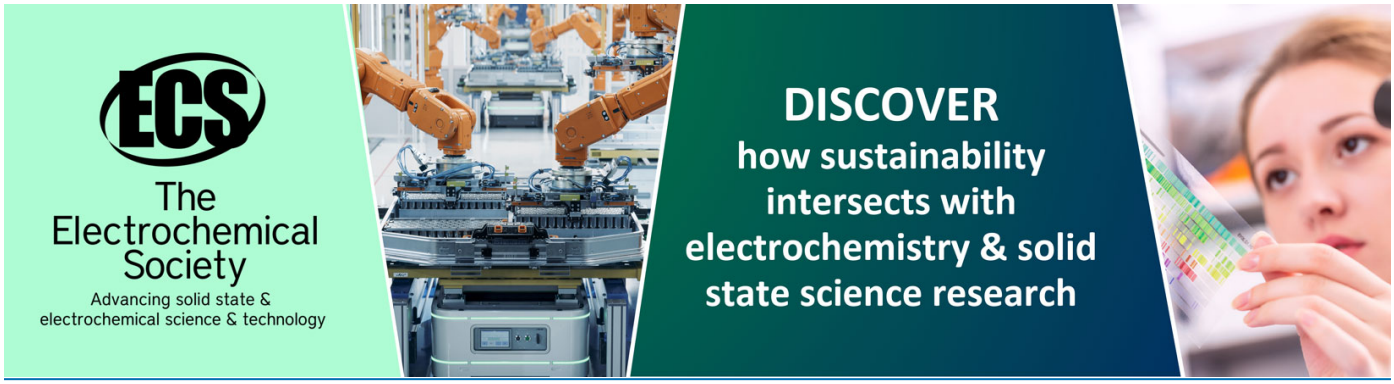

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Testing of the front-end hybrid circuits for the CMS Tracker upgrade

T. Gadek,[a,1] G. Blanchot,[a] A. Honma,[a] M. Kovacs,[a] M. Raymond[b] and P. Rose[a] on behalf of the CMS collaboration

[a] *CERN,*
Route de Meyrin, CH-1211 Geneva 23, Switzerland
[b] *Blackett Laboratory, Imperial College,*
London, SW7 2AZ, United Kingdom

E-mail: tomasz.gadek@cern.ch

Abstract: The upgrade of the CMS Tracker for the HL-LHC requires the design of new double-sensor, silicon detector modules, which implement Level 1 trigger functionality in the increased luminosity environment. These new modules will contain two different, high-density front-end hybrid circuits, equipped with flip-chip ASICs, auxiliary electronic components and mechanical structures. The hybrids require qualification tests before they are assembled into modules. Test methods are proposed together with the corresponding test hardware and software. They include functional tests and signal injection in a cold environment to find possible failure modes of the hybrids under real operating conditions.

Keywords: Detection of defects; Front-end electronics for detector readout

[1] Corresponding author.

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1 Introduction

The future HL-LHC imposes demanding requirements on its particle detectors. An increase in the intensity of proton-proton collisions results in higher radiation doses and data rates. A complete replacement of the CMS Tracker is necessary to cope with these new conditions, moreover, it must be designed to provide the most useful and accurate information about the trajectories of the collision products. To achieve these goals several features are implemented at the module level, such as lower mass, contribution to Level 1 Track Triggering functionality, and a higher density of silicon sensor read-out channels [1, 2].

Current plans for the future CMS Tracker layout assume the use of about 14,000 dual sensor modules of two main types and five different versions. One type is a Strip-Strip (*2S*) module, with a sensitive area consisting of 4,064 5-centimeter long silicon strips distributed over two sensor planes. The second type is a Pixel-Strip (*PS*) module, with a strip sensor consisting of 1,920 2.5-centimeter long silicon strips and a pixelated sensor of 30,720 1.4-millimeter long macro pixels. Different versions of a given type of module are achieved by varying the distance between sensor planes. Each module contains two high-density front-end hybrid circuits. These hybrids host binary readout ASICs and a data concentrator chip. In the PS module there are sixteen pixel read-out ASICs directly bump-bonded to the pixelated sensor and interconnected with the hybrid during module assembly. Each hybrid is equipped with auxiliary electronic components and mechanical reinforcement structures, which also serve as a cooling interface. In total over 28,000 front-end

hybrids of ten different variations will be produced. To ensure a high yield of fully functioning modules, the hybrids must be tested before they are used. Testing should allow detection of all possible failures affecting hybrid performance.

To achieve these goals, the testability of stand-alone hybrids becomes an important factor, putting constraints on the circuits and front-end ASICs designs. Although the ASICs provide much testing capability with their internal features, some other parts of the hybrid require external hardware. Additionally, the temporary connectivity of the hybrids to a readout system must be solved in order to interface the ASICs during tests.

1.1 Description of the device under test

The development of a test setup started with the 2S front-end hybrid prototypes. The structure of a complete 2S module is shown in figure 1. It consists of two microstrip silicon sensors, two front-end hybrids, and a service hybrid. The service hybrid delivers powering to the module and optical link connectivity. The front-end hybrids provide interconnectivity between sensor strips and front-end ASICs as shown in figure 2. The data path through the 2S module is shown in figure 3.

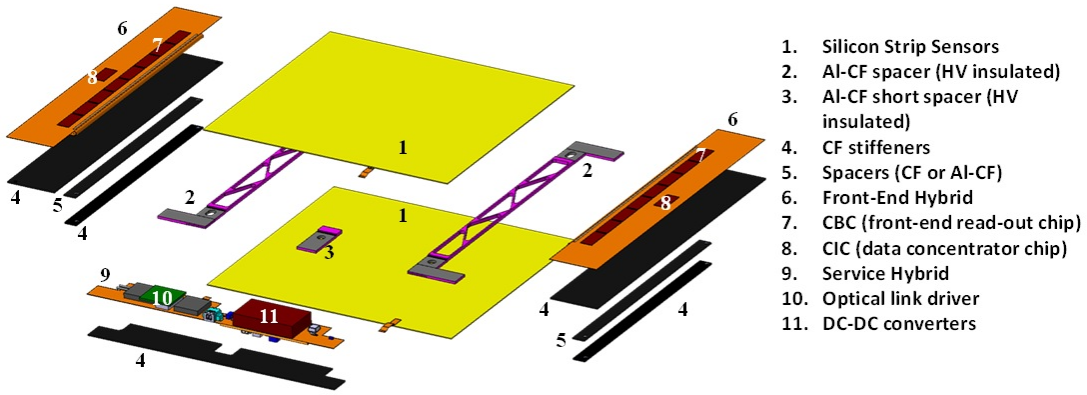

Figure 1. An exploded view of the 2S module components.

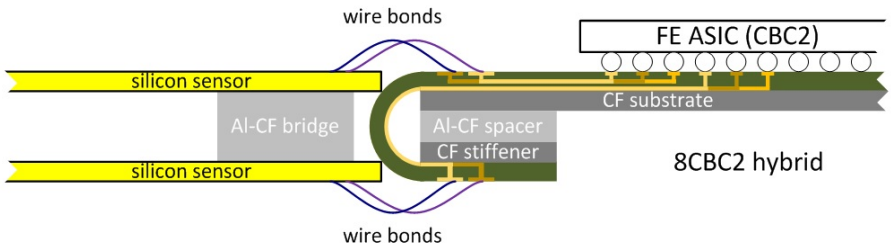

Figure 2. A cross-section sketch of the interconnection between sensors and the front-end hybrid.

The future 2S front-end hybrids will consist of a 4-layer, high-density, flexible circuit laminated onto carbon fibre stiffeners and folded over and glued to a composite aluminium carbon fibre (Al-CF) spacer (figure 1). Active electronic components mounted on this structure include eight read-out ASICs (CMS Binary Chip — *CBC* [3, 4]) and one concentrator chip (Concentrator Integrated

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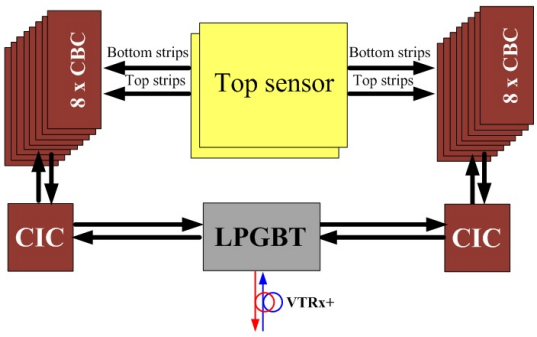

Figure 3. The data read-out scheme for the 2S module.

Circuit — *CIC*), both indicated in dark red in figure 1 and figure 3. The 2S type modules were the first prototypes built by the CMS Tracker Upgrade collaboration. These early prototypes were missing the Service Hybrid and were providing only the sensor read-out functionality without the concentrator ASIC. The first prototype was the so-called mini-module consisting of two CBC2 chips on a small, rigid front-end hybrid (so-called *2CBC2 hybrid*), and two, reduced-size strip sensors. The next generation of prototypes incorporated two full size silicon strip sensors and two flexible front-end hybrids (so-called *8CBC2 hybrids*). Both 2CBC2 and 8CBC2 hybrids are described in detail in [5] and shown in figure 4. The development of 2S module prototypes imposed a need for testing procedures for the corresponding front-end hybrids.

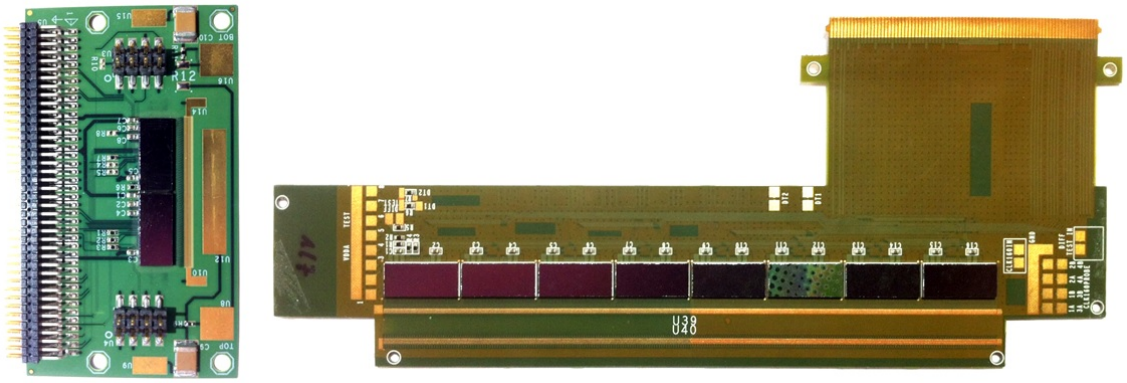

Figure 4. A photo of the 2CBC2 hybrid (left) and a photo of the flexible unfolded 8CBC2 hybrid (right).

The ASICs are produced in flip-chip technology and tested at wafer level. The non-flatness and roughness of the laminated flex in the area of ASIC bump pads can cause difficulties in the assembly. These problems have been reported by the hybrid assembling companies and have been later confirmed at CERN. These difficulties result in shorted or missing connections under the ASICs. From the hybrid testing point of view it is crucial to verify proper connectivity between chips and flex circuit traces.

The testing procedures presented in this paper were created based on functionalities implemented in the second version of the CMS Binary Chip (*CBC2*) which was the only front-end ASIC designed for the upgrade available at the time [4]. Two different hybrids hosting the chip, shown

in figure 4, were used during the development stage. Another hybrid being produced (later referred to as *PS prototype hybrid*) contains two CBC2 ASICs and implements deliberately built-in failure modes. This PS prototype hybrid will be used as a validation platform for the test setup and proposed testing methods [6].

2 Test setup proposal

The test routine will be performed at room and low temperature (−30°C) by cooling the hybrids directly via thermal contacts. The low-temperature test is intended to be representative of the tracker operating conditions. The setup is designed to keep the hybrid in a controlled dry air environment while cooling it with two Peltier modules.

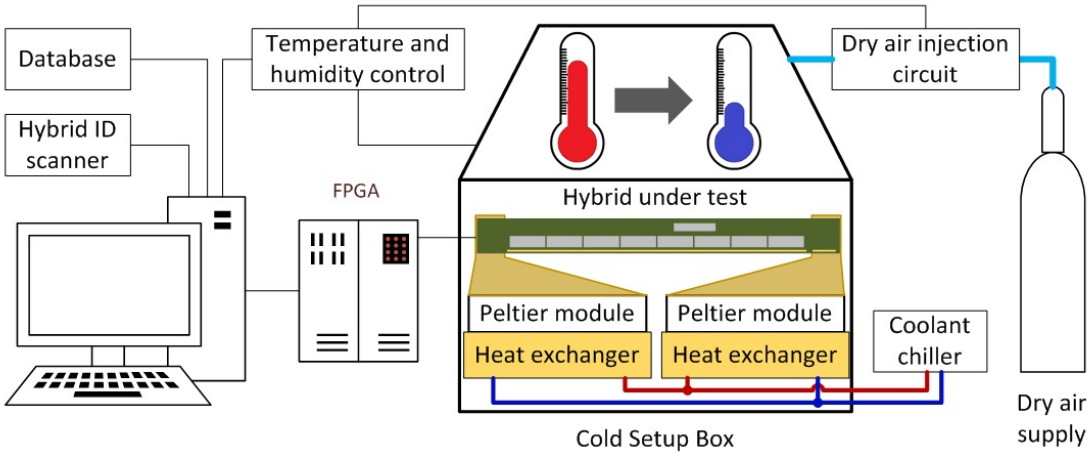

Figure 5. A schematic of the proposed test setup with the cooling functionality.

A prototype solution based on the scheme shown in figure 5 is designed and constructed to test the PS prototype hybrid. The setup is able to reach the required temperature (−30°C) at the cooling points on the hybrid. The next version of the setup will implement several improvements to reduce the required dry air flow and thus minimize heat injection into the cooling system. This should shorten the time of both humidity removal and hybrid cooling processes.

3 Description of the testing scheme planned for the 2S front-end hybrid

Some basic tests of the front-end hybrids are planned to be performed directly at the assembler premises. These include ten passive thermal cycles followed by a simple functional test (read-write of the ASICs configuration registers). At this step most of the initial defects of the hybrids should be found. Testing at the assembler is performed in order to maximize the yield of received hybrids.

Upon reception the assembled hybrids will be weighed. Firstly, due to the large number of front-end hybrids in the tracking volume, any increase in mass brings extra unwanted material in the active tracking volume, which leads to a degraded accuracy in the tracking of particles. For example, one gram of additional weight of the front-end hybrids results in a total mass gain of 28 kilograms at the tracker level. Secondly, the weight control allows to quickly detect process

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changes that may happen during manufacturing or assembling steps, which can affect the reliability of the final product.

After weighing, the hybrids will be installed in the test setup. Functional tests will be performed at room temperature followed by cooling down to the nominal tracker temperature. Functional tests foreseen for the 2S hybrid qualification consist of:

- power consumption,
- verification of ASICs configurability,
- a full calibration of front-end ASICs,
- analogue input channels testing, including:
  - a test of the connectivity of wire bond pads to ASICs,
  - verification of the fast data lines connectivity,
  - a diagnosis of input channel shorts.

In order to perform most of the operations a hybrid read-out chain is needed. In the case of 2CBC2 and 8CBC2 hybrids this consists of an interface card, an FPGA board and a PC. The interface card serves as a bridge between the FPGA and the front-end hybrid. It provides power and translates input/output signals to the voltage levels accepted by the FPGA board. The FPGA emulates the low level functions of missing ASICs, transfers trigger, clock and control signals, and receives data outputs from the front-end ASICs. The control functions and data transactions are invoked from the PC via an Ethernet link using the IPbus protocol [7]. The PC software is organized in three layers: low-level libraries implementing data transfers using IPbus functions, middleware providing operations executed on a number of ASICs (i.e. a given hybrid under test) and the user level methods written on top of the middleware, which inherit an object oriented framework for data analysis (ROOT [8]).

4 Testing methods developed for the 2S front-end hybrid qualification

Each of the foreseen functional tests, listed in the previous section, has a well-defined testing procedure.

4.1 Power consumption monitoring

The CBC2 front-end ASIC is supplied with 1.2 V, which powers directly the digital part of the chip, and an internal LDO voltage regulator provides 1.1 V for the analogue circuitry. Power consumption differs depending on the programmable bias currents and voltages in the chip. The estimated peak current consumption of the 8CBC2 hybrid is 589 mA ±4%, based on measurements of about twenty functioning 8CBC2 hybrids from different manufacturers and of different types. The measurements were always taken immediately after the execution of consecutive data read-out operations.

The acceptance test will reject those hybrids with power consumption above a given threshold. During the production of the final 2S hybrids a final set of parameters will be established based on more statistics. In the prototyping phase, so far, there was just one 8CBC2 hybrid showing

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significantly smaller peak current drain, which was at the level of 511.3 mA. Tests conducted later revealed that the hybrid had one ASIC which was not responding to the I^2C slow control interface transactions nor sending any read-out data. This chip was either not powered or not receiving the 40 MHz clock, thus disabling the digital functionality.

4.2 Validation of front-end ASICs configurability

The CBC2 chip is configured via the I^2C interface by programming a series of 8-bit registers [3]. Performing write and read operations on these registers and comparing sent values with the received ones tests the functionality of the interface. In particular the connectivity of the slow control lines and their proper functioning are verified. The values written to the registers are complementary bit patterns (binary: 10101010 and 01010101). In this way the functionality of every single bit in every register is verified. Read-back errors are listed in the test report. Failures such as shorts or opens in the bump bond region of the flip-chip would be immediately discovered if they were affecting this interface. Hybrids containing any non-configurable ASICs will be rejected.

4.3 Noise-based calibration of the front-end ASIC

The CBC2 registers include control values for digital to analogue converters, which generate biases for tuning the response of the analogue front end of the chip shown in figure 6. Most of those biases are common for the whole ASIC, such as: the gain amplifier non-inverting node voltage (V_{PLUS}) or the comparator threshold voltage (V_{CTH}). There is only one parameter (the post-amplifier *offset*) which can be fine-tuned for each individual channel [3].

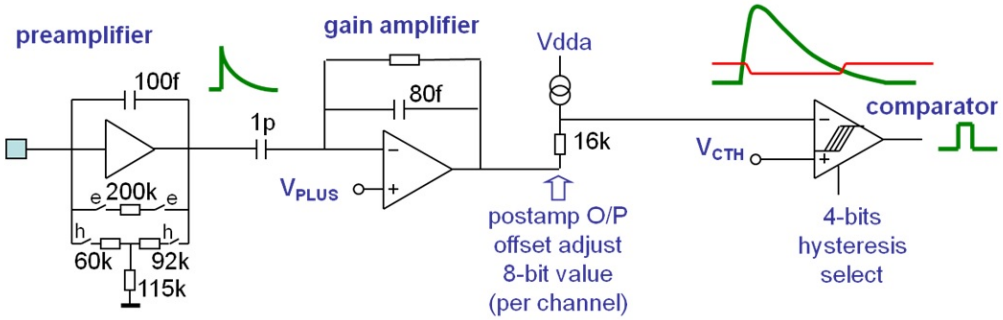

Figure 6. A schematic of the analogue front end of the CBC2 [3].

A calibration procedure searches for *offset* values such that at a fixed V_{PLUS} and V_{CTH} the response to noise of all the 254 channels is converging to the same occupancy value for a specific number of data acquisitions. The plots of channel occupancy dependence on offset have the shape of an S-curve which is a monotonic function. This property enables the use of a bisection algorithm to find the best fitting *offset* value. After calibration of the ASICs, the V_{CTH} value can be set well above the noise level at the comparator input. In this way the front-end channels should give uniform response to incoming signals, free of noise influence.

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4.4 Analogue input channels testing

After *offset* calibration and adjustment of the global comparator threshold V_{CTH} to exclude the comparators being triggered by noise, the tests verifying flip-chip bond continuity can proceed.

4.4.1 Diagnosis of the continuity of the signal paths of analogue inputs

A method was developed to detect any discontinuity in the input signal paths of the hybrid, such as missing bumps under the ASIC or broken traces. In this test a signal is capacitively coupled into the hybrid wire bond pads through two antenna boards as shown in figure 7.

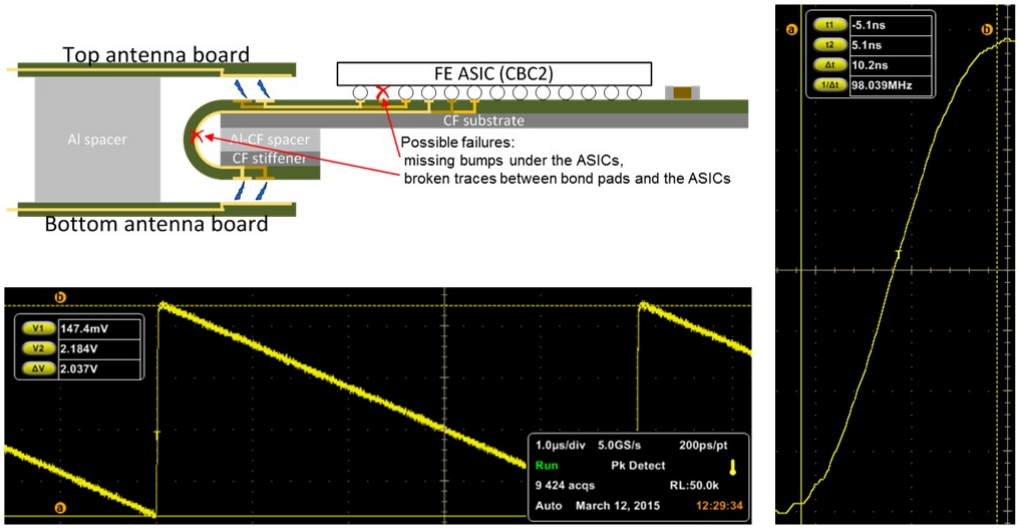

Figure 7. A sketch of signal injection into an 8CBC2 hybrid (top left). An example of a signal applied to the antenna strips during a test (bottom). Zoom on the rising edge of the signal (right).

The response of input channels to this signal is measured in the form of occupancy histograms. The test algorithm looks for channels which show low response to the signals. These are either non-functioning or potentially disconnected from the corresponding wire bond pads. An early implementation of this method has demonstrated its effectiveness, and has uncovered a weakness in the response of the CBC2 to simultaneous large input signals into many channels, a feature which will be corrected in the next version of the chip.

To allow working with the CBC2 in stable conditions the antenna strip was divided into small pads, which pulse less than 30 input channels at a time (figure 8). This new segmented antenna board is controllable from a PC via the USB interface. After a successful implementation of this charge injection scheme for 2CBC2 hybrid testing the solution was also developed for the 8CBC2 hybrid. A photo of the setup is shown in figure 9. A further development of this method is the direct implementation of the antenna in the hybrid. The upcoming PS prototype hybrid will include this feature [6].

An example of the use of the algorithm is shown in figure 10. The algorithm was run on a specially prepared 2CBC2 hybrid, which had a few edge bumps cut with a scalpel. The tool found the disconnected channels, for example the ones visible in the zoomed fragment of the occupancy histogram.

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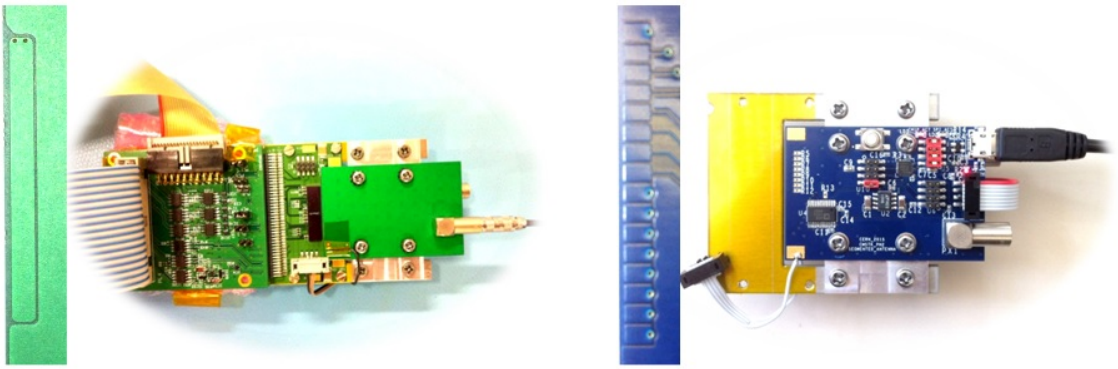

Figure 8. A picture of a setup with two single strip antenna boards, with a zoomed fragment on the antenna strip (left) and a picture of a setup with two segmented antenna boards, with a zoomed fragment on the antenna segments (right). Both were developed for the 2CBC2 hybrid testing.

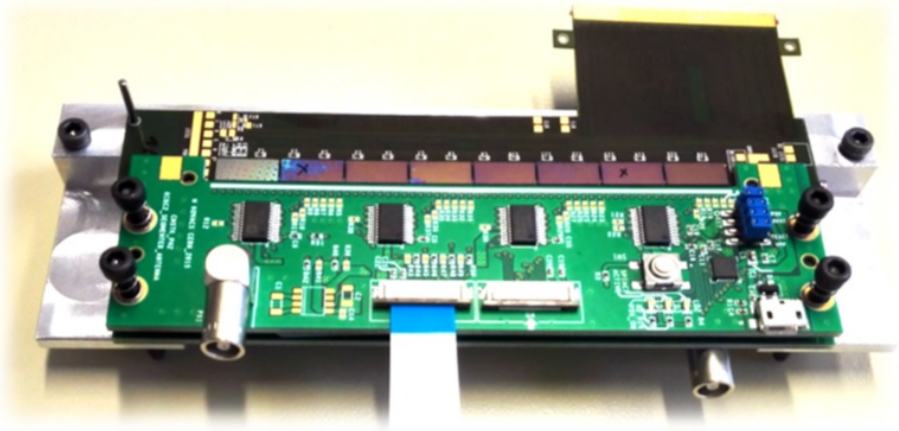

Figure 9. A photo of a setup of two segmented antenna boards developed for the 8CBC2 hybrid testing.

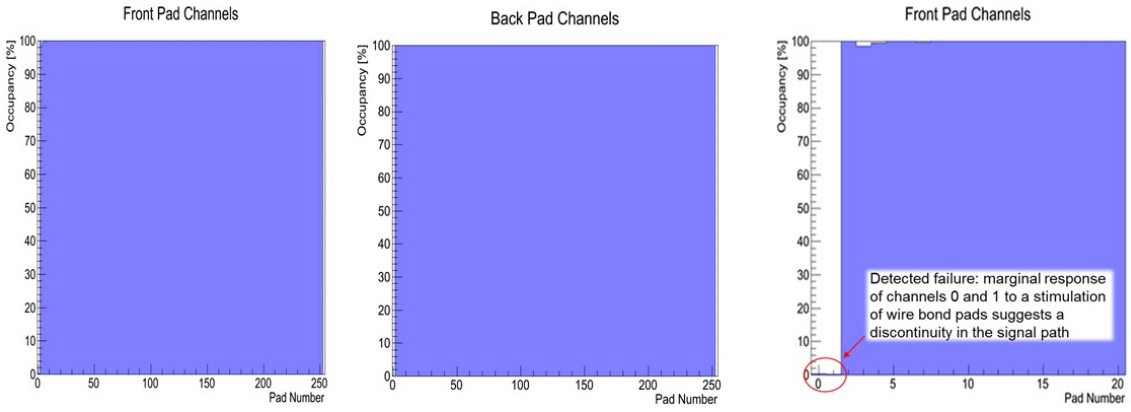

Figure 10. Occupancy histograms created during the run of a diagnosis tool with the use of external signal injection (left and middle). Zoomed fragment of the histogram showing disconnected front-end channels of the ASIC (right).

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4.4.2 Verification of the connectivity of the fast data lines

This test is done together with diagnosis of the continuity of the analogue signal paths described above. Fast data lines problems would manifest themselves as missing read-out data from the ASIC. In this case the algorithm would mark all of the input channels of the affected ASIC as malfunctioning. Therefore there is no need to provide an additional testing method.

4.4.3 Diagnosis of the mutual interconnections of analogue inputs

A method was developed to detect shorts between input channels as shown in figure 11, which cannot be visually inspected due to the fine pitch of traces and use of flip-chip technology. A test pulse generator internal to the front end chips is used as a signal source in this case [3].

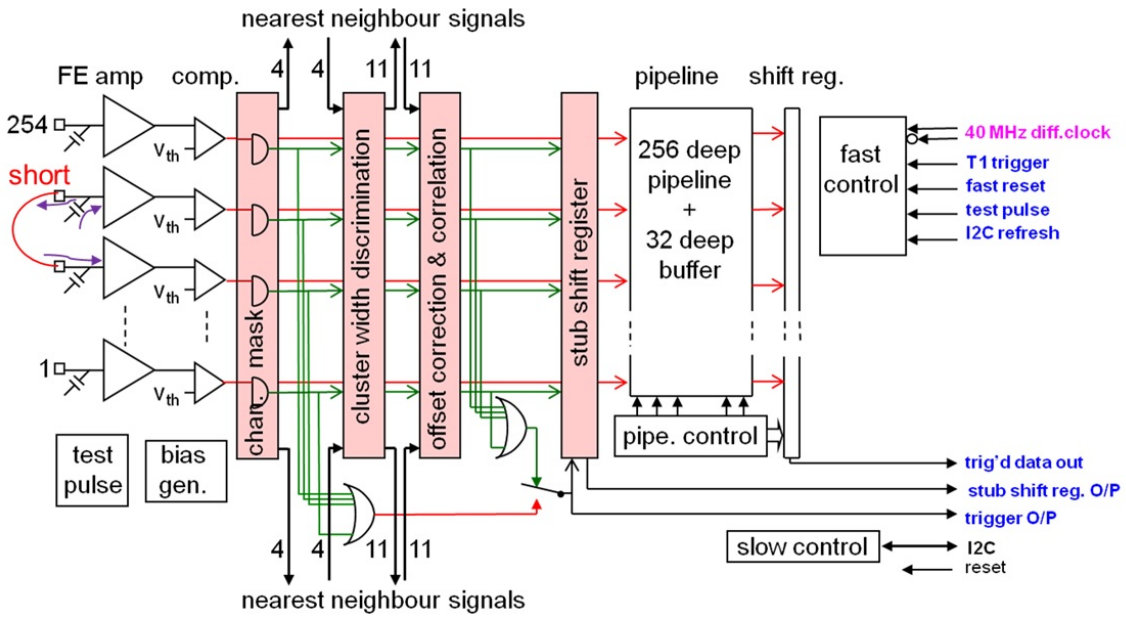

Figure 11. A schematic of the CBC2 signal path [3] with shorted channels 253 and 252. The purple arrows represent the charge flow to the front-end amplifiers when the test pulse injection is activated in the channel 253.

In the CBC2 the test signal can be applied to one of eight pulse groups consisting of 32 channels at a time. Because of a well-planned physical allocation, there are no two channels belonging to the same pulse group that are neighbouring either in the CBC2 footprint, or in the wire bond pads area. This enables the use of the test pulse injection for shorts finding. If two channels are shorted, then injecting a pulse into one of them will show unexpected activity in the other, which can be detected. This method has been validated on many hybrids and its effectiveness has been proven. Most common failures detected in the assembled 8CBC2 hybrids are shorts between bumps under the ASICs (figure 12).

Shorts other than the ones among input channels are detected by previously described methods, for example a short between data lines results in a corrupted or missing read out. A short between power lines causes extensive current drain.

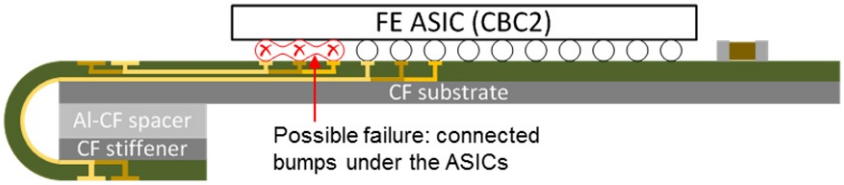

Figure 12. A cross-section sketch of a folded 8CBC2 hybrid with bumps shorted under the ASIC.

An example of use of the shorts detection method on the 8CBC2 hybrid is shown in figure 13. The algorithm found one short between two channels in the seventh CBC2, precisely at the position confirmed by the X-ray image of that ASIC.

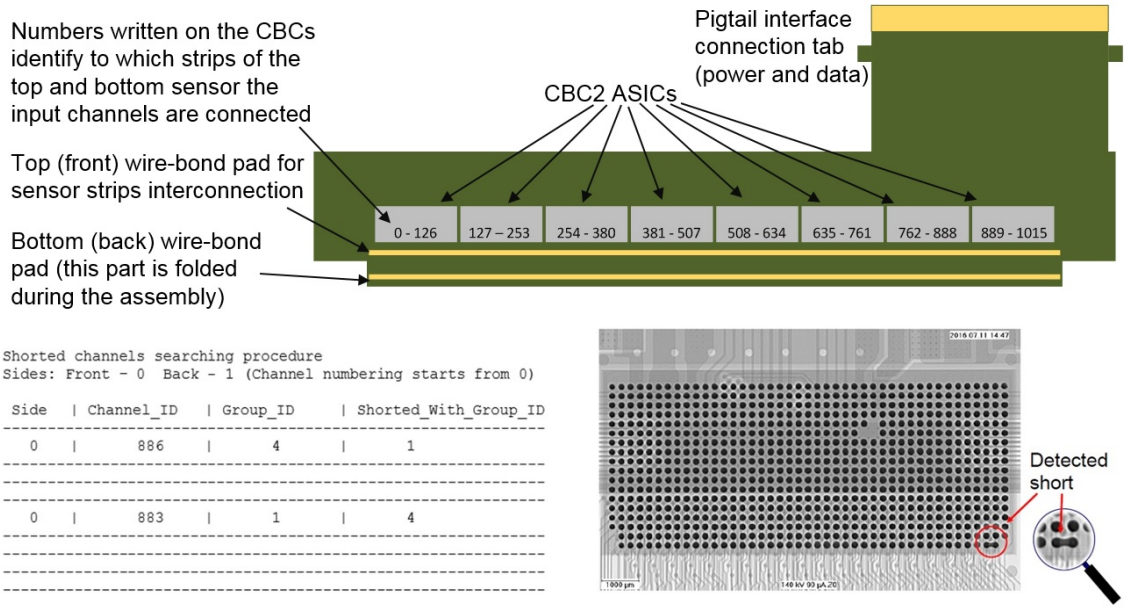

Figure 13. An explanatory sketch of an unfolded 8CBC2 hybrid (top). The printout of the developed software tool for shorts finding run on an 8CBC2 hybrid presenting a detected short (bottom left). An X-ray image of the corresponding ASIC with a short detected by the algorithm (bottom right). The three missing bumps (placed in the upper-right side from the center of the chip) are deliberately implemented for the purpose of the flip-chip orientation and positioning.

The short detection procedure can also be applied during the assembly of the modules. After wire-bonding of the sensors to the hybrids one may use it to find shorts between wire bonds or among the wire bond pads as shown in figure 14.

Detected shorts can be fixed before the encapsulation of the wire bonds thus improving the quality of modules. The algorithm has proven its effectiveness during more than ten hybrid tests. Moreover, it was run on a prototype module where it revealed a very tiny short caused by a scratch on the sensor wire bond pads shown in figure 15. This type of short would be hard to discover by a visual inspection.

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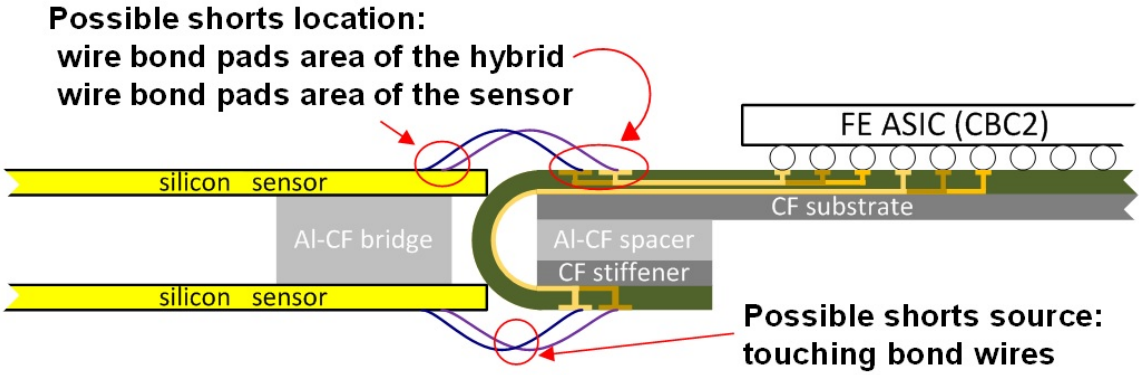

Figure 14. A cross-section sketch of an 8CBC2 hybrid wire-bonded to the sensors with identified possible locations of shorts.

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
-------------------------------------------------------------
   1    |      1012    |      3       |       2
-------------------------------------------------------------
   1    |      1011    |      2       |       3
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
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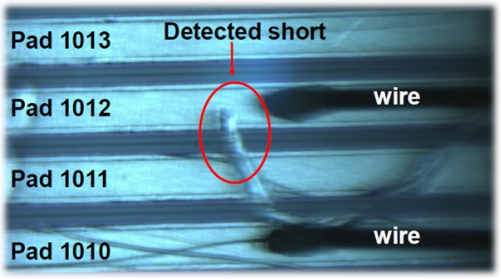

Figure 15. The printout of the developed software tool for shorts finding run on a prototype module assembly presenting a detected short between two channels (left). A microscope image of the short between pads on the silicon sensor detected by the algorithm (right). The wires connecting odd pads are not visible in the picture. They are shifted towards the right hand side because of the staggered pad pattern implemented in the front-end hybrid (as shown in figure 14).

5 Conclusion

This study was conducted with a view to the development of a common protocol for hybrid circuits testing. The study focused on the prototype 2S hybrids. The presented scheme and methods are meant to be used during the prototyping and the production phase of the front-end electronics for the HL-LHC CMS Tracker upgrade. Principles of operation of proposed test methods are defined and already implemented. These methods focus on problems observed in the prototype 8CBC2 hybrids, many of which occur during the assembly of the flip-chips on the flexible circuit. Algorithms for digital data lines testing cover all known potential failures. Results from the testing of the analogue lines seem to be very promising, however, they still require verification during the operation at low temperature. Some of the developed tools have proven to be useful also during the prototype module assembly.

The algorithms together with the corresponding hardware still need to be fully evaluated. A prototype hybrid with known failures was developed for that purpose and will be available in early 2017 [6]. In parallel to that, a cold testing setup is being developed which aims at re-creating temperature conditions of the new CMS Tracker for testing of the mentioned hybrid.

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Acknowledgments

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