SISSA

Radiation hard analog circuits for ALICE ITS upgrade

View the article online for updates and enhancements.

Radiation hard analog circuits for ALICE ITS upgrade

D. Gajanana,[a,1] **V. Gromov,**[a] **P. Kuijer,**[a] **T. Kugathasan**[b] **and W. Snoeys**[b]

[a]*Nikhef,*
Science Park 105,1098XG Amsterdam, The Netherlands

[b]*CERN,*
Geneva 23,CH-1211, Switzerland

E-mail: deepakg@nikhef.nl

Abstract: The ALICE experiment is planning to upgrade the ITS (Inner Tracking System) [1] detector during the LS2 shutdown. The present ITS will be fully replaced with a new one entirely based on CMOS monolithic pixel sensor chips fabricated in TowerJazz CMOS 0.18 μm imaging technology. The large (3 cm×1.5 cm = 4.5 cm^2) ALPIDE (ALICE PIxel DEtector) sensor chip contains about 500 Kpixels, and will be used to cover a 10 m^2 area with 12.5 Gpixels distributed over seven cylindrical layers.

The ALPOSE chip was designed as a test chip for the various building blocks foreseen in the ALPIDE [3] pixel chip from CERN. The building blocks include: bandgap and Temperature sensor in four different flavours, and LDOs for powering schemes. One flavour of bandgap and temperature sensor will be included in the ALPIDE chip. Power consumption numbers have dropped very significantly making the use of LDOs less interesting, but in this paper all blocks are presented including measurement results before and after irradiation with neutrons to characterize robustness against displacement damage.

---

[1]Corresponding author.

Contents

1 Introduction

The ALICE experiment is going to upgrade the ITS (Inner Tracking System) [1] detector during the LS2 shutdown. The present ITS will be fully replaced with a new one entirely based on CMOS monolithic pixel sensor chips fabricated in TowerJazz CMOS 0.18 μm imaging technology. The large (3 cm×1.5 cm = 4.5 cm^2) sensor chip contains about 500 Kpixels. In the outer four cylindrical layers, each stave is comprised of 2 half-staves. Each half-stave is made up of seven modules, with each module carrying 14 pixel sensor chips as shown in figure 1. The inner three cylindrical layers also shown in figure 1, consist of single module staves, where each module is a row of nine pixel chips. The pixel chips will cover 10 m^2 of area with 12.5 Gpixels in total distributed over these seven cylindrical layers. The ITS will work at room temperature. The system is required to withstand a TID of 2.7 Mrad and NIEL 1.7×10^{13} 1 MeV n$_{eq}$/cm^2 (including a 10× safety factor above the expected dose).
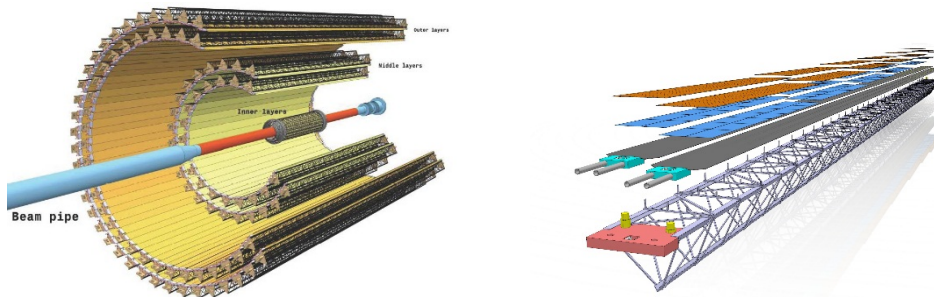

Figure 1. The ALICE ITS (L) and the full blow up of a Stave (R).

2 ALPOSE

The ALPOSE chip was designed as a test chip for the various building blocks foreseen in the ALPIDE [3] pixel chip designed for the ALICE ITS upgrade. The building blocks include: bandgap, Temperature sensor, LDOs for powering schemes. The bandgap will be used as a reference for the on-chip monitoring ADC, and the temperature sensor circuit will be used to monitor the on-chip temperature. Four flavours of bandgap and temperature sensor were designed in this R&D activity. The original power dissipation requirements (in the outer barrels was a maximum of 100 mW/cm^2) made serial powering an efficient alternative. The power numbers have since come down by an order of magnitude (< 20 mW/cm^2) and hence serial powering is not interesting anymore. The shunt Low Drop Out (LDO) regulator and the rail-to-rail opamp therein were developed for the serial powering scheme. The LDO was developed for the regular parallel powering scheme, as an alternative. The TowerJazz 180 nm Image Sensing technology works at a nominal supply of 1.8 V. A block diagram and a micrograph of the chip is shown in figure 2.
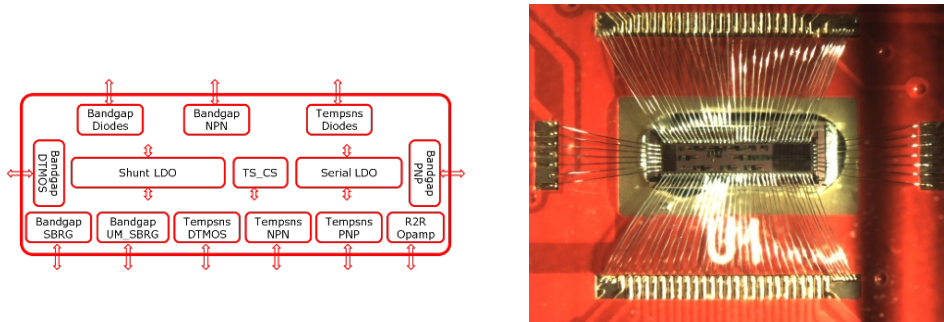

Figure 2. Block Diagram of the ALPOSE chip and the corresponding fabricated chip micrograph (L). A bonded ALPOSE on a test PCB (R).

2.1 Bandgap circuit

Many IP blocks like DACs, Opamps, and ADCs need a stable and a temperature independent reference voltage for good performance. This reference voltage should also be independent of supply variations. Such a reference voltage could be generated in many ways [4]. One of the popular approaches is to utilize the stable bandgap energy of silicon and amplify this bandgap energy to a suitable observable parameter like current or voltage.

We implemented a bandgap circuit in which a temperature and supply independent stable current is derived by summing the currents which are PTAT (Proportional To Absolute Temperature) and CTAT (Complementary To Absolute Temperature) [5]. A resistor is then used to convert this stable current into an accurate and stable reference voltage as shown in figure 3. The advantage of having currents is the ability to generate reference voltages much lower than 1 V and also to generate multiple reference voltages with ease. The V_{BE} across a diode connected transistor, working with constant current decreases linearly with temperature and hence is a CTAT voltage [4]. A resistor (R_2) across such a diode will also have a current that is CTAT. The operational amplifier is part of a feedback loop which keeps the voltages same on the branches. The opamp fixes the input voltage nodes (Node X and Node Y) to be equal. This brings the difference (ΔV_{BE}) between two

diode voltages (V_{BE} and V_{BEn}) on the resistor R_0 and hence is a PTAT voltage [4]. The current through R_0 is therefore PTAT. The opamp has a PMOS differential pair input and is of the folded cascode type. The diodes are sized differently to bring about a small difference in their V_{BE}. A total constant current I_{ref} is supplied by the current mirrors on the top. This total constant current is the sum of the PTAT and CTAT currents and is temperature and supply independent. R_1 is used to make the total current in the branch equal to I_{ref}. The IV characteristics of the left and the right branch cross at 0 and also at another voltage which is the desired working point. A startup failure condition exists if $I_{M2} > I_{M1}$ because in that case the output of the opamp will be driven against the power supply rail preventing the current sources for the reference branches to turn on. To avoid this an artificial offset is introduced by adding M3, guaranteeing that $I_{M2} < I_{M1} + I_{M3}$ and a turn-on of the current sources. Thus M3 enables the circuit to the desired operational point.

Four different flavours of bandgap circuits have been realized. These flavours mainly differ in the type of the reference element used. The different reference elements considered are regular pn diodes, bipolar transistors like npn, pnp and finally a CMOS based approach using DTMOS (Dynamic Threshold MOS) [6]. This helped in evaluating and selecting the best performing bandgap amongst the different flavours.
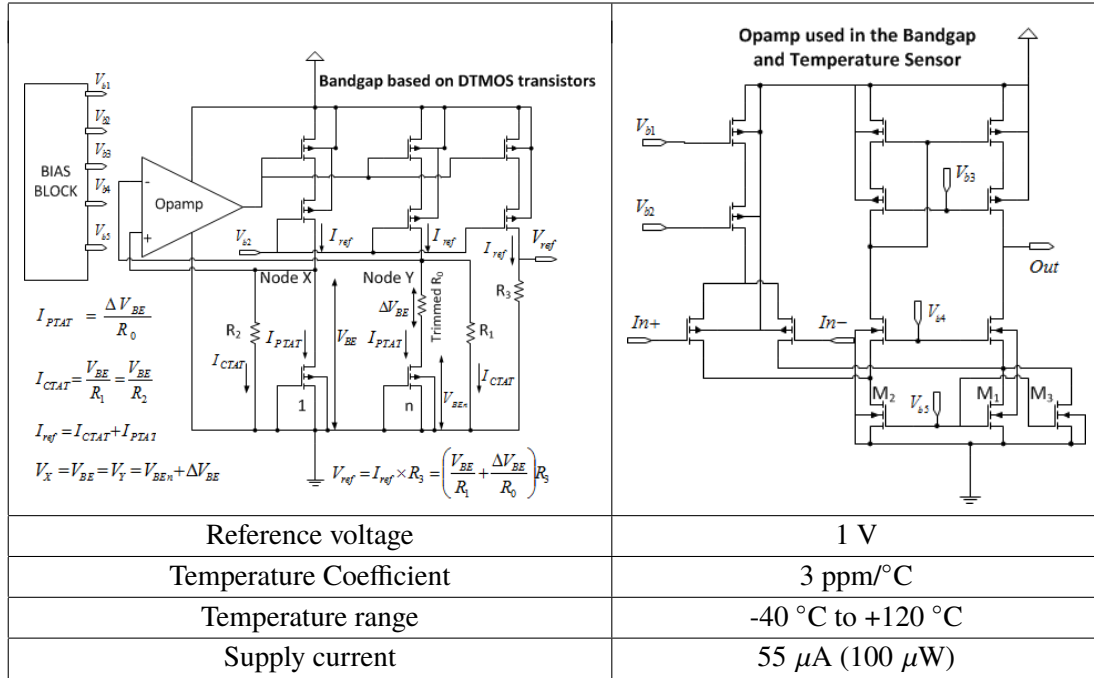

Reference voltage	1 V
Temperature Coefficient	3 ppm/°C
Temperature range	-40 °C to +120 °C
Supply current	55 μA (100 μW)

Figure 3. Bandgap circuit design based on DTMOS as reference elements, Specifications of the bandgap and the opamp circuit used in the bandgap circuit.

2.2 Temperature sensor circuit

It is important to monitor the temperature and hence the power consumption of large pixel chips. The capability to monitor temperature on the chip would significantly increase the granularity of the temperature monitoring, and would provide significant system advantages also to diagnose local issues. In a temperature sensor circuit, a detectable parameter (current or voltage) is proportional
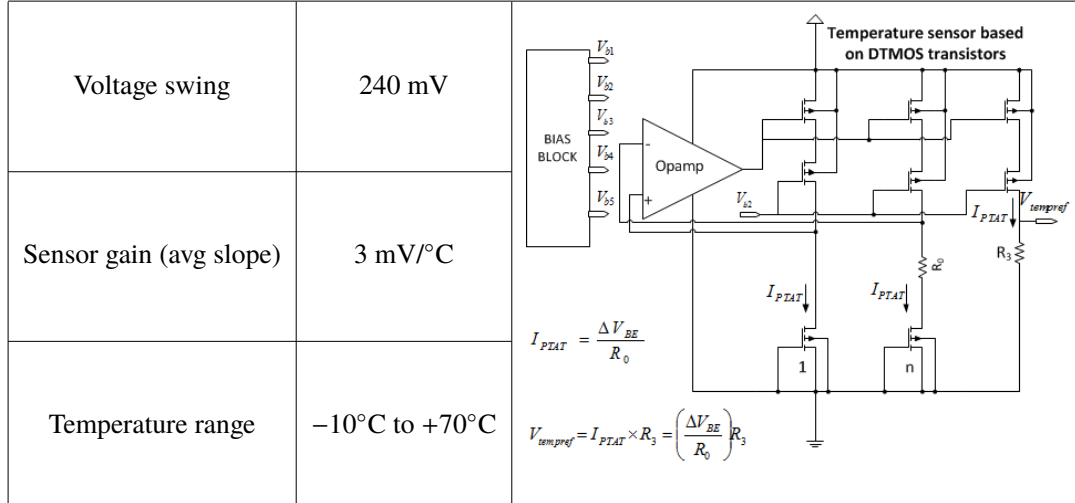
Voltage swing	240 mV
Sensor gain (avg slope)	3 mV/°C
Temperature range	−10°C to +70°C

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_0}$$

$$V_{tempref} = I_{PTAT} \times R_3 = \left(\frac{\Delta V_{BE}}{R_0}\right) R_3$$

Figure 4. Temperature sensor specifications (L) and the design (R).

to temperature. Such a circuit is designed by adapting the aforementioned Bandgap circuit. The opamp plays exactly the same role as explained before. The CTAT branch of the circuit is removed and the PTAT branch will now provide a voltage that is proportional to the temperature and act as a temperature sensor as shown in figure 4.

2.3 Low drop out regulator

A LDO [7] is used to remove or filter power supply noise in a regular voltage powering scheme. Usually these regulators are placed after a DC/DC converter to filter the ripple generated by the converter. The regulator has a serially placed power element regulating the voltage and also ensuring this regulation at a certain current specification. PMOS power elements are popularly used although there are also circuits designed with NMOS elements.

A simple opamp with a resistive feedback and a big series power transistor (M_0) is implemented to realise such a regulator as shown in figure 5. The reference voltage is provided by a diode flavour bandgap circuit previously mentioned, which is temperature independent and hence the output voltage is also temperature independent.

2.4 Shunt Regulator

In the ALICE ITS upgrade project [1], serial powering of the modules of the detector was considered to reduce the required power cabling and hence the material budget. The serial powering scheme was attractive before the power consumption of the pixel chip was significantly reduced. The pixel chips are connected in parallel at the module level and the modules are connected in series at the half-stave level. In serial powering, a constant current is sourced to build the voltage across the load to required levels. A shunt regulator [2, 8] designed (figure 6) to be integrated with the pixel chip operates in parallel with the load, which in this case is the pixel chip itself. The shunt regulator regulates the voltage by shunting any extra (source) current. Such a shunt regulator is implemented using an opamp and a big power shunt transistor (M_0). The opamp has to work rail to rail in order to fully open or close the transistor and reduce any leakage currents through the large

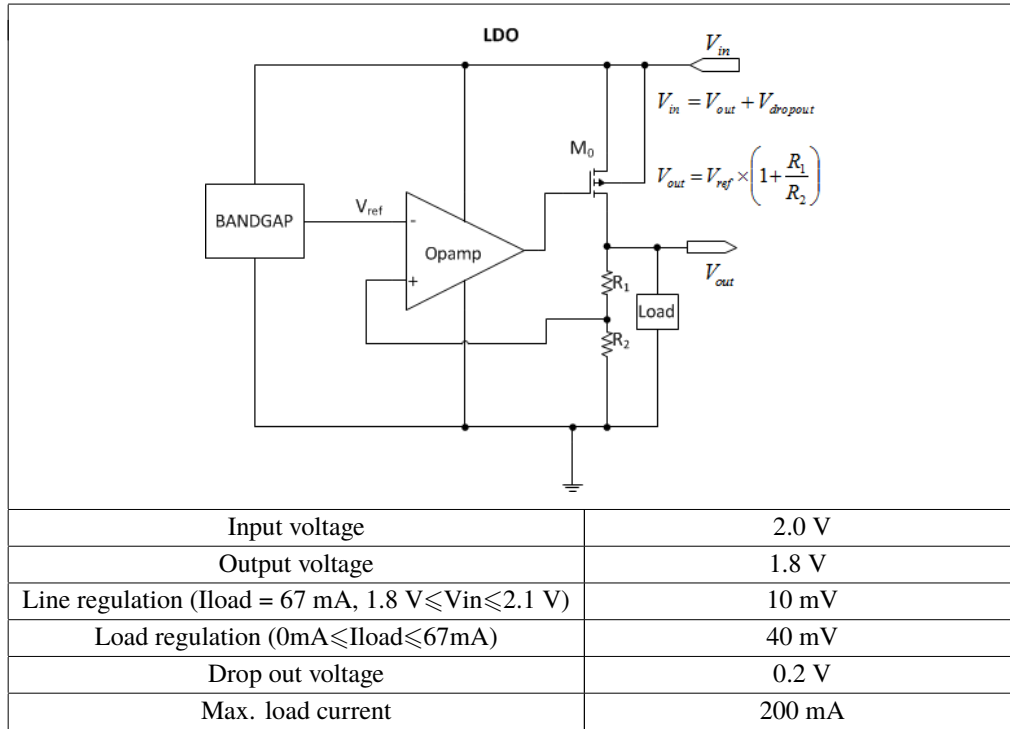|	
Input voltage	2.0 V
Output voltage	1.8 V
Line regulation (Iload = 67 mA, 1.8 V⩽Vin⩽2.1 V)	10 mV
Load regulation (0mA⩽Iload⩽67mA)	40 mV
Drop out voltage	0.2 V
Max. load current	200 mA

Figure 5. LDO specifications (L) and the design (R).

power element. A feedback mechanism is needed to sense the current flowing through the load and shunt the additional source current through the shunt transistor. The simplest form of feedback is the midpoint of 2 resistors connected in series (R_1 and R_2) between the load and the ground. It is important to make them high ohmic to reduce the power consumed in the feedback circuit. When the input source current increases, the voltage on the load increases and this voltage is sensed by the voltage divider (R_1 and R_2) and fed to the opamp. When a chain of shunt regulators are in parallel with each other, track resistance becomes an important issue. The track resistance will cause a drop in the voltage making the regulators to regulate to wrong operating points. The most likely scenario is where the first of the parallel shunt regulators takes up all the load current (no effect of track resistance) instead of it being shared equally amongst all the shunt regulators. To avoid this, the feedback resistor (R_1) was split into a local sensing point (R_{lo}) and a common middle sensing point (R_{cs}). In the ITS module, the common point was envisaged to be the supply of the 7th pixel chip as this is the middle point in the 14 parallel pixel chips.

Stability is an important issue to be considered when shunt regulators operate in parallel. The rail to rail opamp and its feedback (Rf || Cf) was carefully designed and extensively simulated for stability issues. The reference voltage for the opamp was a buffered bandgap (diode flavour) voltage. When the shunt regulators (with identical load requirements) are connected in series, the total source current needed at the input is just equal to one load, and when connected in parallel, the total source current needed is then the number of loads in parallel times the single load requirement.
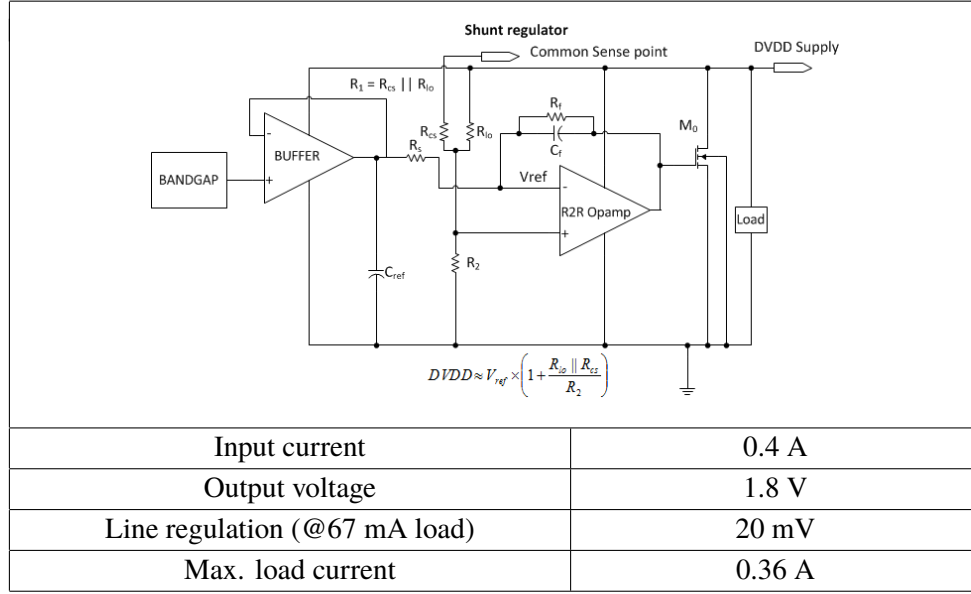
Input current	0.4 A
Output voltage	1.8 V
Line regulation (@67 mA load)	20 mV
Max. load current	0.36 A

Figure 6. Shunt regulator specifications (L) and the design (R).

3 Measurements results, before and after irradiation

A PCB was designed to directly bond the ALPOSE chips for characterization. The characterization of bandgaps and temperature sensors involved the use of climate chambers to vary the temperature and humidity. Measurements reveal a startup problem in cold temperatures ($< 0°C$) in the diodes and bipolar flavoured bandgaps. To illustrate this, a reference measurement of a diode flavoured bandgap at $-10°C$ is shown in figure 7, against a bipolar flavoured bandgap that fails to start at $-10°C$.

If the bandgap had already been powered up at a higher temperature and then the temperature lowered, the bandgap showed full functionality — clearly indicating a startup problem and not a functional problem. It was also proved with 100 measurements on a single sample at cold temperatures that, in majority of the cases, the diodes and bipolar flavoured bandgaps did not start up. The DTMOS flavoured bandgap always started up reliably at all temperatures. The ratios of the reference elements in the two branches of the bandgap design must be chosen very carefully in order to provide a good operation point. Simulations show that the I-V curves of the two branches in the diodes and bipolar flavoured circuits are too close to each other in the present silicon implementation with the risk that for large temperature variations they exhibit more than one crossing point apart from the one at zero current, causing the bandgap to converge to the wrong crossing for a cold start-up, but to maintain converged to the right crossing if after a warm start-up the temperature is lowered. ALICE will work at room temperature, but the DTMOS bandgap was selected for the ALPIDE chip for robustness and because it exhibits a very low temperature coefficient. Regulators had a variable current load by changing jumpers on respective resistive loads and also tested at different supply voltages. The LDO starts to regulate only when Vin > Vout + Vdropout and the shunt regulator will regulate only when Isource > Iload. Line and load regulation measurements for the LDOs were also carried out (figure 7) based on the new reduced power consumption requirements for the pixel chip.
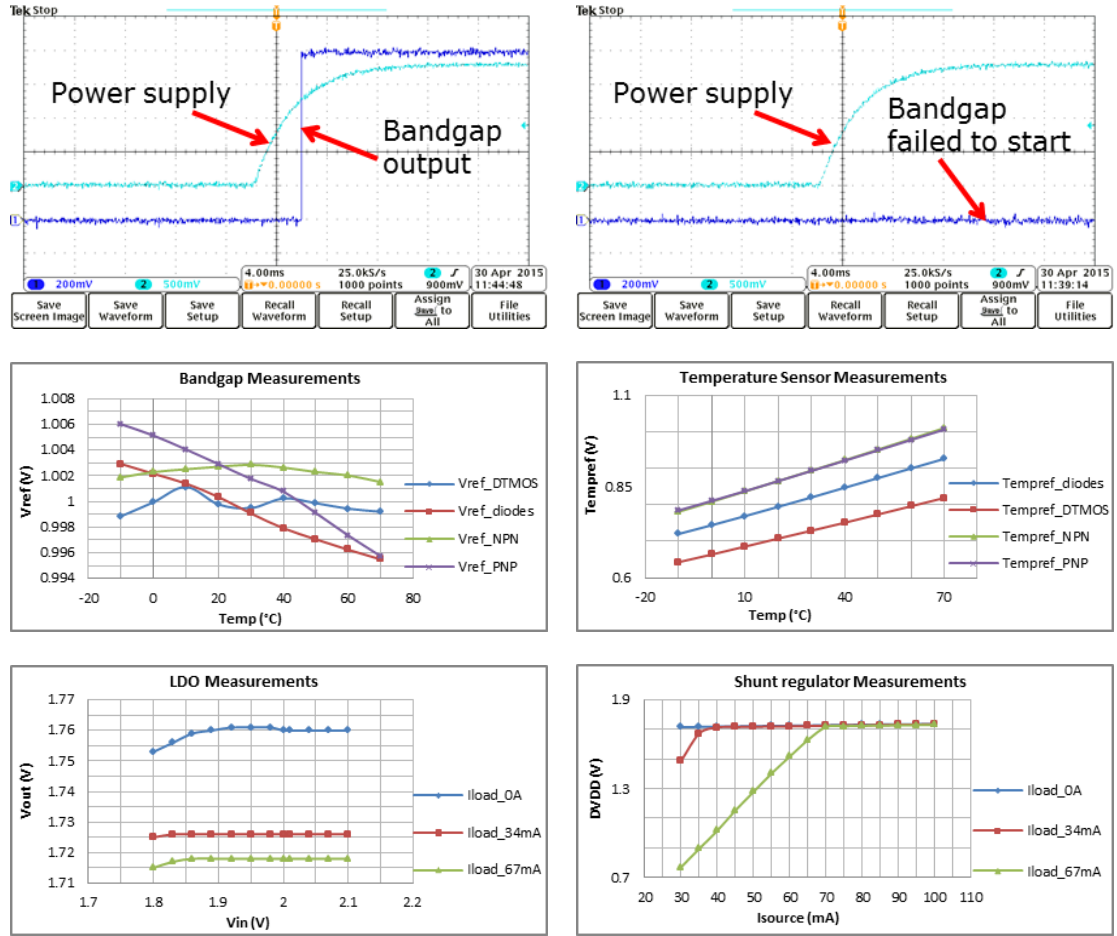
Figure 7. First row: reference measurement of a diode bandgap correctly starting up at $-10°$C, startup failure of a bipolar transistor bandgap at $-10°$C. Second row: bandgap and Temperature sensor measurements w.r.t. temperature. Third row: measurements on Serial and Shunt regulator w.r.t. source voltage and source current respectively.

ALPOSE chips with different epitaxial layer thicknesses (18 μm and 30 μm) were exposed unbiased to neutron irradiation at 1×10^{13} and 1.7×10^{13} 1 MeV n_{eq}/cm^2 (specification for the inner barrel including a 10$\times$ safety factor). No significant differences with non-irradiated chips were observed, except for the temperature sensors, where irradiation introduces a systematic offset ($\sim$50 mV) as shown in figure 8, but this is not an issue for this application.

4 Discussion, conclusions and future

Serial powering of ALPIDE is no longer considered after the significant reduction of power consumption in the pixel chip from 100 mW/cm^2 to $\sim$20 mW/cm^2. Cold startup problems of the bandgaps exist for the bandgaps with bipolar reference elements. All blocks are functional (extensive measurements on Bandgaps, temperature sensors, rail-to-rail opamp and the regulators) and in line with the simulation results. The DTMOS based bandgap and the DTMOS based temperature sensor will be included in the final ALPIDE pixel chip, as the temperature sensitivity is small and
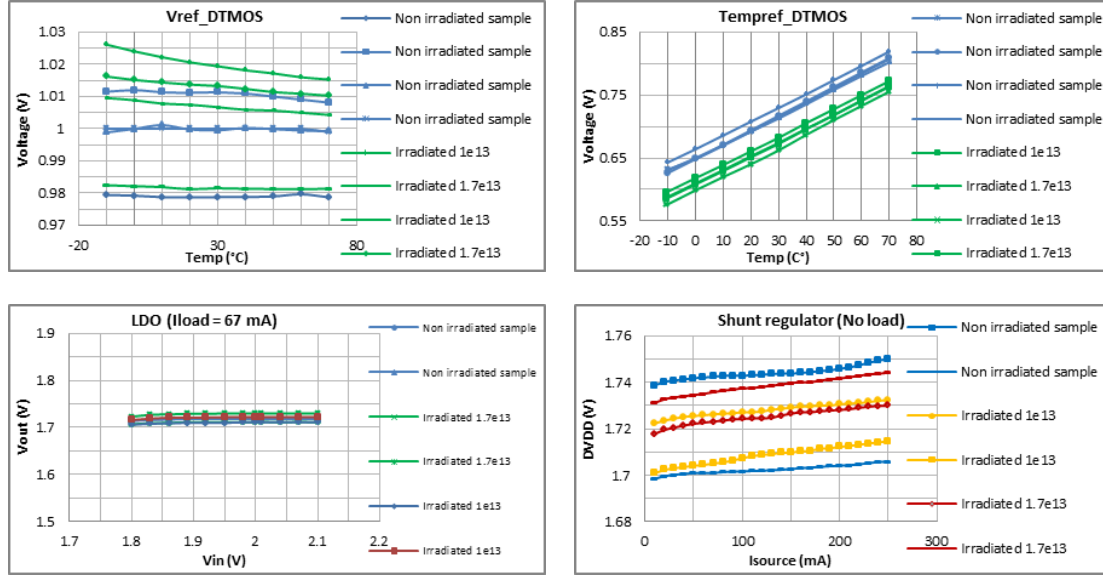
Figure 8. Measurement results after neutron irradiation; first row: bandgap and Temperature sensor measurements w.r.t. temperature. Second row: measurements on Serial and Shunt regulator w.r.t. source voltage and source current respectively.

there is reliable startup in a big temperature range. Gamma irradiation of the ALPOSE chips is foreseen in the near future but neutron irradiation does not show significant effects in any of the circuit structures.

Acknowledgments

References

[1] ALICE collaboration, B Abelev et al., *Technical design report for the upgrade of the ALICE inner tracking system*, *J. Phys.* **G 41** (2014) 087002.

[2] M. Karagounis et al., *Development of FE-I4 pixel readout IC*, talk given at the *Topical Workshop on Electronics for Particle Physics (TWEPP2008)*, September 15–19, Naxos, Greece (2008).

[3] G. Aglieri et al., *Monolithic active pixel sensor development for the upgrade of the ALICE inner tracking system*, 2013 *JINST* **8** C12041.

[4] W.M.C. Sansen, *Analog design essentials*, Springer (2006).

[5] H Banba et al., *A CMOS bandgap reference circuit with sub-1-V operation*, *IEEE J. Solid-State Circ.* **34** (1999) 670.

[6] V. Gromov et al., *A radiation hard bandgap reference circuit in a standard* 0.13 *μm CMOS technology*, *IEEE Trans. Nucl. Sci.* **54** (2007) 2727.

[7] G.A. Rincon-Mora and P.E. Allen, *A low-voltage, low quiescent current, low drop-out regulator*, *IEEE J. Solid-State Circ.* **33** (1998) 36.

[8] M. Karagounis et al., *An Integrated Shunt-LDO regulator for serial powered systems*, in proceedings of the *IEEE European Solid-State Circuits Conference*, Athens, Greece, p. 276 -279, 2009