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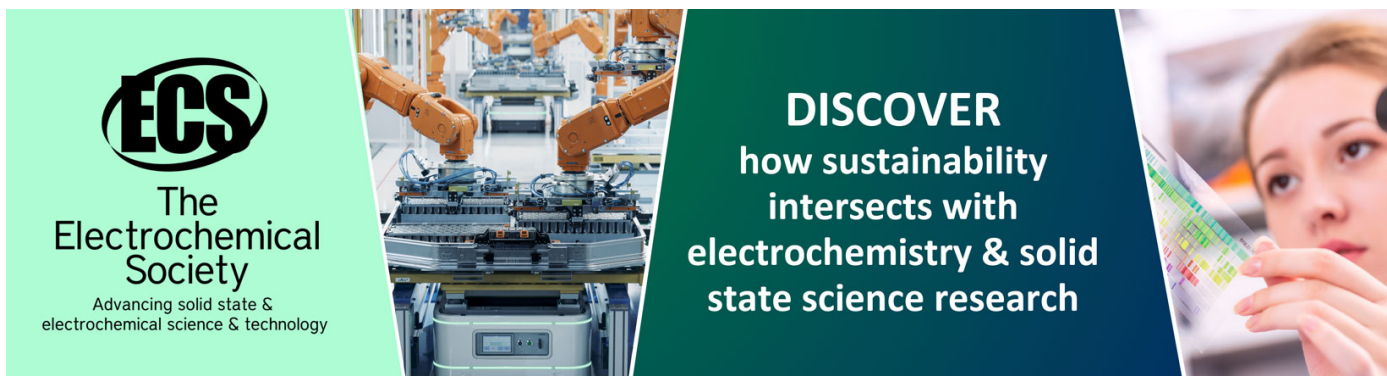
The design of a fast Level 1 Track trigger for the ATLAS High Luminosity Upgrade

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The design of a fast Level 1 Track trigger for the ATLAS High Luminosity Upgrade

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Abstract. The ATLAS experiment at the high-luminosity LHC will face a five-fold increase in the number of interactions per collision relative to the ongoing Run 2. This will require a proportional improvement in rejection power at the earliest levels of the detector trigger system, while preserving good signal efficiency, due to the increase in the likelihood of individual trigger thresholds being passed as a result of pile-up related activity. One critical aspect of this improvement will be the implementation of precise track reconstruction, through which sharper turn-on curves, b-tagging and tau-tagging techniques can in principle be implemented. The challenge of such a project comes in the development of a fast, precise custom electronic device integrated in the hardware-based first trigger level of the experiment, with repercussions propagating as far as the detector read-out philosophy.

1. Introduction

The ATLAS experiment [1] studies high energy proton-proton collisions produced at the Large Hadron Collider [2]. The full data volume which can be produced by the ATLAS experiment is too large to store in its entirety and the readout rate would be beyond the capabilities of current technologies. To reduce the event rate, ATLAS uses a highly-selective trigger built from custom hardware and a CPU farm. Track-based triggering is currently only performed in the High Level Trigger (HLT) and not implemented in early stage hardware-based systems.

The high-luminosity LHC is expected to deliver an instantaneous luminosity of approximately $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. This represents a huge potential reach into new physics as well as the opportunity to improve the precision of current measurements and study previously unobserved Higgs decay modes. The increased luminosity also increases the pile-up¹ to $\langle \mu \rangle = 200$ which represents a challenge for the ATLAS trigger both in terms of event rate and the high flux of particles passing through the detector volume. Pile-up this high would saturate the current HLT and push the readout rate beyond capabilities.

Operating the current trigger within readout constraints would require increasing by a large amount the p_T , transverse momentum, thresholds of single lepton triggers, which contribute a significant proportion of the overall rate. This would lead to a large loss of physics potential so alternative strategies have been explored. To achieve a rate reduction comparable to increasing p_T thresholds for single lepton triggers, one option is to use hardware-based track reconstruction

¹ The average number of proton-proton interactions per bunch crossing.



as an additional discriminant for features identified in the other hardware-based trigger systems. This may give an additional opportunity to increase the acceptance for muons, especially in the most central regions. The projected trigger rates for electrons and taus as a function of the trigger p_T threshold as well as the reduction in tau trigger rate expected from the inclusion of tracking information are shown in Figure 1.

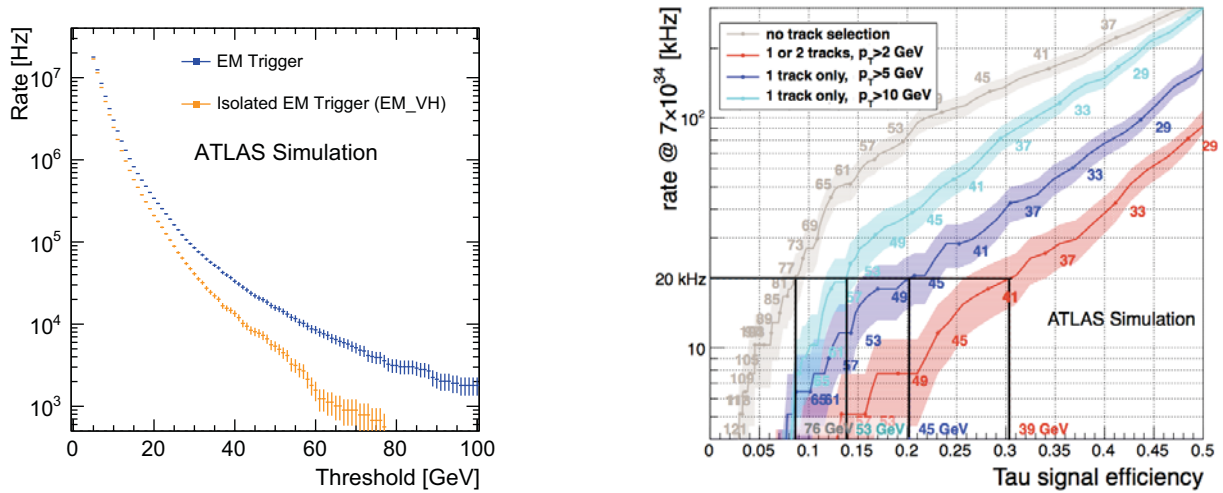


Figure 1. Left: Projected trigger rates as a function of trigger p_T threshold for isolated electron and inclusive EM triggers. The EM triggers which do not pass the hadronic isolation criteria, and are therefore included in the isolated electron rate, contain a large proportion of taus. Right: Trigger rate vs. tau finding efficiency curves for taus from the decay of a 120 GeV Higgs boson for the inclusive tau trigger at a luminosity of $\sim 7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ for different track multiplicity and minimum track p_T requirements. The bands show the efficiency against rate parameterised for different L1 cluster E_T , transverse energy, thresholds, shown as the small numbers next to the corresponding points on each band. The thresholds for each band, such that the integrated rate from the trigger is 20 kHz, are shown at the bottom of the plot.[3]

2. Level 1 Track Trigger System Design

The proposed Level 1 Track trigger baseline design consists of a system of multiplexed FPGAs and Associate Memory(AM) ASICs [4]. The system would be seeded by Regions of Interest (RoIs) defined by the hardware-based Calorimeter and Muon triggers which are similar to the current Level 1 systems. The RoIs in a single event would cover a maximum of 10% of the detector volume. Upon a readout request, the inner tracking detector clusters within the RoI would be passed through the detector electronics to the Level 1 Track trigger.

The clusters are initially processed using only coarse granularity inner detector spatial information called a “superstrip”. The superstrip information is passed through the AM chips to check for matches against a collection of template patterns consisting of one superstrip per detector layer. Patterns are pre-computed using $\sim 100\text{m}$ simulated single muons in each $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ region. The sample muons are produced flat in $\frac{1}{p_T}$ with $p_T > 4 \text{ GeV}$ and impact parameters² restricted to $|d_0| < 2 \text{ mm}$ & $|z_0| < 150 \text{ mm}$. The aim is to require a maximum of 1 million patterns per region. To improve coverage, and account for geometrical inefficiencies, some patterns use wildcards which allow certain layers to not contain a hit. To

² The transverse and longitudinal impact parameters, d_0 and z_0 respectively, of the single muons' tracks.

reduce the number of patterns required to be stored, “Don’t Care Bits” are introduced which merge patterns that are almost identical.

The next stage of the process is to apply a track fitting procedure to the full granularity hits for patterns which have been matched. This stage would be performed within FPGAs to select tracks for a global Level 1 decision. The track fitting is performed by applying a set of fit constants to relate the cluster positions $\{x_j\}$ to the 5 track parameters $\{p_i\}$ using a linear approximation as shown in Equation 1. A similar relationship is used to relate the cluster positions to a χ^2 measuring the quality of the fit.

$$p_i = \sum_{j=1\dots N} C_{ij}x_j + q_i \quad (1)$$

The constants $\{C_{ij}, q_j\}$ are produced by a principal component analysis using a large sample of simulated single muons. Clusters on different modules in the same layer do not have continuity in cluster position which would break the linear approximation. This then defines a sector as a given set of detector modules, one per layer. A set of constants is therefore produced and stored for each sector. For each matched pattern the corresponding sector is found and the constants for that sector applied. Candidate tracks are accepted or rejected based upon the value of the χ^2 computed and then accepted tracks have their track parameters computed using Equation 1. For matched patterns containing a wildcard, a set of constants with the relevant layer removed are used. In the case of patterns containing multiple hits within a single layer, each possible combination is evaluated and the best is kept through use of a suitable figure of merit.

3. Expected Performance

The performance of the pattern matching and track fitting algorithms is evaluated in discrete η regions as the procedure is performed using different tracker layers in each region. The results for the $0.1 < \eta < 0.3$, $0.3 < \phi < 0.5$ region, which has been studied in most detail, are shown here. The majority of results have been produced using only strip detector layers but an improvement has also been observed for replacing the innermost layer of strips with the outermost layer of pixels.

The efficiency of the pattern matching (fraction of events with at least one matched pattern) and track fitting (fraction of those events with at least one successful track fit with a χ^2 below 40) are shown in Table 1 for the $0.1 < \eta < 0.3$, $0.3 < \phi < 0.5$ region using both the strip only and strip plus pixel configurations. Both configurations use the ATLAS Phase II upgrade Letter of Intent layout [3]. The resolutions of each of the track parameters for single muon events, with no additional pile-up, are shown in Table 2 using the same region and configurations.

Table 1. The pattern matching efficiency, ϵ_{pat} , and track fitting efficiency, ϵ_{fit} , for single muons and $< \mu > = 200$ minimum bias events as well as the average number of fits required for minimum bias events for the two layer configurations[5].

	Single Muon		Min. Bias		
	ϵ_{pat}	ϵ_{fit}	ϵ_{pat}	ϵ_{fit}	$< N_{fits} >$
Strip Only	99.4%	99.5%	92.5%	7.5%	114
Strip+1 pixel	99.5%	99.7%	99.0%	61.5%	331

To understand the expected performance at the high-luminosity LHC, events more realistic than single isolated electron and muon events must be used. These are created by taking the

Table 2. Track parameter resolutions for the two layer configurations[5].

	Curv [GeV^{-1}]	ϕ	η	d_0 [mm]	z_0 [mm]
Strip Only	0.003	0.001	0.002	0.3	1.7
Strip + 1 pix	0.003	0.001	0.001	0.2	0.3

single isolated lepton events (weighted to the spectrum expected from L0 triggers) and overlaid with $\langle \mu \rangle = 200$ pile-up. The efficiency of these signal type samples are compared with the efficiency of a candidate background sample consisting of tracks originating from b-jets. The efficiencies of both samples are shown in Figure 2 as a function of the cut on the candidate track's p_T , as calculated by the track fitting. The pattern fit constants are produced using single muons but can also be applied to electrons. Three strategies are tried to select the best track from the possible candidates: the highest p_T track of those with $\chi^2 < 40$, the highest p_T of the two with the lowest χ^2 or the lowest χ^2 track. Current studies show strategy B, the highest p_T of the lowest two χ^2 tracks, to be the optimal choice for efficiency and background rejection. The efficiency for the background sample comes mostly from the large number of combinatoric possibilities of hits found within the b-jet cone.

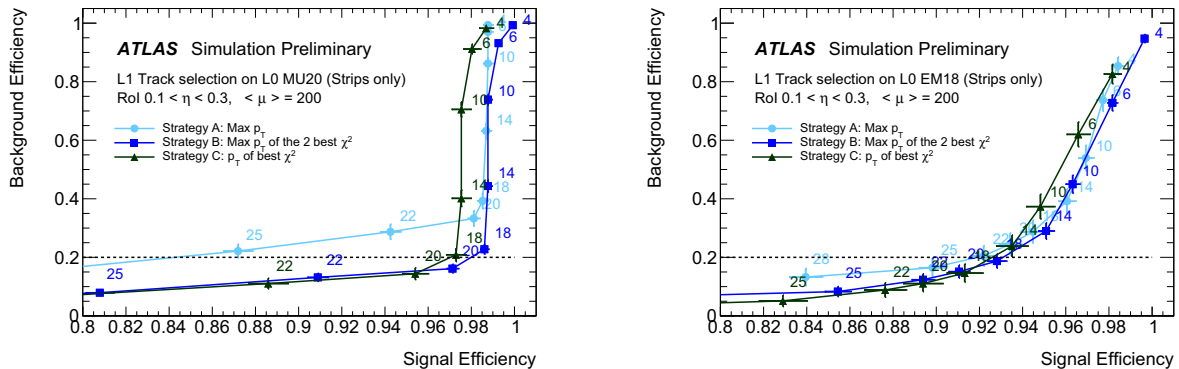


Figure 2. Signal vs background efficiencies for three track selection strategies as functions of a track p_T cut in the region of interest $0.1 < \eta < 0.3$, $0.3 < \phi < 0.5$. The signal is composed of single muons (left) and single electrons (right). The backgrounds are semi-leptonically decaying b-jets weighted to the expected p_T spectra of events firing the L0 MU20 (left) and EM18 (right) triggers and overlaid with a pile-up of $\langle \mu \rangle = 200$. The number next to each marker signifies the p_T cut applied to the track candidates resulting from the L1Track fit, the candidate was selected either by highest p_T (light blue), highest p_T of the two candidates with best χ^2 (dark blue) or the candidate with the best χ^2 (black).[5]

4. Latency of Detector Readout

The proposed Level 1 Track trigger will have to act within a short latency budget, expected to be approximately $15 \mu\text{s}$, so requires fast data collection and fast processing. A discrete event simulation has been developed to simulate the data flow out of the upgraded inner tracker readout to determine the viability of different trigger scenarios. The latency of the pattern matching and track fitting have not been simulated as they are very dependent on the exact

hardware choices arrived at but is not expected to be a limiting factor. It is expected that the AM input capacity will be ~ 200 MHz and the FPGAs will be capable of performing 4 track fits per ns which means that the two processes will take approximately $2\mu\text{s}$ each for the highest occupancy events.

As described in Section 2, a maximum of 10% of inner detector clusters are marked as “Priority” so that this data can “skip the queue” and arrive at the Level 1 Track trigger faster. This is performed in the discrete event simulation, as shown for the full maps of prioritised and non-prioritised latency in Figure 3. It has been found that the prioritised data can all be read out safely within a rough limit of $6\mu\text{s}$ for a total readout rate of 1 MHz. There is little cost to the latency of the non-prioritised data by introducing this prioritisation scheme.

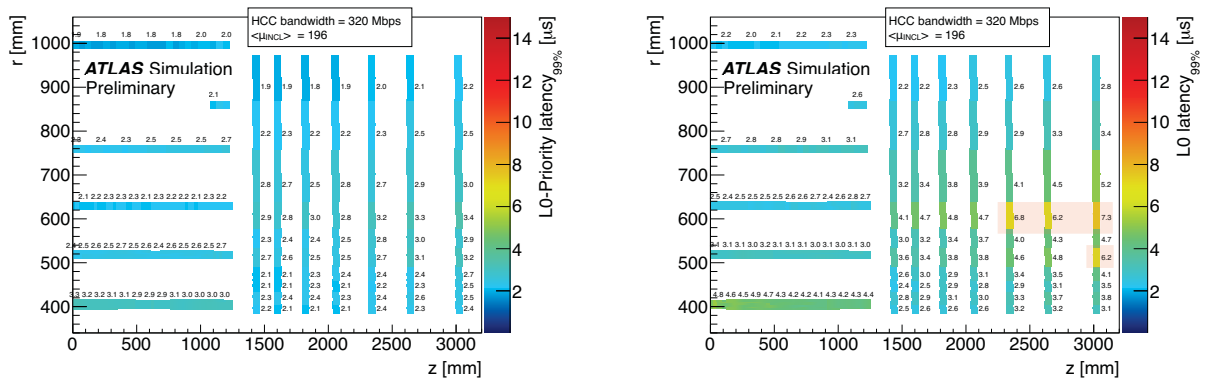


Figure 3. Detector maps showing the latency within which 99% of prioritised (left) and non-prioritised data can be read out after a request for an instantaneous luminosity of $\sim 7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with a total readout rate of 1 MHz. The latencies are estimated with the L1Track discrete event simulation.[5]

5. Conclusions

The challenging environment of the high luminosity LHC will require the ATLAS trigger to be re-designed to avoid a large increase of the single lepton p_T thresholds. A hardware-based Level 1 Track trigger operating within a tight latency budget has the potential to reduce trigger rates while providing high signal efficiency and good parameter resolution. A system using pattern matching and linearised track fitting has been shown, through simulation, to be suitable for this task. A configuration involving only strip layers is sufficient for pattern matching and track fitting efficiency, above 99% for single muons, but is improved upon in the area of parameter resolution through the inclusion of a pixel layer. The exact hardware configuration has not yet been determined but it appears feasible to build such a system using FPGAs and Associative Memory ASICs.

References

- [1] The ATLAS Collaboration 2008 *JINST* **3** S08003
- [2] Evans L and Bryant P 2008 *JINST* **3** S08001
- [3] The ATLAS Collaboration 2012 *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment* CERN–LHCC–2012–022
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- [5] The ATLAS Collaboration 2016 Approved plots for the L1Track Trigger project <https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L1TrackPublicResults>