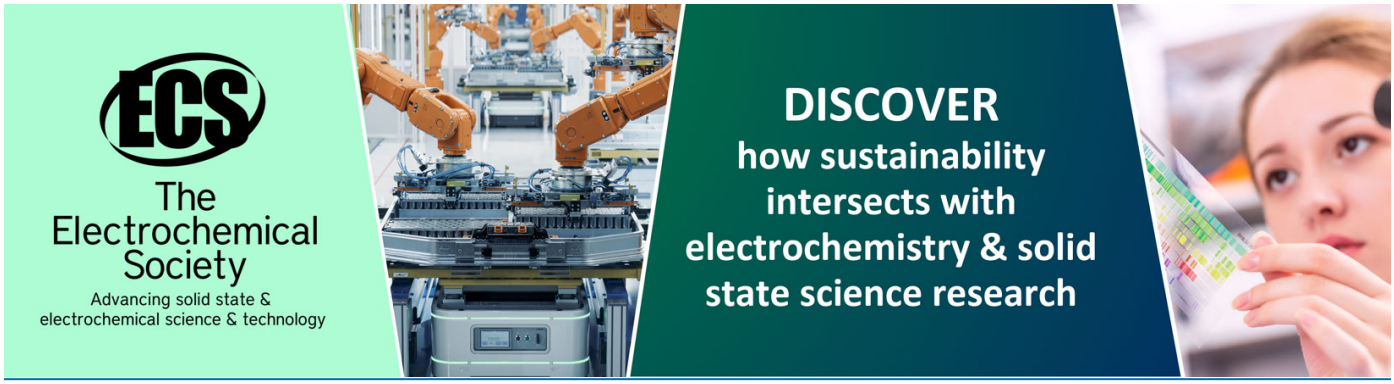
Model Based Optimization of Integrated Low Voltage DC-DC Converter for Energy Harvesting Applications



Model Based Optimization of Integrated Low Voltage DC-DC Converter for Energy Harvesting Applications

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Abstract. A novel model based methodology is presented to determine optimal device parameters for the fully integrated ultra low voltage DC-DC converter for energy harvesting applications. The proposed model feasibly contributes to determine the maximum efficient number of charge pump stages to fulfill the voltage requirement of the energy harvester application. The proposed DC-DC converter based power consumption model enables the analytical derivation of the charge pump efficiency when utilized simultaneously with the known LC tank oscillator behavior under resonant conditions, and voltage step up characteristics of the cross-coupled charge pump topology. The verification of the model has been done using a circuit simulator. The optimized system through the established model achieves more than 40% maximum efficiency yielding 0.45 V output with single stage, 0.75 V output with two stages, and 0.9 V with three stages for 2.5 kΩ, 3.5 kΩ and 5 kΩ loads respectively using 0.2 V input.

1. Introduction

The continuous urban growth with sustainable development thrust demands low cost, low power electronics with small footprint for wireless sensor networks. Low voltage output (around 0.2 V) from thermoelectric or small photovoltaic energy harvesters utilized in such applications needs to be stepped up to support small loads. Researchers proposed several DC-DC step-up circuit topologies and stratergies to improve the conversion efficiency. Body biasing technique proposed by [1] and [2] required an additional power supply and resulted in losses from added wiring. Tanzava [3] modelled the effect of resistance on switching devices in an effort to optimize performance, which guided further developments of such models. The equivalent half circuit model presented by [4] and [5] is limited to the Dickson [6] charge pump topology, and does not extend to more recent designs. An integrated LC tank was proposed as a good alternative to traditional charge-pump clock generators in our previous work [7] for reduced losses. The LC tank half circuit model proposed by [8] and [9] investigates characteristics of such circuits in VCOs. Recent papers [10, 11] present optimization models for the charge pump design, but without linking these to the VCO efficiency. This paper reports a novel model based methodology to determine the optimal device parameters for the full DC-

DC converter [7] in Figure 1 with varying charge pump stages, depending on the required output voltage range for a given load.

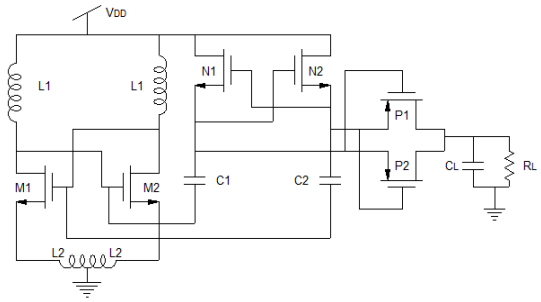

Figure 1. Single stage cross-coupled DC-DC converter with LC tank based oscillator.

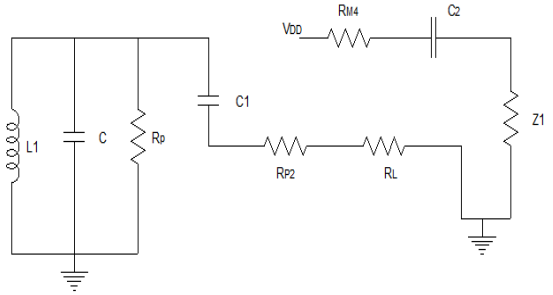

Figure 2. Equivalent half circuit model for Single stage DC-DC converter.

2. DC-DC converter model

The lumped element half circuit for the LC tank based oscillator, shown in Figure 2, consists of the parallel identical inductor (*L1*), capacitor (*C*) and resistor (R_p). The parallel capacitance necessary to sustain oscillation in the LC tank is provided by the switching NMOS (*M1* and *M2* in Figure 1) gate. Charge pump MOSFETs (*N1*, *N2*, *P1*, *P2*) in Figure 1 are modeled using series resistors. MOSFET characteristics have been extracted from the simulation using the target 180nm CMOS process under operation conditions as depicted in Figure 3 and 4 for gate capacitance and resistance respectively.

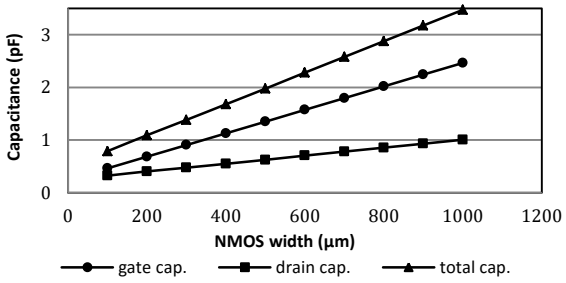

Figure 3. The variation of the NMOS capacitance with MOSFET width, W (length, L=240 nm).

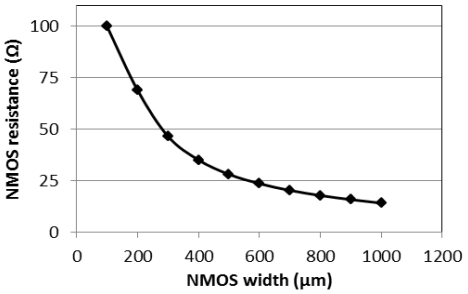

Figure 4. The variation of the NMOS resistance with MOSFET W (L=240 nm).

Equation 1 provides the power output for the single stage DC-DC converter based on the lumped power consumption model. This enables the analytical derivation of the charge pump efficiency when utilized simultaneously with the known LC tank oscillator behavior under resonant conditions, and voltage step-up characteristics of the cross-coupled charge pump topology. The extended equations for two, three, and more stages are not shown here for brevity.

$$P_{out} = \left(\frac{2V_{DD}\, e^{\frac{-t}{C_1(R_L+R_{P2})}} + V_0}{R_L + R_{P2}} \right)^2 \times e^{\frac{-2t}{C_1(R_L+R_{P2})}} \times R_L \,, \tag{1}$$

where, V_0 is a constant (voltage across the *C1* capacitor), t is the half period of the clock signal. V_{DD}, R_{R2} and R_L are input voltage, charge pump NMOS resistance and load resistance respectively. Equation 2 provides an analytical model for the total power in the single stage DC-DC converter, which mainly consists of the switching power consumption in the LC tank, switching power consumption due to the charge pump capacitors, and the power output.

$$P_{total} = P_{out} + V_{rms}^2 \left(\frac{1}{R_p} + \sqrt{{}^{C}/_{L1}} \quad (1 + {}^{1}/_{2\pi}) \right) + 2C_1 V_{rms}^2 \sqrt{{}^{C}/_{2\pi L1}} \,. \tag{2}$$

Relationship of LC tank capacitance to inductance ($L1$), series (R_S) and parallel (R_P) resistances is as shown in Equation 3. Equation 4 and 5 provide fitted models for Figure 3 and Figure 4 respectively.

$$C = L1/(R_P R_S)\,, \tag{3}$$

$$C = 0.003x + 0.4912\,, \tag{4}$$

$$R_N = 3 \times 10^{-10}x^4 - 9 \times 10^{-7}x^4 + 0.001x^2 - 0.5757x + 148.33\,, \tag{5}$$

where, x is the NMOS width in μm and C is the NMOS capacitance in pF. R_N is the NMOS drain-to-source ohmic resistance.

3. Optimization methodology

The area of the on-die inductors is a critical parameter in the optimization process. The first step is to select the maximum possible size of drain inductors ($L1$), and set the source inductors at least 10% of the drain inductors (the purpose of the source inductors is oscillation with 50% duty cycle [7]). LC tank capacitance for the desired average oscillator load range R_P is calculated using Equation 3, and LC tank NMOS size is then determined from Equation 4. The NMOS and PMOS sizes in the charge pump are balanced, based on technology characteristics, to set $R_{Pl} = R_N$. Next, $R_{Pl}+R_L = R_L$ ($R_{pl} \ll R_L$) is substituted into equation $\frac{dP_{out}}{dC} = 1$ to calculate the optimum charge pump capacitance for the maximum output power. Similarly, input-to-output power transfer efficiency equation can be used to determine the optimal capacitance for the maximum efficiency, since the main losses are modelled in the equations in Section 2. The optimized capacitor value can then be substituted into Equation 1 to calculate the corresponding PMOS resistance (R_{Pl}), which is converted to the device size using the characteristic curves in the chosen technology. Similarly, models with two or more charge-pump stages can be used to determine the optimal parameters for the corresponding stages, and also the minimum number of stages to fullfil the required power/voltage output with maximum efficiency.

4. Results and conclusion

The simulated LC tank power consumption is depicted in Figure 5 along with the model results. The power efficiency curves for one- and three-stage DC-DC converter are depicted in Figure 6, as example, for varying L1 inductor sizes. Figure 7 depicts the output power variation of an optimized converter with the load resistance for different number of stages. The optimized system through the established model achieves more than 40% maximum efficiency yielding 0.45 V output with single stage, 0.75 V output with two stages, and 0.9 V output with three stages for 2.5 kΩ, 3.5 kΩ, and 5 kΩ loads respectively using 0.2 V input. The optimizations presented results in efficiency improvement of more than 50% for the unlimited input power scenario with unregulated output, as compared to the alternatives [7], [12].

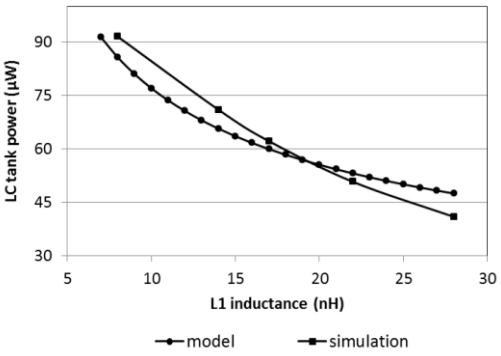

Figure 5. LC tank oscillator power consumption vs. L1 inductance.

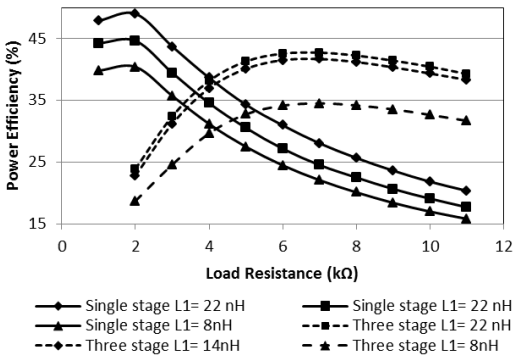

Figure 6. Converter power efficiency vs. load resistance and L1 size for 1 & 3 stages.

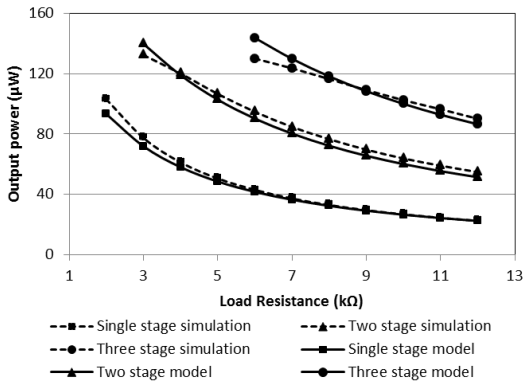

Figure 7. The variation of converter output power with load resistance for 1-3 stages.

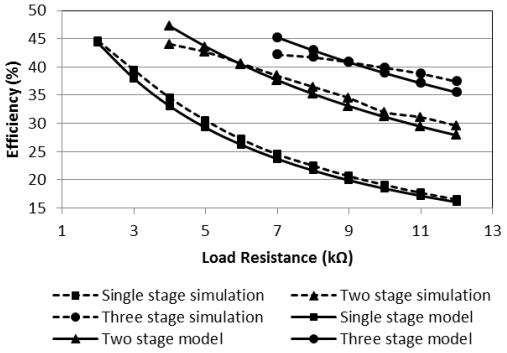

Figure 8. The variation of converter efficiency with load resistance for 1-3 stages.

The developed model can be utilized for circuit optimization in a variety of energy harvesting scenarios. Die area is a primary design constraint for fully integrated (low cost) solutions. After determining the application requirements including input power capacity, load voltage and power targets, either efficiency or output power can be optimized using the provided method.

5. References

[1] Kim J, Mok P K T and Kim C 2014 23.1 A 0.15V-input energy-harvesting charge pump with switching body biasing and adaptive dead-time for efficiency improvement *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.* **57** 394–5

[2] Chen P H, Ishida K, Zhang X, Okuma Y, Ryu Y, Takamiya M and Sakurai T 2010 0.18-V input charge pump with forward body biasing in startup circuit using 65nm CMOS *Proc. Cust. Integr. Circuits Conf.* 2–5

[3] Tanzawa T 2011 A switch-resistance-aware dickson charge pump model for optimizing clock frequency *IEEE Trans. Circuits Syst. II Express Briefs* **58** 336–40

[4] Tanzawa T and Tanaka T 1997 A dynamic analysis of the Dickson charge pump circuit *IEEE J. Solid-State Circuits* **32** 1231–40

[5] Witters J S, Groeseneken G and Maes H E 1989 Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits *IEEE J. Solid-State Circuits* **24** 1372–80

[6] Dickson J F 1976 On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique *IEEE J. Solid-State Circuits* **11** 374–8

[7] Jayaweera HM, Pathirana WP, Muhtaroğlu A 2015 Fully Integrated Ultra-Low Voltage Step-up Converter with Voltage Doubling LC- Tank for Energy Harvesting Applications *Journal of Physics: Conference Series* **660** 012017

[8] Kwok K and Luong H C 2005 Ultra-low-voltage high-performance CMOS VCOs using transformer feedback *IEEE J. Solid-State Circuits* **40** 652–60

[9] Hsieh H, Member S and Lu L 2007 A High-Performance CMOS Voltage-Controlled **55** 467–73

[10] Tanzawa T 2015 A comprehensive optimization methodology for designing charge pump voltage multipliers *Proc. - IEEE Int. Symp. Circuits Syst.* **2015**–**July** 1358–61

[11] Cabrini A, Gregori S and Torelli G 2016 Integrated charge pumps : a generalised method for power efficiency optimisation **10** 12–9

[12] Bassi G, Colalongo L, Richelli A and Kovacs-Vajna Z 2012 A 150 mV-1.2 V fully-integrated DC-DC converter for Thermal Energy Harvesting *Int. Symp. Power Electron. Electr. Drives, Autom. Motion* 331–4