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D V Shuleiko[1] and A S Ilin[1,2]

[1]Faculty of Physics, Lomonosov Moscow State University, 1/2 Leninskie Gory, Moscow, 119991, Russia

[2]National Research Centre "Kurchatov Institute", 1 Kurchatov Sq., Moscow, 123182, Russia

Abstract

Photoluminescence and electrical properties of superlattices with thin (1 to 5 nm) alternating silicon-rich silicon oxide or silicon-rich silicon nitride, and silicon oxide or silicon nitride layers containing silicon nanocrystals prepared by plasma-enhanced chemical vapor deposition with subsequent annealing were investigated. The entirely silicon oxide based superlattices demonstrated photoluminescence peak shift due to quantum confinement effect. Electrical measurements showed the hysteresis effect in the vicinity of zero voltage due to structural features of the superlattices from $SiO_{0.93}/Si_3N_4$ and $SiN_{0.8}/Si_3N_4$ layers. The entirely silicon nitride based samples demonstrated resistive switching effect, comprising an abrupt conductivity change at about 5 to 6 V with current-voltage characteristic hysteresis. The samples also demonstrated efficient photoluminescence with maximum at ~1.4 eV, due to exiton recombination in silicon nanocrystals.

1. Introduction

Current nanostructuring methods provide an opportunity for controllable varying of optical and electrical properties of siliceous films, by forming areas with silicon nanocrystals in the bulk of the film. These structures can be used to produce new types of photovoltaic and optoelectronic devices, such as all-silicon light emitting devices and third-generation tandem solar cells [1]. Moreover, silicon oxide-based films [2, 3] or silicon nitride-based films [4] with silicon nanocrystals can be used to produce logical elements based on memristive effect [5] (the dependence of the circuit element conductivity on the current passed). For practical applications in all cases precise control of the shape, size and concentration of silicon nanocrystals is required.

Silicon nanocrystals embedded in siliceous films can be produced by several techniques such as chemical vapor deposition (CVD) [6], reactive evaporation [7], and magnetron sputtering [8]. Control over all three parameters mentioned above (size, density, spherical shape) can be achieved by depositing layers with alternating material stoichiometry by plasma-enhanced chemical vapor deposition (PECVD) with subsequent high temperature annealing [6, 9]. In this case silicon-rich oxide or nitride layers with thickness of several nanometers are separated with barrier layers of stoichiometric silicon oxide or silicon nitride. These barrier layers effectively constrain the growth of quasi-ordered silicon nanocrystal arrays within the silicon-rich layers during thermal annealing [9, 10].

The purpose of this work is an investigation of nonlinear electrical properties of such silicon nanocrystal arrays in the silicon oxide and silicon nitride superlatices, as these structures may

potentially find application in microelectronics, and detailed study of such structures electrical properties has not been yet carried out. Photoluminescence (PL) properties of the superlattices also were examined to confirm the formation of silicon nanocrystals.

2. Experiment

2.1 Sample fabrication

The superlattices consisting of 20 pairs of thin (1 to 5 nm) alternating $SiO_{0.93}$ or $SiN_{0.8}$, and SiO_2 or Si_3N_4 layers (40 layers in total) were deposited by plasma-enhanced chemical vapor deposition. The samples were deposited at n-type Si substrate with crystallographic surface orientation (100). High temperature annealing during 1 hour at 1150 °C in nitrogen atmosphere caused nanocrystal formation in the silicon-rich layers. Three series of the samples were fabricated: consisting of alternating $SiO_{0.93}/SiO_2$ (SO series), $SiO_{0.93}/Si_3N_4$ (SO/SN series) and $SiN_{0.8}/Si_3N_4$ (SN series) layers. A more detailed description of the sample preparation procedure can be found in works [10, 11]. The samples properties are given in table 1.

Table 1. Structural parameters of the samples.

Sample name	Silicon-rich layer (with nanocrystals)		Barrier layer	
	Material	Thickness (nm)	Material	Thickness (nm)
SO-1	$SiO_{0.93}$	1.5	SiO_2	1
SO-2		3		
SO-3		5		
SO/SN-1		1.5	Si_3N_4	1.5
SO/SN-2		3		
SO/SN-3		5		
SN-1	$SiN_{0.8}$	1.5		
SN-2		3		
SN-3		5		

2.2 Optical measurements

The PL spectra were measured at room temperature using a spectral complex based on the monochromator/spectrograph SOLAR TII MS3504i, which allows to record spectra in the visible and near-infrared (up to 1100 nm) range with CCD digital camera Proscan HS 101H. A HeCd laser with 325 nm wavelength in pulsed mode was used as the excitation source. Output power was 30 mW.

2.3 Electrical measurements

To measure the current-voltage characteristics (CVC), the aluminum contacts were deposited. One common contact was deposited on the entire bottom surface of the substrate, and the group of contacts with 600 μm diameter was deposited on the top of the superlattice. During the measurements the voltage was applied between the common bottom contact, and one of the top contacts.

CVC were measured using picoammeter Keithley 6487. During the measurements voltage was applied cyclically: at first positive bias from 0 to +10 V and back to 0 V was applied to the top contact and then negative bias from 0V to –10V and back to 0 V was applied. Measurement step was 0.2 V and frequency was 1 measurement per second. To control the reproducibility, the measurements were carried out on several contacts for each sample.

3. Experimental results and discussion

According to the measurements carried out, the superlattices possess nonlinear CVCs due to potential barriers between the superlattice layers, at the silicon nanocrystal surfaces, as well as on the film-substrate and film-contact interfaces. All the samples also possess effective PL.

3.1 PL properties

The PL spectra of the samples from SO series are presented in figure 1. Maximum of PL was observed at 1.40 eV for SO-1, 1.50 eV for SO-2 and 1.63 eV for SO-3. The PL reason in this spectral range can only be exciton recombination in the silicon nanocrystals [9]. The PL peak shift can be explained by the quantum confinement effect in the silicon nanocrystals. Due to the quantum confinement effect, the size of the nanocrystals can be evaluated using calibration graph from [12], or the equation:

$$E_{gap}(D) = E_{gap}(\infty) + \frac{2\hbar^2\xi_{n,l}^2}{m_r D^2} = E_{gap}(\infty) + \frac{A}{D^2} \quad (1)$$

where $E_{gap}(D)$ – band gap in silicon nanocrystal with diameter D, $E_{gap}(\infty)$ – band gap in bulk Si, $\xi_{n,l}^2$ – Bessel spherical function root of half-integer argument l+1/2 (l=0,1,2…); for l = 0, $\xi = \pi n$ (n=1,2,3...). The second term in the equation can be simplified using constant for spherical nanocrystals in the strong confinement mode A=3.57 eV·nm^2 [13]. Calculated silicon nanocrystal sizes are in a good agreement with Si-rich layers thickness in the superlattices (Table 2). Minimal crystallization diameter expected in previous works was 1.8 nm [10], hence in 1.5 nm Si-rich layers silicon nanocrystals are formed with larger diameter for all structures.

Maximum of PL was observed at approximately 1.40 eV for all samples from SO/SN and SN series also. The PL reason is a same exiton recombination in the silicon nanocrystals correspondingly. However, the PL peak shift absent in these cases. Therefore, there is no silicon nanocrystal size control effect in the superlattices with Si_3N_4 barrier layers.

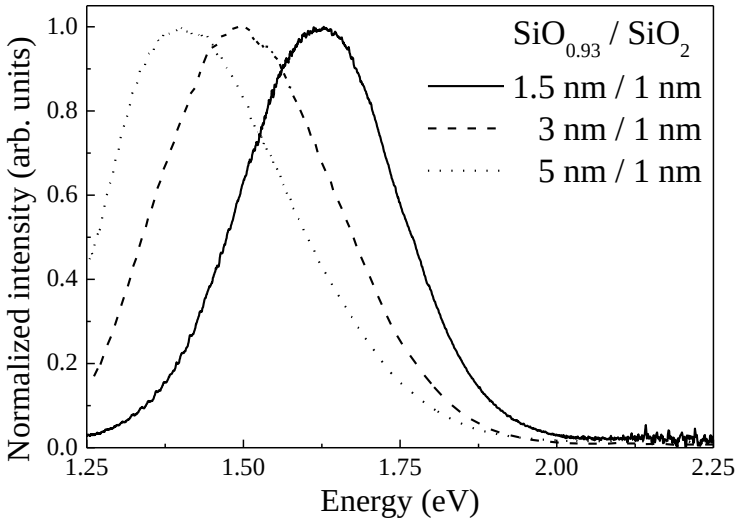

Figure 1. PL spectra of the $SiO_{0.93}/SiO_2$ superlattices.

Table 2. Silicon nanocrystal size compared to thickness of Si-rich layers in the superlattice

Sample name	Thickness of the layers with nanocrystals (nm)	Silicon nanocrystals mean size calculated using:	
		Calibration graph [12] (nm)	Equation (1) (nm)
SO-1	1.5	2.0	2.6
SO-2	3	3.0	3.1
SO-3	5	4.5	3.6

3.2 Current-voltage characteristic hysteresis at zero voltage

For all samples of the SO/SN and SN series, a symmetrical CVC hysteresis effect at 0 V was observed. Figure 2 shows the CVC of the sample SO/SN-1 compared to the CVC of a 100 GΩ test impedance. This comparison confirms that the observed effect is not associated with the capacity of the experimental setup parts. It should also be noted that the hysteresis effect at 0 V was not observed in the SO series as the samples from SO series have resistance by 2 orders of magnitude higher

compared to the samples from other series. And as will be shown below, the resistance of the multilayer structure is important in the explanation of the observed hysteresis.

The effect of hysteresis can be explained by the relatively high capacity of the superlattices constituting a structure of alternating layers with different dielectric constants. This structure can be considered as serially connected flat capacitors that cause charge retention with certain impedance. Thus the equivalent circuit can be represented with parallel-connected resistor and capacitor, and is characterized by charge relaxation time $\tau = RC_\Sigma$. The capacity of each layer is

$$C_i = \frac{\varepsilon\varepsilon_0 S}{d}, \quad (2)$$

where S – capacitor plate area, d – layer thickness, ε – dielectric constant of the material layer. The table values $\varepsilon(SiO_{0.93}) = 4.8$, $\varepsilon(Si_3N_4) = 9$ were used. The total capacity C_Σ of the samples from SO/SN series is calculated by the formula for the series-connected capacitors:

$$C_\Sigma = \left(\sum_{i=1}^{40}\left(\frac{1}{C_i}\right)\right)^{-1}, \quad (3)$$

where 40 is the total number of layers.

The resistance R of the samples at $U = 1$ V, and the relaxation time $\tau = RC_\Sigma$ were calculated using the experimentally measured CVC. The data are given in table 3. Also, time-resolved charge relaxation of the superlattices from the SO/SN series was measured. Charge relaxation behavior of the structures is biexponential: figure 3 shows electric current relaxation for the sample SO/SN-3 and its approximation. Measured decay times are also presented in table 3.

Table 3. Resistance, capacity and charge relaxation time for the sampler from SO/SN series

Sample name	Resistance R at U=1V (GΩ)	Capacity C_Σ (pF)	Relaxation time τ=RC (s)	Experimental relaxation time	
				τ_1 (s)	τ_2 (s)
SO/SN-1	58	260	15	6.7±1.9	0.9±0.5
SO/SN-2	24	160	4	6.0±0.6	0.8±0.1
SO/SN-3	88	100	9	7.8±0.7	1.0±0.1

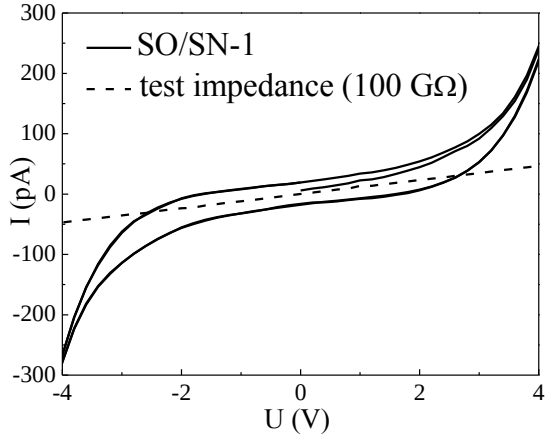

Figure 2. CVC hysteresis of the SO/SN-1 superlattice compared to test impedance

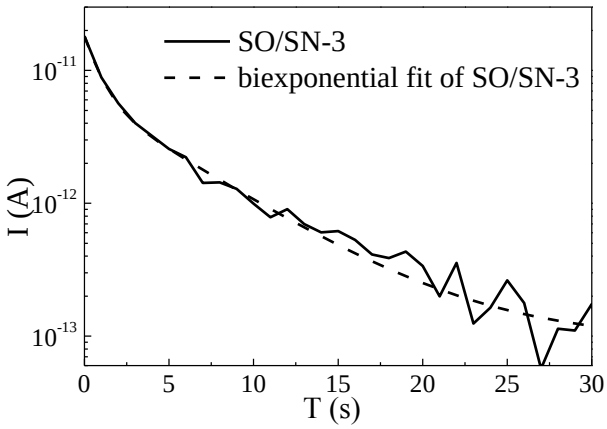

Figure 3. Electrical current relaxation in the sample SO/SN-3

The binexponential nature of charge relaxation can be attributed to presence of the silicon nanocrystals in the volume of the superlattice, and in the model used above these nanocrystals were not taken into account (see below). Thus capacity of the interfaces between matrix and nanocrystal should be taken into account [14]. Also, the contact–superlattice and superlattice–substrate interfaces

can contribute to the sample capacity. It is also important to note that the presence of the silicon nanocrystals leads to a change in the dielectric constant of the layers.

In addition, silicon nanocrystals embedded in the dielectric matrix should be considered as quantum dots (QDs) with discrete electron spectrum, separated by potential barriers. The arrays of coupled QDs can accumulate electrons by trapping them, and current flow in such system occurs by electron tunneling. Electron tunneling is governed by the Coulomb interaction between localized electrons and is highly dependent on the morphology of the QDs (size, shape and spacing). The QDs morphology determines the energy level intervals and transition rates of electrons between the QDs [15]. Similar effect of charge retention due to accumulation of electrons into the silicon nanocrystals that act as QDs was observed in [16]. In that work charge retention occurred in the silicon nitride films with silicon nanocrystals, with relaxation time of several hundred of microseconds.

As biexponential charge relaxation behavior was observed in our work, the presence of an additional charge relaxation channel can be assumed; and this channel is most likely associated with electron tunneling between the silicon nanocrystals acting as QDs. Due to the presence of such supplemental channel the relaxation rate in the initial stage is fast, while the amount of electrons trapped on silicon QDs is large.

3.3 Resistive switching with hysteresis (memristive effect)

Resistive switching effect, comprising the abrupt conductivity change with CVC hysteresis was demonstrated by the sample SN-2. At the voltage of 5 to 6 V, the conductivity increased by almost two orders of magnitude (Figure 4). The sample withstood at least 10 measurement cycles without substantial change in the switching parameters. This hysteresis effect is similar to the memristive switching observed in SiO_2 films containing silicon nanocrystals [2, 3] or Si_3N_4 films with thickness of 4 to 13 nm [4]. However, the hysteresis effect was observed only at positive voltage bias, and no hysteresis was observed at negative bias.

This conductivity switching most likely occurs due to formation of silicon filaments in the matrix between the nanocrystals [2–4]. In the low conductivity ("off") state electrons are trapped in the silicon nanocrystals and conductive path is formed by electron tunneling between the nanocrystals. At certain voltage (from 5 to 6 V) a conductive path is formed from the silicon filaments in the spaces between the silicon nanocrystals due to nitride ion migration or generation of nitride vacancies [4] by current-induced heating [3]. The local current density in the regions between closely spaced nanocrystals is higher than in the surrounding matrix, and current-induced local heating is sufficient for such structural changes and formation of silicon filaments. When conductive path is formed, the sample is switched into high conductivity state ("on").

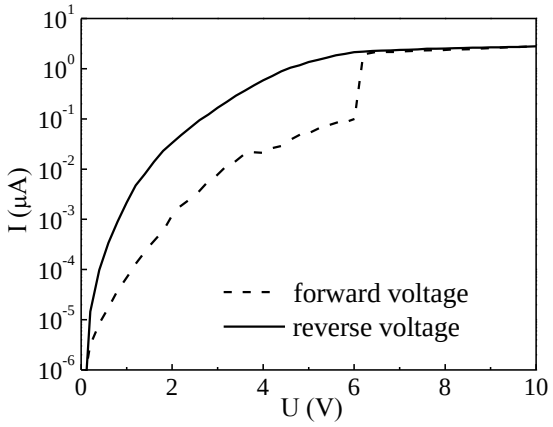

Figure 4. Current-voltage characteristic of the sample SN-2.

An important feature of the observed resistive switching is distinct CVC hysteresis at the switching voltage, formed by CVC curves of the sample in the "off" and "on" states (Figure 4). The hysteresis occurs due to the fact that after the conductive path of silicon filaments is formed, it exists as long as the electric current flows, and degrades after the voltage is turned off.

4. Conclusions

The silicon oxide and silicon nitride superlattices with embedded silicon nanocrystals demonstrate PL properties in the red and near-infrared band. PL maximum was observed at ~1.4 eV for all $SiO_{0.93}/Si_3N_4$ and $SiN_{0.8}/Si_3N_4$ samples while PL peak position for $SiO_{0.93}/SiO_2$ samples depended on size of the nanocrystals and shifted from 1.40 to 1.63 eV. For all samples from SO/SN and SN series PL maximum was observed at approximately 1.40 eV and had no shift.

Superlattices of $SiO_{0.93}/Si_3N_4$ and $SiN_{0.8}/Si_3N_4$ layers, demonstrated current-voltage characteristics hysteresis at zero voltage. This effect is most likely due to resistive and capacitive parameters of the structures representing a multilayer RC circuit, as well as presence of silicon nanocrystals acting as QDs in the bulk of the superlattice.

The memristive effect was detected in the $SiN_{0.8}/Si_3N_4$ superlattice with silicon nanocrystals. The conductivity abruptly increased by almost two orders of magnitude at 5 to 6 V during forward voltage sweep, followed by CVC hysteresis with a smooth voltage decrease at reverse voltage sweep. This effect is most likely associated with silicon filament formation between silicon nanocrystals at switching voltage and gradual degradation of the filaments after the voltage is turned off.

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References

[1] Cheng K–Yu, Anthony R, Kortshagen U R and Holmes R J 2011 *Nano Lett.*, **11(5)** 1952; Green M A 2001 *Prog. Photovoltaics* **9** 123
[2] Yao J, Sun Z, Zhong L, Natelson D and Tour J M 2010 *Nano Lett.* **10** 4105
[3] Wang Y, Chen Y–T, Xue F, Zhou F, Chang Y–F, Fowler B and Lee J C 2012 *Appl. Phys. Lett.* **100** 083502
[4] Kim H–D, An H–M, Hong S M and Kim T G 2013 *Phys. Status Solidi* A **210(9)** 1822
[5] Strukov D B, Snider G S, Stewart D R and Williams R S 2008 *Nature* **453** 80
[6] Creazzo T, Redding B, Marchena E, Murakowski J and Prather D W 2010 *J. Lumin.* **130** 631
[7] Cheylan S, Elliman R G, Gaff K and Durandet A 2001 *Appl. Phys. Lett.* **78** 1670
[8] So Y–H, Huang S, Conibeer G and Green M A 2011 *Thin Solid Films*, **519** 5408
[9] Zacharias M, Heitmann J, Scholz R, Kahler U, Schmidt M and Blaesing J 2002 *Appl. Phys. Lett.* **80** 661
[10] Zelenina A, Dyakov S A, Hiller D, Gutsch S, Trouillet V, Bruns M, Mirabella S, Löper P, López–Conesa L, López–Vidrier J, Estradé S, Peiró F, Garrido B, Bläsing J, Krost A, Zhigunov D M and Zacharias M 2013 *J. Appl. Phys*. **114** 184311
[11] Zelenina A, Sarikov A, Zhigunov D M, Weiss C, Zakharov N, Werner P, López–Conesa L, Estradé S, Peiró F, Dyakov S A and Zacharias M 2014 *J. Appl. Phys*. **115** 244304
[12] Takeoka S, Fujii M and Hayashi S 2000 *Phys. Rev.* B **62(24)** 16820
[13] Goncharova L V, Nguyen P H, Karner V L, D'Ortenzio R, Chaudhary S, Mokry C R and Simpson P J 2015 *J. Appl. Phys.* **118** 224302.
[14] Forsh F A, Martyshov M N, Timoshenko V Yu and Kashkarov P K 2006 *Semiconductors* **40(9)** 476
[15] Mantsevich V N, Maslova N S and Arseyev P I 2013 *Solid State Commun.* **168** 36
[16] Liao W, Zeng X, Wen X, Zheng W, Wen Y and Yao W 2015 *J. Electron. Mater*. **44(3)** 1015