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Planarization of Silicon Dioxide and Silicon Nitride Passivation Layers

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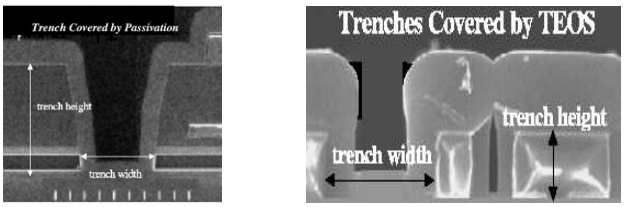
Abstract. Final passivation planarization is achieved by optimizing the stack height and trench width for technologies that are sensitive to passivation planarization like image sensor processes. Deposition profiles obtained by using our topography simulator ELSA (Enhanced Level Set Applications) predict a range of trench width, stack height, and the thickness of the deposited layers which lead to a sufficient planarization margin. Furthermore, these predictions enable design of trenches with a sufficient side wall and bottom coverage in order to guarantee a proper moisture seal.

1. Introduction

Planarized final passivation is required for technologies like image sensor processes. A typical passivation stack in IC chips is a layer of SiO_2 from PECVD (Plasma Enhanced Chemical Vapor Deposition) TEOS (Tetraethoxysilane) covered by a layer of PECVD Si_3N_4. Our objective is to achieve planarized passivation in the presence of deep trenches that serve as moisture barrier (cf. Figure 1a) or topmost metal topography (cf. Figure 1b). Planarization of a moisture seal Si_3N_4 layer can be achieved by optimizing the trench width and taking advantage of the PECVD breadloafing characteristic. Planarization of a TEOS process on top metal topography can be achieved by depositing a thick layer of silicon dioxide from TEOS, which then is planarized by



(a) (b)

Figure 1. Trenches covered by (a) passivation and (b) silicon dioxide from TEOS.

CMP (Chemical Mechanical Planarization) down to an optimized thickness. Such an optimization requires a topography simulator for predicting profiles of these deposition processes.

The topography simulator ELSA developed at our institute is based on a level set method [1] for tracking moving boundaries in two and three dimensions. ELSA is capable of handling different deposition and etching models and has been proven for different semiconductor manufacturing processes [2–5].

2. The geometrical parameters of investigations

The geometrical parameters considered for investigations are divided into two different sets. The first set consists of 45 cases for the deposition of silicon nitride with the following geometrical parameters D, H, and T (cf. Figure 2) that stand for trench width, trench height, and the thickness of the deposited layer, respectively:

- D = 0.5, 1.0, 2.0, 3.0, and 4.0μm
- H = 2.0, 3.0, and 4.0μm
- T = 0.3, 0.6, and 0.9μm

The second set consists of 63 cases for the deposition of silicon dioxide from TEOS with the following parameters:

- D = 0.3, 0.5, 0.8, 1.0, 1.4, 2.0, and 3.0μm
- H = 0.3, 0.5, and 0.9μm
- T = 0.3, 0.7, and 1μm

The process conditions of the deposition of silicon nitride and silicon dioxide were the same as those investigated in [2] and [3], respectively. Therefore, the parameters extracted during those two investigations are also used by our new investigations. The actual optimization has been performed using the optimization and calibration tool SIESTA (Simulation Environment for Semiconductor Technology Analysis) [6] developed at our institute.

3. The goals of simulations

The goals of the simulations are: First, optimizing the trench width such that after Si_3N_4 deposition and breadloafing, the trench top closes completely, while sufficient bottom and sidewall coverage is obtained. Second, assuming 1μm silicon dioxide is deposited from TEOS

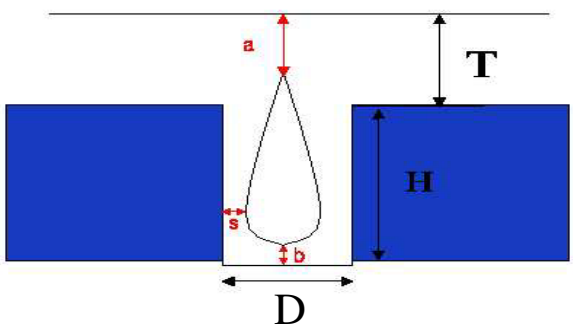


Figure 2. A schematic of a trench and its geometrical parameters. Parameters a, b, and s are used for the difference between the top of the void and the thickness of the deposited layer, bottom coverage, and sidewall coverage, respectively.

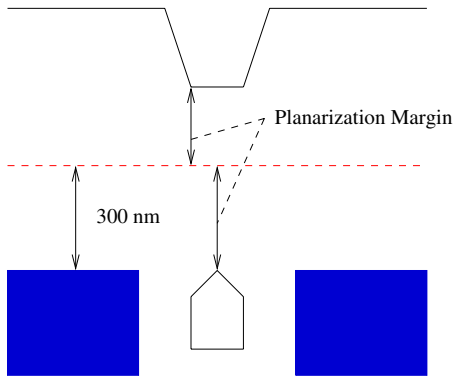


Figure 3. An illustrative description of planarization margin.

and polished down to 0.3μm, optimizing the trench width and height such that a sufficient planarization margin (cf. Figure 3) larger than the CMP process variation is obtained. In the following sections the simulation results are discussed.

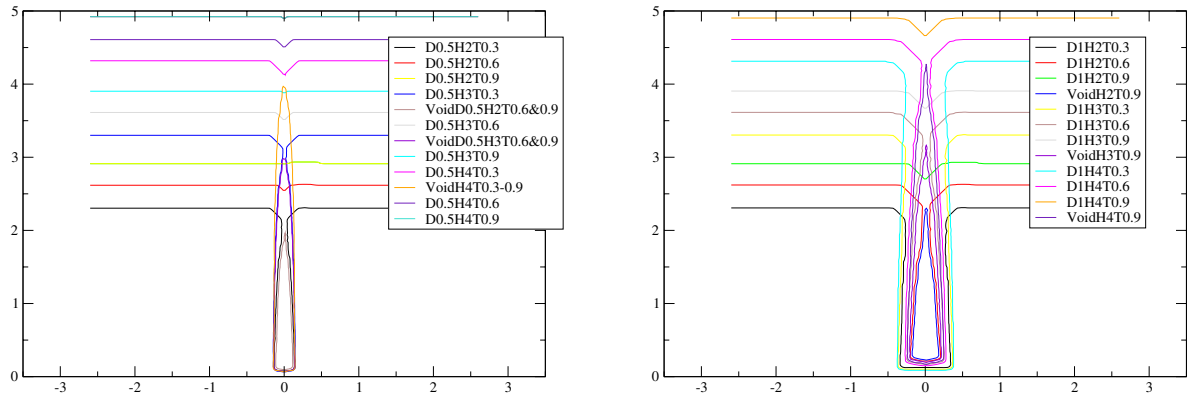
3.1. Results of silicon nitride deposition

Table 1 presents a part of the simulation results, namely, those of the deposition of silicon nitride into different trenches as shown for example in Figure 4 for D = 0.5μm and D = 1μm. The tabulated results can be summarized as follows:

- Narrowing down the trench to 1μm with the deposition of 0.9μm nitride results in a planarized topside and at least about 0.3μm of side wall and 0.17μm of bottom nitride coverages (cf. Table 1).

Table 1. Tabulated results for 0.5μm and 1μm wide trenches.

T(μm)	H(μm)	D(μm)	a(μm)	s(μm)	b(μm)
0.9	4	1	0.43	0.29	0.17
0.6	4	1	NA	0.29	0.17
0.3	4	1	NA	0.14	0.09
0.9	3	1	0.49	0.31	0.17
0.6	3	1	NA	0.31	0.17
0.3	3	1	NA	0.14	0.09
0.9	2	1	0.4	0.34	0.26
0.6	2	1	NA	0.34	0.26
0.3	2	1	NA	0.14	0.09
0.9	4	0.5	0.9	0.1665	0.06
0.6	4	0.5	0.57	0.1665	0.06
0.3	4	0.5	0.17	0.1665	0.06
0.9	3	0.5	0.9	0.1665	0.06
0.6	3	0.5	0.57	0.1665	0.06
0.3	3	0.5	NA	0.1665	0.06
0.9	2	0.5	0.9	0.18	0.11
0.6	2	0.5	0.57	0.18	0.11
0.3	2	0.5	NA	0.18	0.11



(a) (b)

Figure 4. The deposition of silicon nitride into trenches of (a) D = 0.5μm and (b) D = 1μm.

- Narrowing down the trench to 0.5μm with a thin nitride thickness of 0.6μm results in a planar topside with at least 0.1665μm of side wall and 0.06μm of bottom nitride coverages. Thinning down nitride to 0.3μm does not result in a planar topside where the stack height is 2μm and 3μm, respectively.

Finally, we can draw the following conclusions from the simulation results:

- A planar passivation with complete nitride sealed die edge is possible. A 1μm or lower trench width is required.
- When the trench width is reduced to 0.5μm, the topside nitride thickness can be reduced to 0.6μm, which, however, could raise reliability issues.

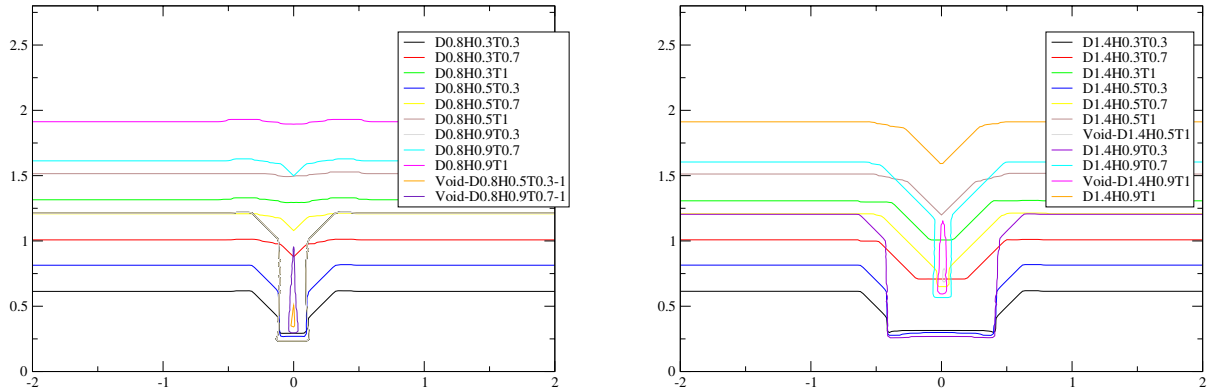
3.2. Results of silicon dioxide deposition

Figure 5 shows two of 63 simulations as listed in Section 2. Based on the simulation results the planarization margins for different trench widths and heights have been calculated as shown in Figure 6. The results can be summarized as follows:

- Varying the trench width does not allow voids to be completely eliminated.
- Void formation is a strong function of trench width and height. Voids are either already formed with deposition of 0.3μm silicon dioxide from TEOS or they will be formed as more oxide is deposited. Therefore, increasing the oxide thickness does not influence the void formation.
- By polishing down from 1μm to 0.3μm TEOS:
  - 0.3μm trench height provides sufficient planarization margin regardless of trench width (cf. Figure 6).
  - 0.5μm and 0.9μm trench heights lead to a non-planar surface either by opening up voids or by incomplete removal of the dimple at spaces > 1μm (cf. Figure 6).

4. Conclusion

State of the art topography simulator was employed for deposition processes. Deposition simulation was used to optimize the features which cause non-planar final passivation deposition



(a) (b)

Figure 5. The deposition of silicon dioxide into trenches of (a) D = 0.8μm and (b) D = 1.4μm.

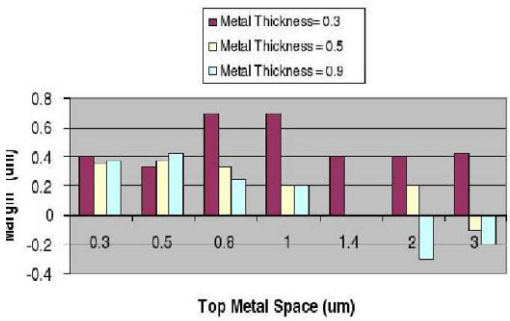


Figure 6. Planarization margin calculated for different widths and thicknesses.

such as trenches and topmost metal topography. One set of simulations was used to determine the moisture seal trench width that results in a planar silicon nitride surface while maintaining sufficient bottom and side wall coverage. Another set of simulations was used to optimize trench width and height in order to provide sufficient planarization margin for the deposition of oxide from TEOS followed by CMP.

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