R&D for a highly granular silicon tungsten electromagnetic calorimeter

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Abstract. This article reports on first experience with the technological prototype of a highly-granular silicon-tungsten electromagnetic calorimeter as envisaged for the detectors at a future lepton collider. In the focus of the analysis is the performance of a highly integrated Application Specific Integrated Circuit designed to meet the requirements in terms of dynamic range, compactness and power consumption. The beam test results show that the circuit will allow a future detector with a signal over noise ratio of at least 10:1. To minimise the power dissipation the ASIC will be operated in a power pulsed mode. So far no conceptual problem was revealed but the studies show the way for further work. The prototype is read out by a DAQ system conceived to meet the needs of a trigger less system with a huge number of readout cells.

1. Introduction

The next major worldwide project in high energy particle physics will be a linear electron positron collider at the TeV scale to complement and extend the scientific results of the LHC. The most advanced proposal for this linear collider is the International Linear Collider (ILC). Here, electron and positrons will be collided at centre-of-mass energies between 0.2 and 1 TeV. The detectors which will be installed around the interaction point are required to achieve a jet energy resolution of $30\%/\sqrt{E}$, thus a factor two better than the energy resolution achieved for a typical detector at LEP. The reconstruction of the final state of the e^+e^- will be based on so-called particle flow algorithms (PFA) [1]. The goal is to reconstruct every single particle of the final state which in turn demands a perfect association of the signals in the tracking systems with those in the calorimeters. As a consequence this requires a perfect tracking of the particle trajectories even in the calorimeters. State of the art Particle Flow algorithms such as the Pandora PFA [2] or ARBOR [3] promise to reach jet energy resolutions between 3% and 4% over an jet energy range from 45 GeV up to the TeV region [4, 5]. At hadron colliders the technique of Particle Flow is applied successfully for the jet reconstruction by the CMS collaboration [6, 7].

To meet the requirements of a detector optimised for PFA, the detectors have to cover the whole solid angle and have to feature an unprecedented high granularity. The calorimeters have to be placed inside the coil of the super-conductive solenoid of the detectors. This puts tight constraints on the available space for the installation of the detectors. The design of the calorimeters have to take the following guidelines into account

- Optimisation of the number of calorimeter cells.

- Choice of the absorber material and the infra-structural components such as cooling, power supplies, readout cables and the very front end electronics.

For the electromagnetic calorimeter at lepton colliders these criteria has lead to the choice of tungsten with a radiation length of X_0=3.5 mm, a Molière of R_M=9 mm and an interaction length of λ_I=96 mm. In the years 2005 to 2011 the CALICE collaboration has performed beam campaigns at DESY, CERN and FNAL in order to demonstrate the principle of highly granular calorimeters and to confront the concept of particle flow with real data. The first results of the data analysis have been published in three articles [8, 9, 10, 11]. The work is now focused on a technological prototype that addresses the engineering challenges which come along with the realisation of highly granular calorimeters. The key parameters of the new prototype are

Figure 1 shows in its left part a schematic view of the technological prototype that can house up to 30 layers with a total depth of $24\,X_0$. The mechanical housing is realised by a tungsten-carbon reinforced epoxy (CRP) composite, which supports at the same time the absorption medium and ensures the mechanical integrity of the detector.


Figure 1. _Left:_ Schematic view of the technological prototype with dimension. _Center:_ Mechanical structure of the technical prototype with a short slab in front and one inserted on the right. _Right:_ 2.5 m alveolar end-cap layer.

A large prototype structure has been produced in 2012, close in scale to a barrel module for the ILD detector concept (see Fig. 1 middle). It features 15×3 1.5 m-long alveola interleaved with Tungsten plates. As shown on the right part of Fig. 1, some long alveolar layer prototypes of 2.5 m in length have been moulded in order to validate the technological specific production process for mechanical structures as needed for ILD.

The left part of Fig. 2 shows a cross section through two calorimeter layers which form a slab. The sensitive parts will be mounted on both sides of tungsten board embedded in an "H" made of carbon fibre, equipped with a thermal drain, wrapped and inserted into the alveoli of the mechanical structure. The silicon wafers are composed of high resistive silicon. An example of a silicon wafer matrix is shown in the right part of Fig. 2. These silicon wafers are glued onto an interface card, called PCB hereafter which carries the ASICs for the readout of the silicon wafers.

2. The silicon sensors

The silicon sensors are the central component of the detector, and also the most expensive. Work is on-going on the sensor design, particularly on the sensor edge. Silicon sensors of various designs and producers have been purchased. These include large $9 \times 9\,\text{cm}^2$ sensors from Hamamatsu
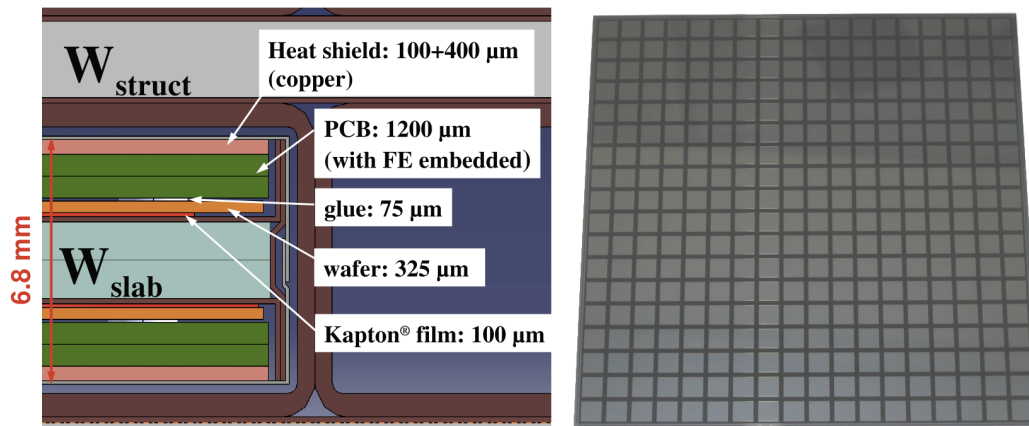
Figure 2. <u>Left:</u> *Cross section through one slab of the prototype with the thickness of the various components.* <u>Right:</u> *Hamamatsu Photonics silicon sensor: 324 pixels of $5 \times 5 \, \mathrm{mm}^2$.*

Photonics (HPK) subdivided in 324 pixels (256 in more recent versions). The HPK sensors have excellent electrical characteristics, and a number of them have been successfully tested in beam tests. An undesirable feature was identified in beam tests with the physics prototype: a large energy deposition near the guard rings provokes a cross-talk between the (electrically floating) sensor guard rings and the pixels at the sensor edge. Dedicated numerical and experimental studies on "baby wafers" of the effect have shown that the effect can at least be attenuated by about a factor of 80 by segmenting the guard ring [12]. Studies with wafers without any guard rings show promising results as well.

Recent tests with an infrared laser shooting in the guard-ring reproduced the cross-talk effect, opening the way to a validation of the design on a test bench.

Simpler and/or "open" designs, which could then be manufactured by non-specialist companies and therefore reducing the sensor cost, have been developed.

3. The SKIROC ASIC
The main purpose of the beam tests carried out in the years 2012 and 2013 was to understand the performance of the highly integrated SKIROC2 circuit [13]. Each of the ASICs reads 64 calorimeter cells and realise the measuring of the analogue signal, the digitisation and the zero suppression such that only a limited number of channels are finally sent to the data acquisition. The ASIC is designed in Silicon Germanium 0.35μm technology. Its outer dimensions are $7.5 \times 8.7 \, \mathrm{mm}$. The signal from the silicon pad is is amplified by a variable gain charge sensitive amplifier and the split into a trigger chain and a chain which actually shapes signal that it is readout by a sample and hold stage. The trigger chain provides an internal trigger fro signals as small as about $1/2$ of a Minimal Ionising Particle (MIP). This corresponds to a charge of about $0.4 \, \mathrm{fC}$. The signal is stored in a 15 bin deep buffer. The buffer is emptied if either all of the 15 buffers of one of the 64 channels is full or if the clearing of the buffer is initiated by an external signal. The signals stored in the buffer are finally digitised by a 12-bit Wilkinson ADC internal to the ASIC.

The implementation of the 15-bin deep buffer is motivated by the beam structure of the International Linear Collider. The beam arrives in so called bunch trains containing up to 3000 bunches. Each bunch train is about 1 ms second long followed by a time gap of about 200 ms. This time structure of the ILC beam allows to operate the ASIC in power pulsed mode. Roughly speaking the front end electronics will only be fully enabled during the millisecond of a bunch
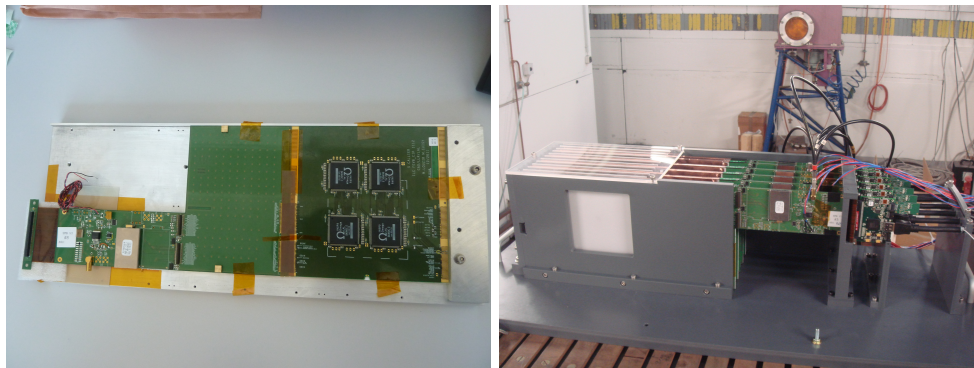
Figure 3. <u>Left:</u> *Picture of one layer of the SiW Ecal setup tested in 2012 and 2013.* <u>Right:</u> *Experimental setup at DESY..*

train of particles.and the bias currents will be shut down during the gap between the bunch trains.

4. Data Acquisition System

The DAQ is divided in four parts. The detector interface (DIF) is reading data directly from the chips and format their data stream in packets. These packets are aggregated by two levels of aggregation cards. The data concentrator card (DCC) aggregates data from the DIF to use the full capacity of the protocol (similar to FastEthernet) on HDMI cable. The Giga concentrator card (GDCC) converts this streams to Giga-Ethernet encoding. The acquisition clock and the detector-level commands are sent through a specific card named the Clock and Control Card (CCC) which convert the analogue signal into numeric words. This commands words are faned-out by both GDCC and DCC to the DIF. A software suite, named Calicoes, handles the data acquisition and control-command of the whole system. A data acquisition chain acquires Gigabit data flow. It is able to dispatch this data through several kind of media (files, shared memory and TCP socket). It verifies the integrity of the data flow and uncaps the data to produce physical events and feed an event builder. The software suite includes also a complete control and command system, allowing to configure all the cards from a single XML configuration file.

5. Beam test setup

Between March 2012 and July 2013 four beam test campaigns have been carried out at the DESY Testbeam facility of which a detailed description can be found elsewhere. Electrons with an energy between 1-6 GeV are delivered to the beam test area. For the beam tests simplified detector layers were fabricated, see left part of Fig. 3. The layers consisted of one silicon wafer glued onto a PCB. This PCB was equipped with four SKIROC ASICs packed in a regular PQFP package. This layers were operated in continuous powering mode in the 2012 running and in power pulsed mode during 2013. During the beam tests up to eight layers were available for tests. and assembled into the mechanical structure as shown in the right part of Fig. 3.

6. Data analysis

Altogether up to 2048 read out cells were available for the data taking. For details, in particular on the analysis of the 2012 data, the reader is referred to [14][1] and [15]. Here a brief summary

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[1] This is an internal CALICE-Note that can be made available upon request. The work is about to get published soon in a refereed journal
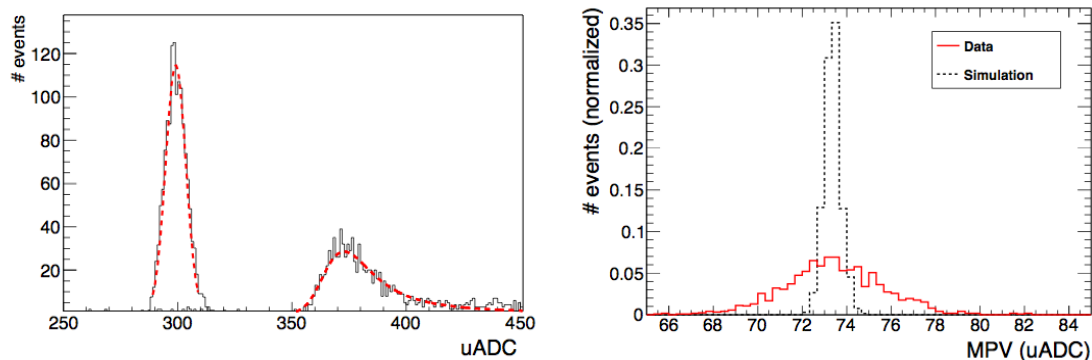
Figure 4. *Left: Pedestal and MIP distribution of one channel. Right: Most probable value of the Landau fit for all active channels in data compared with simulation.*

of the calibration procedure and the data analysis is given.

The first step of the analysis to clean the data from signals caused by hardware issues. The analysis allowed to disentangle effects due to the ASIC from effects rom peripheral devices.. Effects of the ASICs manifest themselves for example by events in which nearly all channels of an ASIC carry a signal. These kind of events are provoked by voltage dips on the ASIC due to high in-rush currents to the ADC in case of e.g. large signals. This shortcoming can e.g. be remedied by a bypass capacitor that stabilises the power supply of the pre-amplifier. Another observation is empty events. Empty events occur if the same signal triggers a readout in two consecutive bunch crossing due to an non-optimal timing of the ASICs w.r.t. the arrival of particles. Empty events won't occur once the timing of the ASICs are coupled to a machine clock. A filter to select undesired events has been developed.

6.1. Calibration of detector modules

The ASIC SKIROC2 [13] is operated in auto-trigger mode. Therefore the calibration starts with the settings of the trigger thresholds. Within the ASIC the signal is shaped and propagated to a sample and hold unit. The readout of the signal happens at a given position determined by the time of the trigger arrival and and internal delay. The goal is to read out when the shaped pulse is at it's maximum. Finally the analogue signal is digitised in Wlikinson-type 12-bit ADC.

The thresholds are determined in a so called threshold scan. For this the internal threshold of the trigger is raised until no or only a few hits of the detector noise are recorded. One threshold threshold is set for all 64 channels of the ASIC. In the next version of the ASIC the threshold will be set on a cell-by-cell basis.

In the hold scan the signal of minimal ionising particles (MIP) is sampled for different delay values. The optimal value hold value is obtained when the Most Probable Value, MPV, of the MIP signal is at maximum as a function of the delay time.

At the example of one channel the left part of Fig. 4 demonstrates the excellent separation of the MIP signal from the detector noise. In [14] the Signal-over-Noise ratio is found to be always above 10:1 for different settings of the SKIROC2 ASIC. The MIP signal is fitted with a Landau distribution and the MPV of that distribution is the calibration constant of a given channel. The right part of Figure 4 shows the distribution of the MIP signal for all active channels in 2012 data taking period. The data are compared with a simulation of the detector. While the position of the MIP is very well reproduced by the simulation the dispersion of the signal cannot be reproduced. The origin of this dispersion is under study.
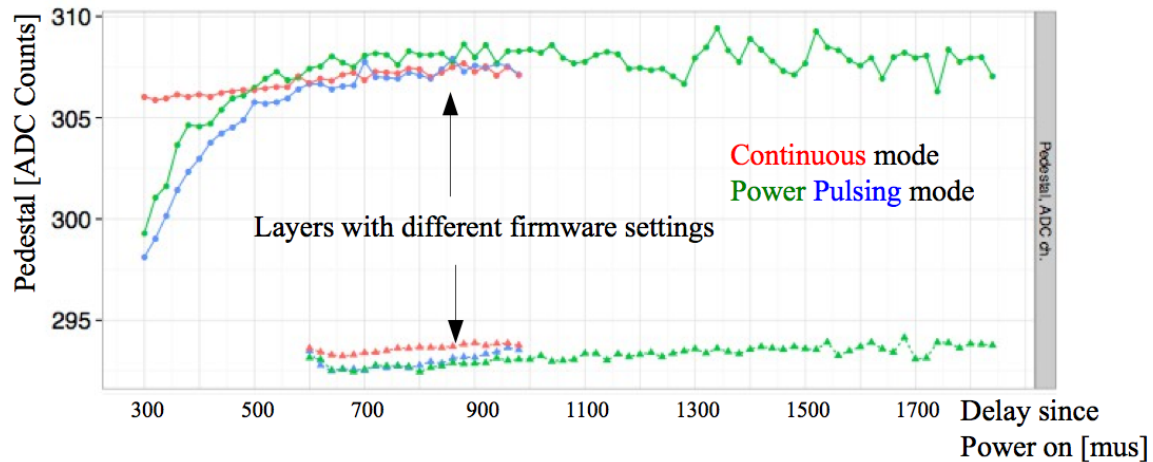
Figure 5. *Pedestal position as a function of time elapsed after the enabling of the bias currents for detector operation in power pulsed mode. The upper and lower lines correspond to two different detector settings. The red line shows the pedestal position for the continuous powering mode.*

6.2. Study of power pulsing
The data taking in 2013 was dedicated to the study the behaviour of the detector in power pulsed mode. Power pulsing implies a periodical shut-down and relaunch of the bias currents that polarise the various stages of the ASIC. After the relaunch a certain delay has to be taken into account until the ASIC is fully operational. The Fig. 5 shows the pedestal position as a function of the time of the signal arrival. In this study two different settings were tested one in which signals can arrive earliest after about $300\,\mu s$ and another with an allowed arrival time of at least $600\,\mu s$. It is clearly visible that the pedestal stabilises after about $600\,\mu s$. The time of stabilisation has been subject to a systematic study for all pixels across a layer. In the left part of Fig. 6 the time dependence of one one cell is approximated by the function $a \cdot (1 - \exp(-(x - 300\mu s)/t)) + c$ where x is the constant of the exponential increase of the pedestal before the stable plateau. As shown in the right part of Fig. 6 this constant is around $100\mu s$ for all cells of the studied layer.

In the following only signals are taken into account that arrive at least $600\,\mu s$ after the relaunch of the bias currents. In the left part of Fig. 7 the correlation of the pedestals between continuous and power-pulsing modes are shown. The right part gives the difference for MIP signals in both operation modes for four ASICs of a layer. The pedestal positions are very well correlated between the two operation modes. The right part shows that for two ASICs the difference in the MIP position is less than 1ADC count equivalent to about 1.5%. The ASICs revealing a bigger difference and therefore worse agreement are connected by relatively long lines to the Si Pads. In [14] it is shown that for these ASICs also the signal over noise ratio is worse than for ASICs connected with short lines to the Si Pads. In the third region the trigger thresholds were too high for various reasons. Details are left to the finalisation of the data analysis.

6.3. Detector simulation
For a deeper understanding of the detector response the detector has been implemented into a detailed GEANT4 simulation. Great care has been taken to the digitisation step of the simulation which allows to reproduce the hardware behaviour in terms of for example residual
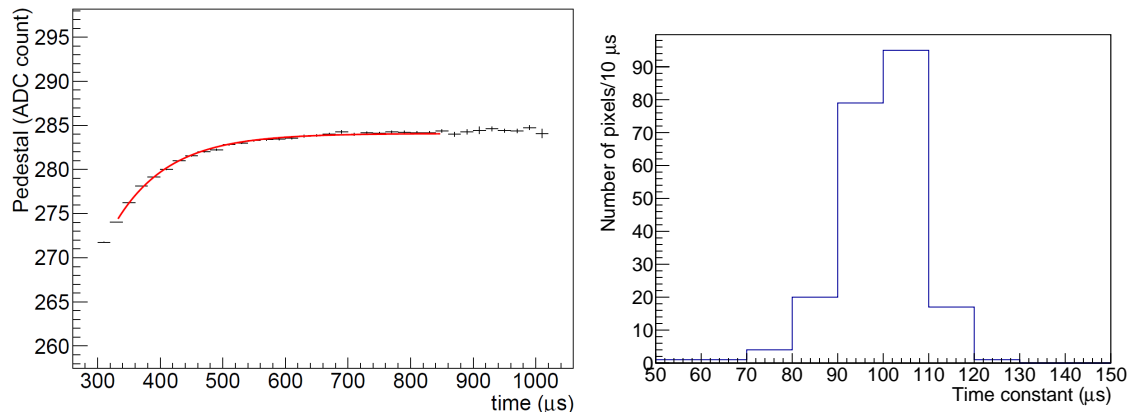
Figure 6. _Left:_ _Time dependence of the pedestal position as time elapsed after the enabling of the bias currents for detector operation in power pulsed mode for one pixel. The functional dependence is approximated by_ $a \cdot (1 - \exp(-(x - 300\mu s)/t)) + c$. _Right:_ _Time constant x for all pixels across a layer._
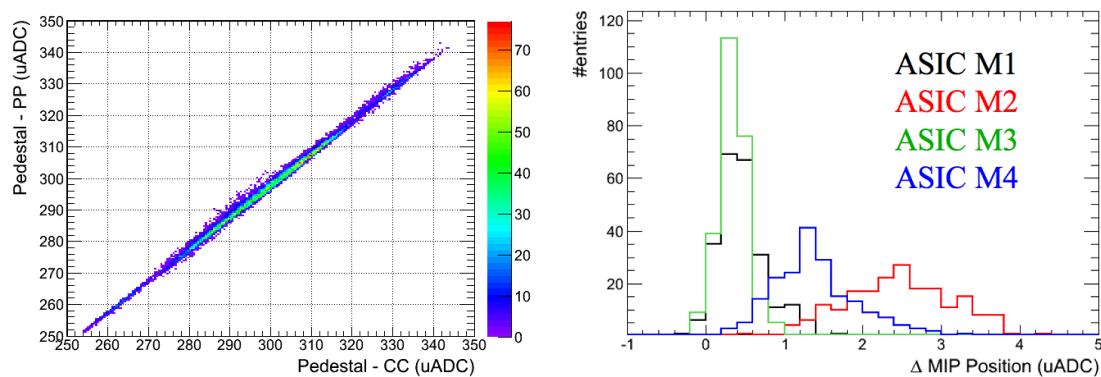

Figure 7. _Left:_ _Correlation between pedestals recorded in continuous and power-pulsed operation of the SKIROC2 ASIC._ _Right:_ _Difference between the MPV of the MIP signal recorded in continuous and power-pulsed operation of the SKIROC2 ASIC.._

detector noise or the influence of the trigger threshold In Fig. 8 the simulation are compared with data for runs in which the mechanical structure was equipped with tungsten plates. The simulation reproduces the data very well.

7. R&D plans and steps towards a real detector

The next few years will be used to progressively complete the technological prototype with up to 30 short ASUs and at least one long layer with up to 10 ASUs. This prototype is to be tested in beam test campaigns in the years 2015-2016.

The very next step is to produce ASUs for four wafers and read out by 16 ASICs. The final layout of the calorimeter for a linear collider detector depends significantly on the success of the PCB manufacturing. As for the sensors a close collaboration with industrial partners is needed. An option for maximum compactness is embedding the naked dies of the front end chips into the PCB. The application of thin BGA packaging is considered at least as a safe intermediate
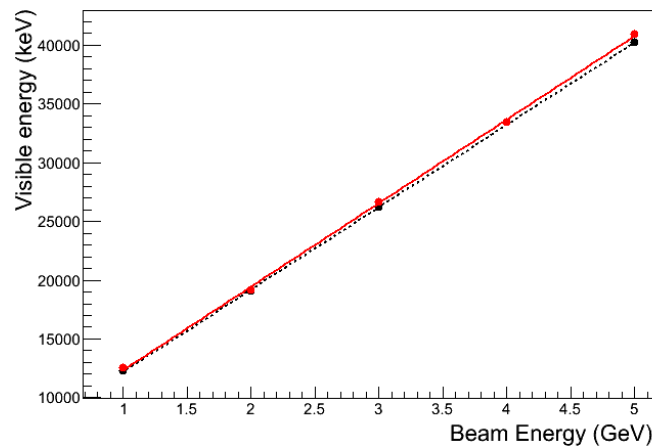
Figure 8. *Comparison between data and simulation of the detector response to electrons between 1 and 6 GeV for runs in which the detector layers were interleaved with tungsten plates.*

step and currently under study.

The final SKIROC ASIC will feature an on-chip zero suppression. As this is a major step it has been agreed to produce first an intermediate version, dubbed SKIROC2b, to assure that (minor) flaws observed with the current SKIROC2 ASIC can be completely remedied. A production run of SKIROC2b ASICs is planned for the end of 2014.

Further development of links with silicon sensor manufacturers is essential in order to better understand the eventual cost of such a detector, and to prepare for possible mass production.

The use of power pulsing in the front end electronics is a central tenet of the detector design. The results obtained in the 2013 beam test campaign are very promising in this respect but need to be confirmed as the system evolves. The validation need to incorporate an estimation of the final power dissipation of the detector.

Many steps of detector construction will be outsourced to industry, and one aim of the technological prototype is to choose techniques which are well adapted to an industrial process. This however requires still scrutinising the available assembly tools and techniques as e.g. the robotic gluing system. In parallel with this, a significant quality control control process will have to be developed, with tests of detector components being carried out at various stages of their integration into detector elements.

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