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Gate-Induced Superconductivity in Layered-Material-Based Electric Double Layer Transistors

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Abstract. High carrier density part of many materials could be accessed by a variation of the field effect transistor technique: electric double layer transistor. Carrier density regime of $n \sim 10^{14} \text{ cm}^{-2}$ can be easily accessed electrostatically realizing effective doping without chemical modification. In this study, we utilized micro-cleavage on a number of interesting layered materials. And realized high carrier density state and high performance transport on atomically flat surfaces.

Recent introduction of micro-cleavage techniques (Scotch-tape method) shows great success on graphene researches. The electrical transport of graphene could be effectively modulated by field effect. Especially, at the low carrier density ($n \sim 10^{12} \text{ cm}^{-2}$) regime, many exciting new physical phenomena were observed. Whereas, for broad range of layered materials, the effectiveness of field effect is confined by the conventional transistor techniques where the maximum carrier density is limited at around $n \sim 10^{13} \text{ cm}^{-2}$. In this research, we aim at studying the transport properties of layered materials with extended carrier concentration electrostatically, especially in the less explored higher density regime using electric double layer transistor (EDLT).

These EDLT utilize ion accumulated on a liquid/solid interfaces as gate dielectrics. They are widely used in applications in high performance organic electronics [1-5], field-induced electronic phase transitions [6-9], as well as superconductivity in SrTiO_3 [10]. Broadening EDLT to creating

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novel transport properties within other interesting materials is interesting especially in layered materials, where special advantage exist because high quality surface could be easily prepared by cleavage. Combining ionic liquids as gate dielectrics, transistor made on mechanical micro-cleavage techniques surface can show field-induced superconductivity with a T_c as high as 15.2 K in ZrNCl. Also, large amount of carriers could also be induced on other materials such as graphene and its multi-layers reaching a value of 2×10^{14} using similar techniques. These highly charged interfaces are interesting candidates for superconductivity researches, which are also investigated in high T_c cuprates for inducing or manipulating superconductivities [11-13].

Thin flakes of layered materials (Graphene, ZrNCl, etc.) were fabricated by exfoliation of bulk crystals using an adhesive tape. The produced thin flakes were subsequently transferred onto a Si substrate covered by 300 nm of SiO₂. The thickness of the flakes was determined by analyzing optical micrographs to extract the intensity shift in the green channel (in RGB composition), Raman spectroscopy, and AFM characterization. A 20 nm thick flake (measured by AFM) was subsequently patterned into a Hall bar configuration (Figure 1(a), top panel) using conventional micro-fabrication techniques (electron beam lithography, electron-beam evaporation, and lift-off). The electrodes consisted in a multilayer Ti/Au/SiO₂ (10/50/30 nm), with Ti providing good electrical contacts and SiO₂ minimizing the direct contact area between the electrodes and the ionic liquids. The carrier was doped onto the surface of the channel by the moving ions accumulated on its surface. As shown in figure 1(b), if we cool down the system at high charged state, the “snap shot” the states at high temperature (220 K) could be maintained to show superconductivity at low temperature.

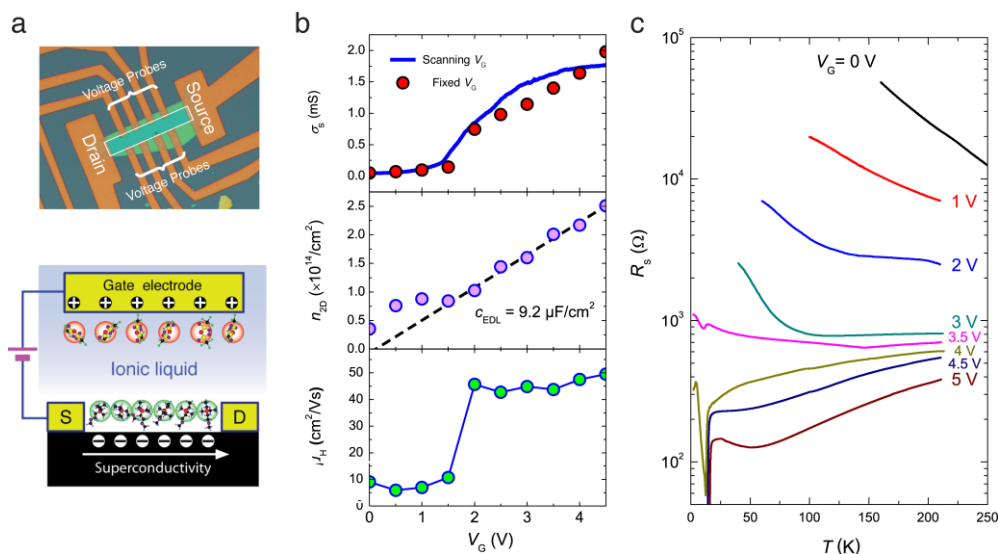


Figure 1 (a), A Hall bar structure made on a ZrNCl thin flake (upper panel) and charge accumulation on surface of materials (down panel) (b), Channel sheet conductance σ_s , sheet carrier density n_{2D} and Hall mobility μ_H of the ZrNCl EDL transistor modulated by the gate voltage V_G from 0 to 4.5 V at 220 K. The solid line in the top panel is obtained by a continuous upward scan of V_G , whereas the open squares represent the conductance in the Hall effect measurement. The dashed line in the middle panel shows a linear fit to the carrier density from which the EDL capacitance was estimated to be $C_{EDL} = 9.2 \mu\text{F}/\text{cm}^2$. (c), Low temperature transport properties of ZrNCl based EDLT and field-induced superconductivity.

The top panel of Figure 1b shows a transfer curve for ZrNCl-EDLT measured at 220 K with a gate voltage scan rate of 0.1 V/min. The sheet conductivity σ_s of the channel is enhanced as a function of gate voltage V_G between 0 to 4.5 V, indicating typical n-channel FET operation with an on/off ratio of around 40. The transfer curve is reversible implying the electrostatic nature of carrier accumulation.

The carrier density n_{2D} on the ZrNCl channel surface (middle panel of Fig. 1b), determined by Hall effect measurements, increases from $n_{2D} = 0.3 \times 10^{14}$ to $2.5 \times 10^{14} \text{ cm}^{-2}$ with increasing V_G from 0 to 4.5 V. In particular, above 1.5 V, n_{2D} increases almost linearly with V_G . From the slope above 1.5 V, the capacitance $c_{EDL} = n_{2D}e/V_G$ of the EDL formed at the ZrNCl surface is estimated to be $9.2 \text{ } \mu\text{F}/\text{cm}^2$, which is larger than that estimated for an electrolyte made of polyethylene oxide and KClO_4 [8]. At $V_G = 0 \text{ V}$, we observed a carrier density of $n_{2D} = 3 \times 10^{13} \text{ cm}^{-2}$ originate from of bulk carriers (corresponding to $n_{3D} = 1.5 \times 10^{19} \text{ cm}^{-3}$) due to chlorine deficiency or hydrogen intercalation formed during the growth of the single crystals [14, 15]. By subtracting n_{2D} at $V_G = 0 \text{ V}$, we can obtain the net gate-tunable carrier density as $n_{2D} = 2.2 \times 10^{14} \text{ cm}^{-2}$, which is larger than that reported for electrolytes [10] and covers the density range required for the insulator-metal transition in the phase diagram of bulk Li_xZrNCl . The Hall mobility μ_H , shown in the bottom panel of Fig. 2b, displays a threshold behavior at 1.5 V as μ_H abruptly increases from 10 to $50 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and then shows an almost constant value at higher V_G of $50 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. It is noted that the $\mu_H = 50 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ agrees well with that of bulk Li_xZrNCl [16], estimated from transport measurements of polycrystalline samples. The threshold behaviors (i.e. the sheet conductivity σ_s shows a quick increase, the carrier density n_{2D} shows linear increase, and the shift to higher mobility) indicate the formation of FET channel when V_G reaches 1.5 V. This feature also suggests that the channel conductance becomes dominant over the bulk contribution at $V_G > 1.5 \text{ V}$.

Figure 1c displays the temperature dependence of the sheet resistance R_s at different gate voltages. R_s at $V_G = 0 \text{ V}$ increases with decreasing temperature, showing typical insulating behavior. The contribution from the bulk carriers is frozen at low temperature, consistent with the previous results and the band insulator picture of undoped ZrNCl [17]. The gate voltage V_G was applied at 220 K, followed by cooling the device with fixed V_G . R_s is dramatically reduced at low temperatures by increasing V_G associated with the decrease of the activation energy, followed by an occurrence of the insulator-metal transition. At $V_G = 3.5 \text{ V}$, a small dip in R_s appears near 14 K, which is the first sign of superconductivity as confirmed by its dependence under a magnetic field. Further development of superconductivity and suppression of resistance upturn appear by increasing V_G from 3.5 to 4 V; superconducting transitions with zero resistance are observed at $V_G = 4.5$ and 5 V.

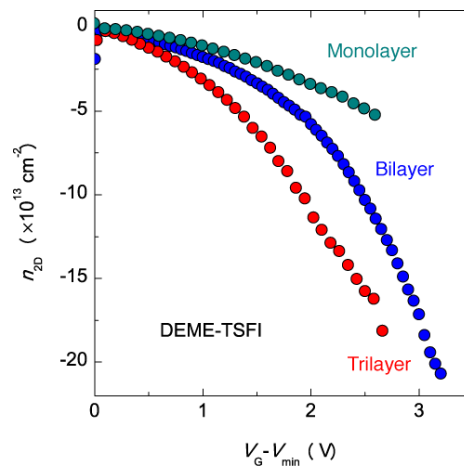


Figure 2 The gate voltage V_G dependence of carrier density n_{2D} using DEME-TSFI as the gate dielectrics. The maximum carrier density reaches $2 \times 10^{14} \text{ cm}^{-2}$ in the bilayer graphene.

Mono-, bi-, and trilayer graphene devices were fabricated on SiO_2/Si substrates by exfoliating graphite [18]. The graphene based EDLT was fabricated in similar way as that of ZrNCl. We measure the sample gated with different ionic liquids of DEME-TSFI, ABIM-TSFI, and DEME- BF_4 ; this is important to check that the features observed in the experiments are not artifact caused by the specific

ionic liquid. The measurements were performed in a limited gate voltage range, to avoid the occurrence of chemical reactions between the ionic liquid and graphene, as it is necessary to obtain reproducible and reversible results. Despite this limitation, charge density as large as $n_{2D} \approx 2 \times 10^{14} \text{ cm}^{-2}$ could be reached.

In summery, ionic liquid gating appears to be an effective and reliable technique to accumulate very large amounts of carriers at liquid/solid interface on layered materials. Although our investigations have mainly focused on basic aspects of the electronic properties, the technique has the potential to have a much broader impact, both to disclose new phenomena of fundamental interest and for possible future applications. For instance, the high transition temperature in ZrNCl EDLT indicates gate-induced superconductivity could be a useful technique in manipulating the superconductivity even at high temperature if high T_c . High carrier density obtained from other materials could be important for inducing superconductivity in other materials.

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