New Journal of Physics
The open access journal at the forefront of physics

Deutsche Physikalische Gesellschaft DPG IOP Institute of Physics

PAPER • OPEN ACCESS

Cryogenic surface ion trap based on intrinsic silicon

To cite this article: Michael Niedermayr *et al* 2014 *New J. Phys.* **16** 113068

View the article online for updates and enhancements.

You may also like

- Diversifying beam species through decay and recapture ion trapping: a demonstrative experiment at TITAN-EBIT
E Leistenschneider, R Klawitter, A Lennarz et al.

- Studies of highly charged iron ions using electron beam ion traps for interpreting astrophysical spectra
G V Brown, C Beilmann, S Bernitt et al.

- Hybrid MEMS-CMOS ion traps for NISQ computing
M G Blain, R Haltli, P Maunz et al.

This content was downloaded from IP address 18.218.38.125 on 23/04/2024 at 10:06

New Journal of Physics
The open access journal at the forefront of physics
Deutsche Physikalische Gesellschaft DPG | IOP Institute of Physics

Cryogenic surface ion trap based on intrinsic silicon

Michael Niedermayr[1], Kirill Lakhmanskiy[1], Muir Kumph[1], Stefan Partel[2], Jonannes Edlinger[2], Michael Brownnutt[1] and Rainer Blatt[1,3]

[1] Institut für Experimentalphysik, Universität Innsbruck, Technikerstr. 25, A-6020 Innsbruck, Austria
[2] Forschungszentrum Mikrotechnik, FH Vorarlberg, Hochschulstr. 1, A-6850 Dornbirn, Austria
[3] Institut für Quantenoptik und Quanteninformation, Österreichische Akademie der Wissenschaften, Technikerstr. 21A, A-6020 Innsbruck, Austria
E-mail: michael.brownnutt@uibk.ac.at

Received 7 April 2014, revised 30 June 2014
Accepted for publication 15 October 2014
Published 26 November 2014

New Journal of Physics **16** (2014) 113068

doi:10.1088/1367-2630/16/11/113068

Abstract

Trapped ions are pre-eminent candidates for building quantum information processors and quantum simulators. To scale such systems to more than a few tens of ions it is important to tackle the observed high ion-heating rates and create scalable trap structures which can be simply and reliably produced. Here, we report on cryogenically operated intrinsic-silicon ion traps which can be rapidly and easily fabricated using standard semiconductor technologies. Single $^{40}Ca^{+}$ ions have been trapped and used to characterize the trap operation. Long ion lifetimes were observed with the traps exhibiting heating rates as low as $\dot{\bar{n}} = 0.33$ phonons s^{-1} at an ion-electrode distance of 230 μm. These results open many new avenues to arrays of micro-fabricated ion traps.

Keywords: surface ion trap, silicon, cryogenic

1. Introduction

Processing information using a quantum system allows problems to be solved which are difficult or impossible to compute classically [1], and trapped atomic ions provide a promising platform for such quantum information processors [2–4]. Ions can be confined using a combination of radio-frequency (RF) and static (dc) electric fields [5]. The electrode structures

Content from this work may be used under the terms of the Creative Commons Attribution 3.0 licence. Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.

© 2014 IOP Publishing Ltd and Deutsche Physikalische Gesellschaft

required to create the appropriate fields can take a variety of geometries, and great progress has recently been made using planar structures [6, 7]. For these, all electrodes are located in a plane above which the ions are trapped. Notable among the advantages of such a structure is the scalability [8]: arrays with hundreds or thousands of traps can in principle be built on a single chip using very-large-scale integration technologies like optical lithography and etching, far exceeding what is possible using bulk fabrication.

In making such traps a reality, a number of features must be considered. It is essential that scalable trap architectures have low RF losses: if the losses are too high the RF power applied in order to trap will be dissipated in the chip. Additionally, microfabrication has become highly developed and it would be desirable to bring these techniques to bear on ion traps. For large arrays of traps the creation of through-wafer vias [9], so that electrical connections can be made throughout the array, is a prerequisite. Optical addressing of ions in an array can be facilitated by fabrication of holes through the substrate. Moreover, the integration of on-chip electronics, such as would be afforded by complementary metal-oxide-semiconductors (CMOS), would open up untold possibilities for ion traps [10, 11].

Surface ion traps can be broadly divided into two groups, according to the type of substrate material: dielectric or semiconductor. Dielectric substrates like sapphire or fused silica have a very low RF power dissipation. For such traps the electrodes are created by simple optical lithography combined with lift-off processes or electroplating on top of the substrate [12]. However, dielectric materials are difficult to pattern by means of wet or dry etching and not suitable for features such as through-wafer vias. The second type of substrate materials are semiconductors, such as silicon, which are easy to structure. Slots, holes and vias with aspect ratios up to 160 can be etched by standard techniques [13]. However, the RF losses in intrinsic (i.e. undoped) silicon at room temperature are significant.

In some cases, the issue of RF losses was mitigated by using highly doped silicon for the trap electrodes [14, 15] or substrate [16]. This method would not, however, work in a cryogenic environment because of the silicon's low electrical conductivity at low temperatures. In other cases there was an additional ground electrode which shielded the silicon against the trapping RF voltage [17–19]. This type of trap can also be operated at cryogenic temperatures [20], though it necessitates a more complicated fabrication process and precludes vias for RF electrodes.

At low temperatures, the charge carriers in intrinsic silicon freeze out, leaving the substrate as a good insulator with low RF loss. This obviates the need for a shielding electrode. By operating intrinsic-silicon traps at cryogenic temperatures and omitting the shielding ground-plane, the trap capacitances and the amount of power dissipated can be reduced. A range of fabrication techniques also become available, which would have otherwise have been precluded either by the substrate material or the ground plane. Intrinsic silicon is already used for several superconducting-qubit applications in the mK-range [21, 22], though all silicon-based ion traps to date have been designed to operate at room-temperature.

In this paper, we report on silicon-based surface ion traps built for cryogenic applications. The cryogenic environment inheres several advantages which are well known. Ultra-high vacuum can be attained within a few hours due to cryogenic pumping, without baking the system [23]. This facilitates fast turn-around times for trap installation (∼1 day). Furthermore, operation at liquid-helium temperatures reduces the rate at which the ions' motion is heated, typically by around two orders of magnitude [24]. This is beneficial as it increases the coherence time of the ions' motion, which is used to transfer quantum information between

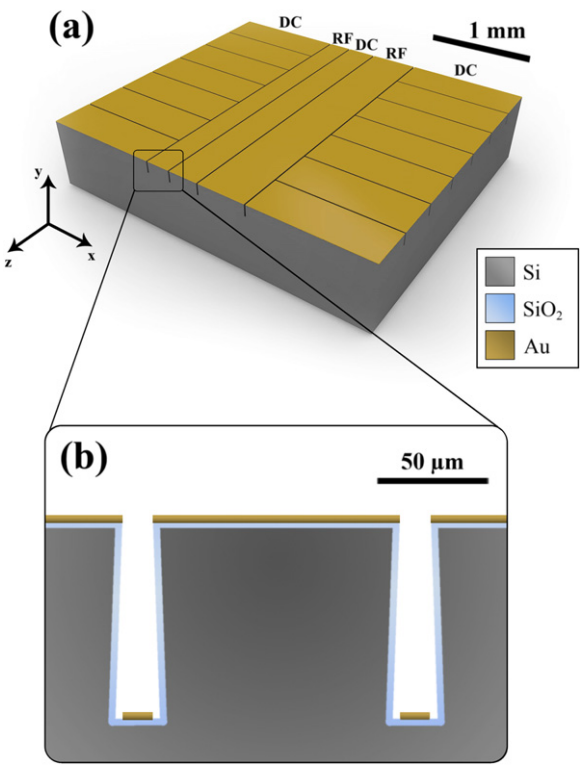

Figure 1. (a) Schematic showing the surface-trap design. The trap consists of a pair of asymmetric RF electrodes (widths of 200 µm and 400 µm respectively), a centre dc electrode (width: 250 µm) and seven segmented dc electrodes on each side (axial width: 350 µm). The electrode separation is 10 µm. This geometry allows strings of ions to be trapped 230 µm above the surface. (b) Cross section through the trap. Trenches etched to a depth of ~100 µm separate the individual electrodes. The entire silicon surface is covered by a thermally grown SiO_2 layer preventing metals from diffusing into the silicon. The trap electrodes are created by gold deposition normal to the surface. Well-defined undercuts prevent electrical connection between the different electrodes.

different ions. In addition to these benefits, the novel use of intrinsic silicon as a trap material means that the traps neither need nor have a ground plane to shield the substrate. This allows for a very simple basic fabrication procedure and permits the use of standard silicon processing techniques, while mitigating the problems of RF loss.

2. Design overview and fabrication

The planar design used for this work is illustrated in figure 1. The electrode layout is based on a similar design used elsewhere [25]. Ions are trapped 230 µm above the centre electrode by applying an RF voltage to the two RF electrodes. Lasers used to Doppler cool the ions are aligned parallel to the plane of the trap, to minimize scatter from the surface. To efficiently cool the ions along all three principal axes of their motion, each axis must have a projection along the direction of the cooling laser beam. Consequently, none of the principal axes of motion should be perpendicular to the trap surface. The RF electrodes have thus been fabricated with unequal widths ensuring that the two radial principal axes both have a component parallel to the

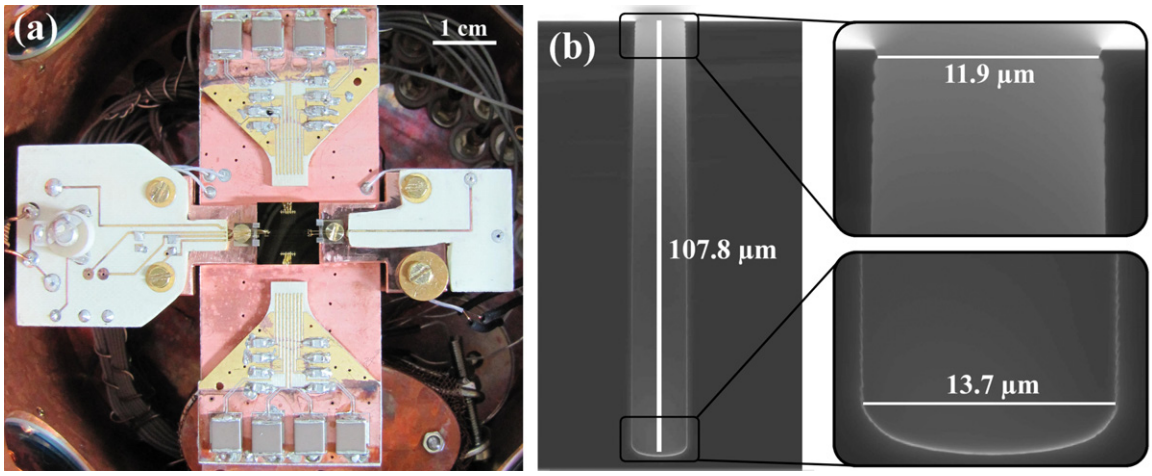

Figure 2. (a) Cryostat's 10 K stage. The trap is at the centre. The dc filters are located on the vertical printed circuit board. The LC drive circuit is mounted on the left of the trap and a capacitive divider for measuring the trap voltage is on the right. (b) Scanning electron microscope images of an undercut trench formed by deep reactive ion etching separating two electrodes.

trap surface [26]. Seven segmented electrodes are located on each side of the two RF electrodes. Dc voltages are applied to these electrodes and create confinement along the axial (z) direction. Ions can be shuttled along the z-axis by changing the dc voltages. Stray electric fields arising from contamination of the trap or imperfection in trap fabrication can cause micromotion [27], which is minimized by adding suitable dc voltages to the segmented dc electrodes.

To fabricate the traps an intrinsic silicon substrate is patterned by optical lithography and deep reactive ion etching (see figure 2(b)). Deep, undercut trenches are etched in the substrate and mark the gaps between the individual electrodes. Following a thermal growth of 2 µm of SiO_2 the electrodes are formed by evaporation of gold perpendicular to the surface. Due to the undercuts, there is no electrical connection between the different electrodes (figures 1(b) and 2(b)) and no further lift-off or etching steps are necessary. There are no further cleaning steps and, to avoid any contamination of the surface, the gold electrodes are never brought into contact with liquids such as solvents for cleaning. The fabrication process and the packaging are explained in detail in appendix A.1.

Initially, the operation of a single trap (trap #1) was characterized in detail over several weeks. To demonstrate the reproducibility of the results, a further five traps—randomly selected from two different silicon wafers—were tested and shown to exhibit similar behaviour.

3. Cryogenic setup

The silicon ion trap is cooled to 10 K in a closed-cycle, two-stage, Gifford McMahon cryostat equipped with a vibration-isolation system [23, 28] to reduce the vibrations at the trap to around 100 nm at 2 Hz. The trap is attached to the second cooling stage of the cryostat (figure 2(a)). It is enclosed by a copper shield, also cooled to 10 K. This minimizes the incident black-body radiation and reduces the number of background molecules at the trapping site, as they freeze on the shield walls. Surface contamination caused by background gas molecules freezing out on

the trap electrodes during the cool down can be reduced by temporarily heating the trap. Since the background gas mainly consists of water, it is sufficient to keep the trap at 320 K till the first stage of the cryostat has reached a temperature of 240 K. Thereafter the second stage is cooled to 10 K, while the first stage reaches a final temperature of 50 K. $^{40}Ca^{+}$ ions are loaded from a neutral Ca-beam produced by a resistively heated oven located within the vacuum chamber but not mechanically connected to the cold stage. The atoms are introduced to the trapping region through a small hole in the copper shield (diameter ~3 mm) and are ionized by a two-photon process [29] in the trapping region.

The voltage on the RF electrodes (amplitude $U_0 = 140$ V, frequency $\Omega_T/2\pi = 20.6$ MHz) is provided by an LC lumped-circuit resonator driven by a function generator [28] and creates a trapping potential with trap depth of 75 meV. The power dissipation in the resonator goes as $P_D = U_0^2 C\Omega_T/2Q$, where C is the resonator capacitance and Q the quality factor of the resonator. To keep P_D low, C must be kept small. This is achieved by locating the resonator in vacuum next to the trap on the cold stage of the cryostat (see figure 2(a)). The measured C is 9.5 pF, which is mainly limited by the capacitance of the RF electrodes. The power necessary for trapping is less than 10 mW, which is well below the cryostat's cooling power of 500 mW and increases the temperature measured next to the trap by only 0.2 K. Filters with a cut-off frequency of 4.8 kHz are mounted on the cold stage next to the resonator in order to filter the voltages applied to the dc electrodes (see appendix A.2 for further details on the LC resonator and dc filters). Dc voltages in the range $-40\ \text{V} < V_{dc} < 40\ \text{V}$ are applied to the central three electrode segments and provide an axial trapping frequency of around 1 MHz. With this voltage configuration the principal radial axes are tilted with respect to the x and y directions by approximately 20°.

4. Silicon at cryogenic temperatures

The characterization of the RF resonator (including the trap) as a function of temperature is shown in figure 3. The inductor of the LC resonator is provided by a copper coil with an air (vacuum) core and the capacitance primarily comes from the trap's RF electrodes. The quality factor, Q, was recorded while the cryostat was slowly heated up. The temperature was measured by a silicon diode mounted on the copper trap carrier. Q follows the relation $1/Q = 1/Q_L + 1/Q_C$, where Q_L and Q_C are the quality factors of the inductor and the capacitor, respectively.

At room temperature the silicon substrate, which supports the RF electrodes, has a very high loss tangent [30], $\tan\delta$, of 1.5 at the driving frequency $\Omega_T/2\pi = 20.6$ MHz. For comparison, under the same conditions, $\tan\delta$ of fused silica is around $\sim 10^{-4}$ [31]. Due to the high loss tangent, at room temperature the entire RF driving power is absorbed by the silicon substrate. There is no measurable resonance: using an impedance analyzer the measured resonator Q was less than 20, and within the measurement uncertainty it was indistinguishable from zero. In contrast, a quality factor of 400 was measured in a similar trap fabricated on a fused-silica substrate and operated at room temperature. Cooling leads to a reduction of the charge-carrier concentration in the silicon and, below 100 K, to a steep decrease of the electrical conductivity and loss tangent. Ultimately, all free charge carriers freeze out at ~25 K and the silicon becomes an insulator [30]. In addition to these changes in the silicon, the electrical conductivity of the coil increases with decreasing temperature, and therefore the inductor

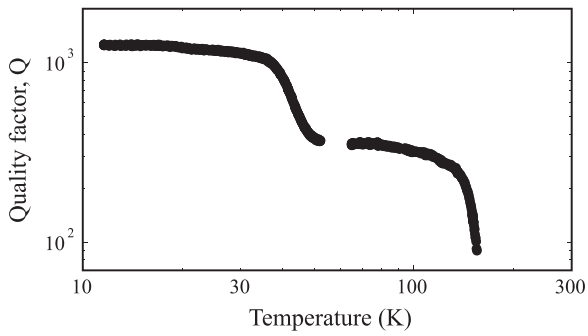

Figure 3. Resonator quality factor as a function of temperature. The inductive and capacitive parts of the LC resonator are predominantly provided by a copper air-coil and the trap RF electrodes, respectively. At room temperature, the entire RF driving power is absorbed by the silicon substrate and there is no measurable resonance. On cooling, the conductivity of the inductor increases (thereby increasing its quality factor, Q_L). Cooling also reduces the charge-carrier concentration in the silicon and, below 100 K, causes a steep decrease of its electrical conductivity and loss tangent (thereby increasing the capacitive quality factor, Q_C). These effects all serve to increase the overall Q, with the plateau around 100 K being due to the nonlinear response of the material properties. Below 20 K, the quality factor is comparable to that measured with a fused-silica trap, meaning that Q is limited by Q_L and that $Q_C \gg Q_L$. The data shown were measured in trap #1 (see table 1). The other five traps tested showed similar behaviour.

quality factor, Q_L, goes up [28]. Increasing Q_C and Q_L leads to an increasing overall resonator quality factor, Q, with decreasing temperature, as shown in figure 3. Below 20 K the value of $Q > 1200$ is comparable to that measured with a fused-silica trap at the same temperature indicating that Q is then only limited by Q_L and not by RF absorption in the silicon.

Photocharging of trap structures has previously been observed in a number of experiments [32, 33]. In the traps reported here, it is in principle possible that photons could also excite charge carriers in the silicon of the trenches' sidewalls which are not covered by gold. Such an effect could disturb trap operation. To investigate this possibility, the resonator's quality factor was measured at low temperature both with trapping lasers on and off to determine the influence of the laser light. The trap was directly illuminated with around 10 mW cm^{-2} of laser light at each of the wavelengths used to trap $^{40}Ca^+$ ions (375 nm, 397 nm, 422 nm, 729 nm, 854 nm and 866 nm). However, no changes in performance were observed. Furthermore, while trapping $^{40}Ca^+$ ions, no effects due to photocharging of the substrate were observed.

5. Trapped ion lifetime

A trapping parameter which becomes especially important with a large number of trapped ions is the length of time for which an ion can be trapped, sometimes called the trapped-ion lifetime. The loss of a single ion can complicate the implementation of, for example, a quantum algorithm. While trapping lifetimes of a few minutes may be acceptable for experiments using small numbers of ions, experiments with many ions require significantly longer ion lifetimes, as the probability of losing an ion increases. Ions are usually lost by collisions with background gas molecules or by motional heating. A cryogenic setup is an ideal tool to achieve long

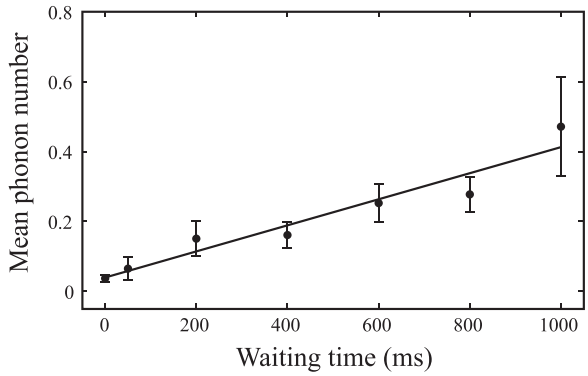

Figure 4. Heating-rate measurement. Mean phonon number, $\bar{n}$, of the axial mode ($\omega_z/2\pi = 1.069$ MHz) as a function of the waiting time after ground-state cooling. $\bar{n}$ was determined by measuring the Rabi flops on the blue sideband [35]. In this instance the heating rate, taken to be the gradient of a linear fit to the data, is $\dot{\bar{n}} = 0.37(6)$ phonons s^{-1}. Taking data on different days over a period of six weeks the trap exhibited a heating rate of $\dot{\bar{n}} = 0.6(2)$ phonons s^{-1}.

lifetimes since it provides extremely high vacuum and helps to reduce heating rates [23, 24, 34, 36].

Cooled and uncooled ion lifetimes were investigated using trap #1. With laser cooling, no ion losses were recorded over a total experimental period of more than 50 h with a single ion. To investigate uncooled lifetimes, the lasers were turned off and, after some waiting time, turned back on to see if the ion was still trapped. Waiting times of up to 9 h were used, and the ions were never lost. The trap is therefore suitable for scaling up to hundreds of ions without the need for continuous reloading. Five further traps were tested for shorter periods and the results from these traps were consistent with the more extended observations made with trap #1.

6. Heating rates

For many quantum-information applications ions should be at or near their motional ground state, and heating of the ions' motion degrades the quality of quantum operations. Trapped ions are predominately heated by electric-field noise resonant with the ions' motional frequencies. To measure the heating rate [35], the axial motion of a single ion was cooled to near the ground state by resolved-sideband cooling. Following a predefined waiting time, the mean phonon number was determined by two different methods: measurement of the transition probability on the red and blue sidebands and Rabi flops on the blue sideband [35]. The heating rate was determined by the change in phonon number with different waiting times (figure 4).

Over a period of six weeks, the heating rate in trap #1 was measured several times and found to be constant, within the error bars, at $\dot{\bar{n}} = 0.6(2)$ phonons s^{-1}. The electric-field noise inferred to underlie this heating [36] is $S_E = 4.4 \times 10^{-15}\,V^2\,m^{-2}\,Hz^{-1}$. Heating rates were measured in five further traps, four from the same wafer and one (trap #6) from a second wafer, with the results given in table 1.

Trap #5 exhibits a heating rate of 0.33(4) phonons s^{-1}, which is the lowest measured heating rate ever reported: the lowest previously-reported heating rate at room temperature was 0.83(10) phonons s^{-1} in a trap with a 3.5 mm ion-electrode separation [37]. The lowest previously-reported

Table 1. Heating rates of different Si traps. Heating rates of six traps, all of the same design, with an ion–electrode separation of 230 μm. Measurements were made over 84 days. Traps #1–5 were taken from a single Si wafer, with trap #6 being from a second wafer. The heating rate measured in trap #5 is 0.33(4) phonons s^{-1}, which is the lowest rate ever reported.

Trap #	Heating rate (phonons s^{-1})	Axial frequation (MHz)
1	0.6(2)	1.069
2	3.3(2)	1.059
3	0.96(7)	1.069
4	0.95(7)	1.045
5	0.33(4)	1.066
6	21.5(8)	1.073

heating rate at cryogenic temperatures was 2.1(3) phonons s^{-1} in a trap with a 100 μm ion-electrode separation [38]. It is not known to what extent the lower heating rate in the present trap can be attributed to the use of silicon, rather than the lower temperature (compared to [37]) or larger trap dimensions (compared to [38]). The reason for the variation in heating rates between traps on the same wafer is not known, though it is not necessarily surprising, given the level of variation which is often observed in nominally identical traps [36]. Trap #6 exhibits a heating rate of 21.5(8) phonons s^{-1}. This falls well within the range of heating rates observed in other cryogenic ion traps [36, 39], but is is significantly higher than the other five traps tested here. The second wafer, from which trap #6 was taken, was nominally identical to the first, but was patterned separately. Slightly modified etch parameters were used, so that the underetch initially proceeded at a steeper angle. It is not known whether this is related to the higher heating rate.

7. Conclusion and outlook

We have presented a new ion-trap design based on a silicon substrate. This will allow trap fabrication to benefit from well-developed silicon-fabrication processes. The design was made possible by exploiting the fact that, at low temperatures, intrinsic silicon becomes an insulator with low RF losses. The traps exhibit a high Q of >1200 and reproducibly low ion-heating rates of around 1 phonon per second at a trap frequency of 1 MHz.

Fabrication could be extended to include slots for increased optical access [17] and through-wafer vias [9]. Unlike room-temperature silicon traps, vias in our design would also work at RF frequencies, allowing the realization of a 2D trap array with adjustable RF electrodes [40]. One may ultimately envision such traps integrated with a wide variety of other silicon-based technologies including CMOS electronics [10, 11], micro-optics [41], micro- and nano-mechanical systems, and sensors. This would ultimately mean that the entire science package, including optical, mechanical, and electronic functions could be integrated on a single substrate to provide a quantum lab on a chip.

Acknowledgments

MN thanks M Brandl for discussions about dc filters. SP thanks P Choleva and S Stroj for assisting during the trap fabrication. The authors acknowledge support from the European

Research Council (ERC) through the projects CRYTERION #227959 and CARAT #334952, the Fonds zur Förderung der wissenschaftlichen Forschung (FWF) project Q-SAIL, and the Institute for Quantum Information GmbH.

Appendix

A.1. Trap fabrication and packaging

High-purity float-zone silicon wafers (diameter: 100 mm, thickness: 525 μm) with specific resistivity larger than 5000 Ωcm were used. The wafers were coated by the positive photoresist AZ1518 with a thickness of 2.4 μm. The resist was patterned by means of standard optical lithography. The wafers were deep reactive ion etched by gas chopping based on SF_6 and C_4F_8 to create trenches with slight undercuts separating the different electrodes of the ion traps. The 10 μm gaps between the electrodes were etched to a depth of ∼100 μm with an undercut of ∼1 μm. The resist was then removed by O_2 plasma cleaning. A 2 μm thick SiO_2 layer was grown on the silicon surface by thermal oxidation to prevent metals from diffusing into the silicon. Each wafer provided 52 traps and the individual trap chips were separated by laser scribing. To form the electrodes, titanium and gold layers of a thickness of 2 nm and 500 nm respectively were deposited on the substrate surface by electron-beam evaporation. No further cleaning steps were performed after evaporation.

Traps were mounted on a copper carrier. To ensure good thermal contact between the trap and the carrier, each trap was coated on the backside with a thin layer of heat-conducting grease (Apiezon-N) and then clamped in place by two stainless-steel forks. Printed circuit boards (PCBs) (Rogers—RO4350B) supporting the dc filters and the LC resonator where glued (Stycast—2850-FT) to the carrier. The trap electrodes were connected to the PCBs by 25 μm thick gold wirebonds. The copper traces on half of each PCB were gold-electroplated to increase the adhesion of the bonding wires from the trap to the PCBs (see figure 2(a)). The wiring of the cryostat to connect the PCBs to the outside world is explained in detail in [28]. The entire fabrication and assembly process of the trap took place in a cleanroom to reduce surface contamination. The only exception to this was installing the trap in the cryostat itself which was not located in a cleanroom, though this step took less than ten minutes.

A.2. LC resonator and dc filter

The lumped-circuit LC resonator is similar to that reported by Gandolfi *et al* [28] and is formed by a homebuilt copper air-coil inductor with an inductance of 6.3 μH mounted next to the trap, a capacitance of 9.5 pF provided by the trap's RF electrodes, and a capacitive voltage divider. The circuit's resonance frequency is 20.6 MHz at 10 K. The capacitive divider, which allows the measurement of the voltage on the RF electrodes, has a ratio of 1:400 and a total capacitance of 2.5 pF. It consists of one 1000 pF capacitor (CDE—MC22FD102J-F) and two 5 pF capacitors (CDE—MC12CD050D-F) arranged in parallel. Furthermore, there is a matching network to match the LC circuit to 50 Ω. This is located next to the resonator at the 10 K stage. It consists of a tunable capacitor (12–100 pF, Johanson Manufacturing—9328) and a homebuilt inductor (186 nH) connected in series and parallel, respectively.

For best trapping performance all dc electrodes must be properly RF-grounded which can be accomplished by installing capacitors as close as possible to the dc electrodes. For this

reason, small surface-mounted NP0 capacitors with a capacitance of 470 pF (Kemet—C0805C471J1GACTU) are located ~15 mm from the electrodes. Additionally, RC low-pass filters are used to filter RF noise on the dc lines. The filters each consist of a 100 Ω thin-film resistor (VPG—Y1625100R000Q9R) and a 330 nF NP0 capacitor (Kemet—C2220C334J1GACTU) placed ~30 mm from the trap. The cut-off frequency of these filters is 4.8 kHz. The resistors and capacitors used are cryo-compatible and do not significantly change performance during cooling. In addition to these filters there are 6th-order RC low-pass filters outside of the vacuum chamber with a cut-off frequency of 80 Hz.

References

[1] Nielsen M A and Chuang I L 2011 *Quantum Computation and Quantum Information* (Cambridge: Cambridge University Press)

[2] Ladd T D, Jelezko F, Laflamme R, Nakamura Y, Monroe C and OBrien J L 2010 Quantum computers *Nature* **464** 45–53

[3] Blatt R and Wineland D 2008 Entangled states of trapped atomic ions *Nature* **453** 1008–15

[4] Zoller P *et al* 2005 Quantum information processing and communication strategic report on current status visions and goals for research in Europe *Eur. Phys. J.* D **36** 203–28

[5] Major F G, Gheorghe V N and Werth G 2005 *Charged Particle Traps: Physics and Techniques of Charged Particle Field Confinement* (Berlin: Springer)

[6] Chiaverini J, Blakestad R B, Britton J, Jost J D, Langer C, Leibfried D, Ozeri R and Wineland D J 2005 Surface-electrode architecture for ion trap quantum information processing *Quantum Inf. Comput.* **5** 419

[7] Hughes M D, Lekitsch B, Broersma J A and Hensinger W K 2011 Microfabricated ion traps *Contemp. Phys.* **52** 505–29

[8] Kim J, Pau S, Ma Z, McLellan H R, Gates J V, Kornblit A, Slusher R E, Jopson R M, Kang I and Dinu M 2005 System design for large-scale ion trap quantum information processor *Quantum Inf. Comput.* **5** 515–37

[9] Motoyoshi M 2009 Through-silicon via (TSV) *Proc. IEEE* **97** 43–48

[10] Mehta K K, Eltony A M, Bruzewicz C D, Chuang I L, Ram R J, Sage J M and Chiaverini J 2014 Ion traps fabricated in a CMOS foundry *Appl. Phys. Lett.* **105** 044103

[11] Alonso J, Leupold F M, Keitch B C and Home J P 2013 Quantum control of the motional states of trapped ions through fast switching of trapping potentials *New J. Phys.* **15** 023001

[12] Seidelin S *et al* 2006 Microfabricated surface-electrode ion trap for scalable quantum information processing *Phys. Rev. Lett.* **96** 253003

[13] Parasuraman J, Summanwar A, Marty F, Basset P, Angelescu D E and Bourouina T 2014 Deep reactive ion etching of sub-micrometer trenches with ultra high aspect ratio *Microelectron. Eng.* **113** 35–39

[14] Sterling R C, Rattanasonti H, Weidt S, Srinivasan P, Lake K, Webster S C, Kraft M and Hensinger W K 2014 Fabrication and operation of a two-dimensional ion-trap lattice on a high-voltage microchip *Nature Commun.* **5** 3637

[15] Britton J, Leibfried D, Beall J A, Blakestad R B, Wesenberg J H and Wineland D J 2009 Scalable arrays of RF Paul traps in degenerate Si *Appl. Phys. Lett.* **95** 173102

[16] Wilpers G, See P, Gill P and Sinclair A G 2012 A monolithic array of three-dimensional ion traps fabricated with conventional semiconductor technology *Nat. Nanotechnol.* **7** 572–6

[17] Allcock D T C *et al* 2012 Heating rate and electrode charging measurements in a scalable, microfabricated, surface-electrode ion trap *Appl. Phys.* B **107** 913–9

[18] Doret S C *et al* 2012 Controlling trapping potentials and stray electric fields in a microfabricated ion trap through design and compensation *New J. Phys.* **14** 073012

[19] Leibrandt D R *et al* 2009 Demonstration of a scalable, multiplexed ion trap for quantum information processing *Quantum Inf. Comput.* **9** 901

[20] Vittorini G, Wright K, Brown K R, Harter A W and Doret S C 2013 Modular cryostat for ion trapping with surface-electrode ion traps *Rev. Sci. Instrum.* **84** 043112
[21] Chang J B *et al* 2013 Improved superconducting qubit coherence using titanium nitride *Appl. Phys. Lett.* **103** 012602
[22] Johnson J E, Macklin C, Slichter D H, Vijay R, Weingarten E B, Clarke J and Siddiqi I 2012 Heralded state preparation in a superconducting qubit *Phys. Rev. Lett.* **109** 050506
[23] Antohi P B, Schuster D, Akselrod G M, Labaziewicz J, Ge Y, Lin Z, Bakr W S and Chuang I L 2009 Cryogenic ion trapping systems with surface-electrode traps *Rev. Sci. Instrum.* **80** 013103
[24] Brownnutt M, Kumph M, Rabl P and Blatt R 2014 Ion-trap measurements of electric-field noise near surfaces arXiv:1409.6572
[25] Daniilidis N, Narayanan S, Möller S A, Clark R, Lee T E, Leek P J, Wallraff A, Schulz S, Schmidt-Kaler F and Häffner H 2011 Fabrication and heating rate study of microscopic surface electrode ion traps *New J. Phys.* **13** 013032
[26] Shaikh F A and Ozakin A 2012 Stability analysis of ion motion in asymmetric planar ion traps *J. Appl. Phys.* **112** 074904
[27] Berkeland D J, Miller J D, Bergquist J C, Itano W M and Wineland D J 1998 Minimization of ion micromotion in a Paul trap *J. Appl. Phys.* **83** 5025–33
[28] Gandolfi D, Niedermayr M, Kumph M, Brownnutt M and Blatt R 2012 Compact radio-frequency resonator for cryogenic ion traps *Rev. Sci. Instrum.* **83** 84705
[29] Gulde S, Rotter D, Barton P, Schmidt-Kaler F, Blatt R and Hogervorst W 2001 Simple and efficient photo-ionization loading of ions for precision ion-trapping experiments *Appl. Phys.* B **73** 861–3
[30] Krupka J, Breeze J, Centeno A, Alford N, Claussen T and Jensen L 2006 Measurements of permittivity, dielectric loss tangent, and resistivity of float-zone silicon at microwave frequencies *IEEE Trans. Microw. Theory Techn.* **54** 3995–4001
[31] Kaye G W C and Laby T H 1995 Section 2.6.5 Dielectric properties of materials *Tables of Physical and Chemical Constants* (London: Longmans Green)
[32] Harlander M, Brownnutt M, Hänsel W and Blatt R 2010 Trapped-ion probing of light-induced charging effects on dielectrics *New J. Phys.* **12** 093035
[33] Wang S X, Low G H, Lachenmyer N S, Ge Y, Herskind P F and Chuang I L 2011 Laser-induced charging of microfabricated ion traps *J. Appl. Phys.* **110** 104901
[34] Berkeland D J, Miller J D, Bergquist J C, Itano W M and Wineland D J 1998 Laser-cooled mercury ion frequency standard *Phys. Rev. Lett.* **80** 2089–92
[35] Leibfried D, Blatt R, Monroe C and Wineland D 2003 Quantum dynamics of single trapped ions *Rev. Mod. Phys.* **75** 281–324
[36] Labaziewicz J, Ge Y, Leibrandt D R, Wang S X, Shewmon R and Chuang I L 2008 Temperature dependence of electric field noise above gold surfaces *Phys. Rev. Lett.* **101** 180602
[37] Poulsen G, Miroshnychenko Y and Drewsen M 2012 Efficient ground-state cooling of an ion in a large room-temperature linear Paul trap with a sub-hertz heating rate *Phys. Rev.* A **86** 051402
[38] Wang S X, Ge Y, Labaziewicz J, Dauler E, Berggren K and Chuang I L 2010 Superconducting microfabricated ion traps *Appl. Phys. Lett.* **97** 244102–244102–3
[39] Labaziewicz J, Ge Y, Antohi P, Leibrandt D R, Brown K R and Chuang I L 2008 Suppression of heating rates in cryogenic surface-electrode ion traps *Phys. Rev. Lett.* **100** 013001
[40] Kumph M, Brownnutt M and Blatt R 2011 Two-dimensional arrays of radio-frequency ion traps with addressable interactions *New J. Phys.* **13** 073043
[41] Streed E W, Norton B G, Jechow A, Weinhold T J and Kielpinski D 2011 Imaging of trapped ions with a microfabricated optic for quantum information processing *Phys. Rev. Lett.* **106** 010502