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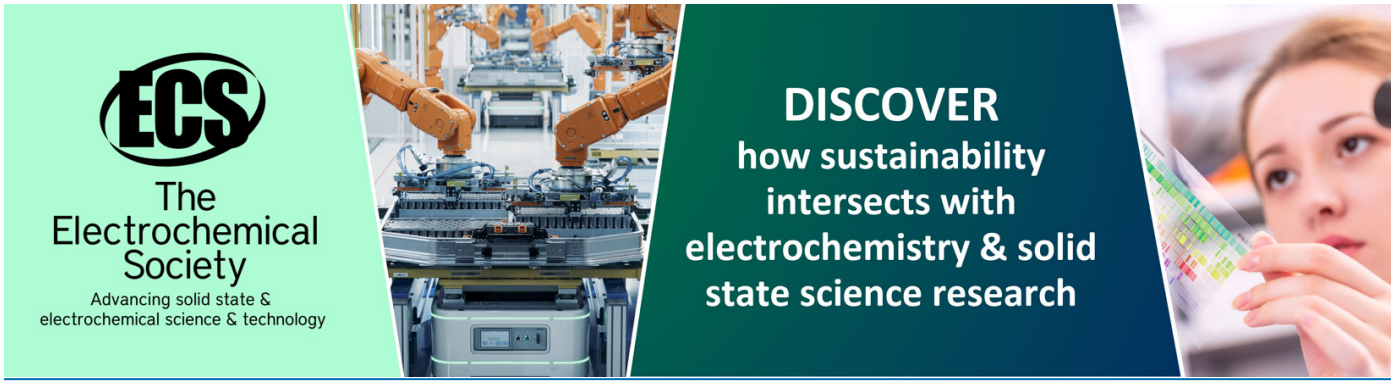

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APCVD hexagonal boron nitride thin films for passive near-junction thermal management of electronics

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Abstract

The ability of graphene to serve as an ultrathin heat spreader has been previously demonstrated with impressive results. However, graphene is electrically conductive, making its use in contact with electronic devices problematic from a reliability and integration perspective. As an alternative, hexagonal boron nitride (h-BN) is a similarly structured material with large in-plane thermal conductivity but which possesses a wide band gap, thereby giving it potential to be utilized for directing contact, near-junction thermal management of electronics without shorting or the need for an insulating intermediate layer. In this work, the viability of using large area, continuous h-BN thin films as direct contact, near-junction heat spreaders for electronic devices is experimentally evaluated. Thin films of h-BN several square millimeters in size were synthesized via an atmospheric pressure chemical vapor deposition (APCVD) method that is both simple and scalable. These were subsequently transferred onto a microfabricated test device that simulated a multigate transistor while also allowing for measurements of the device temperature at various locations via precision resistance thermometry. Results showed that these large-area h-BN films with thicknesses of 77–125 nm are indeed capable of significantly lowering microdevice temperatures, with the best sample showing the presence of the h-BN thin film reduced the effective thermal resistance by 15.9% $\pm$ 4.6% compared to a bare microdevice at the same power density. Finally, finite element simulations of these experiments were utilized to estimate the thermal conductivity of the h-BN thin films and identify means by which further heat spreading performance gains could be attained.

Supplementary material for this article is available online

Keywords: thin films, thermal conductivity, electronics thermal management, chemical vapor deposition, hexagonal boron nitride

(Some figures may appear in colour only in the online journal)

Introduction

It is well known that the decreasing size and increasing density of transistors over time has significantly advanced computing capabilities. However, these factors also have led to greater power dissipation across the device, die, and system levels [1–3]. To complicate matters, the power dissipation in modern electronics can be highly non-uniform, with localized cores or other functional areas having power densities five to ten times higher than the average across the die [4–6]. These

power-dense regions can in turn produce 'hot spots' where local temperatures are significantly higher than the spatially averaged temperature [1, 4, 6, 7]. A similar situation is faced at the individual device level where a localized high temperature region can form near the junction between the drain contact and channel in a transistor [1, 3–8]. Because the reliability of electronics is determined by the hottest region of the device rather than its average temperature, hot spots often dictate the upper limits of power and performance for a given device if its target reliability and lifetime goals are to be met. Hence, there is a great desire to have effective near-junction thermal management solutions that minimize the magnitude and negative influence of hot spots. Further, the ideal solution should be scalable and passive, i.e. can be implemented on the wafer-scale and would not require electrical power input. To achieve this, there is a pressing need to find high thermal conductivity (κ) materials to serve as near-junction heat spreaders that can also offer straightforward integration into electronic devices and are compatible with existing semiconductor processing techniques.

In answer to this need, the large in-plane κ of graphene [8–15] as well as its compatibility with modern micro/nanofabrication processes has recently led researchers to investigate its potential to serve as a device-level heat spreader [16–24]. Several of these studies reported ~8 °C–45 °C of temperature reduction compared to devices without graphene present [17, 20, 22], especially impressive considering that these reductions could represent more than an order of magnitude improvement in device lifetime [22]. Unfortunately, graphene is electrically conductive, making its use in direct contact to electronic devices problematic from a reliability and integration perspective without the presence of an additional performance-degrading insulation layer. However, there may be an alternative material that can overcome these limitations and still act as an effective near-junction heat spreader. Hexagonal boron nitride (h-BN) is a nontoxic material which, like graphite, possesses a layered atomic structure and is known for its high in-plane κ of 350 $W\,m^{-1}\,K^{-1}$ at 300 K [25]. Significantly, h-BN differs from graphite in its more chemically inert nature [26] and wide 4–6 eV bandgap [27, 28]. Due to these advantageous properties, h-BN has been used in high temperature lubricants, protective coatings for sensors in harsh operating environments, advanced thermal management packaging for electronics, and many other moderate-to-high temperature applications where the electrically conductive or chemically reactive nature of graphite prohibits its use [29]. Single- and few-layer atomic sheets of h-BN are analogous to graphene in structure and can likewise be obtained by mechanical exfoliation, chemical vapor deposition (CVD) on certain metals, or other methods. The hexagonal atomic ordering and wide bandgap [30–32] of ultrathin h-BN make it a superior dielectric material for use in graphene-based electronic devices compared to conventional oxides [33, 34], leading it to be considered part of the next wave of 2D materials research [35]. Further, studies have shown that suspended bi-layer and few-layer mechanically exfoliated h-BN possesses similarly high in-plane κ, comparable or superior to bulk h-BN [36, 37]. Even higher κ values near 750 $W\,m^{-1}\,K^{-1}$ have been predicted for isotopically purified single-layer h-BN [38] but have yet to be observed experimentally.

In terms of using h-BN nanomaterials for heat spreading from hot spots in electronic devices, Sun *et al* formed microns-thick composite films from ultrasonically liquid-phase exfoliated h-BN sheets and acetate cellulose. These composite films were able to reduce the temperature of a 400 μm × 400 μm serpentine heater by 20 °C under an applied power density of 625 $W\,cm^{-2}$ [39]. A follow-on work by Bao *et al* used drop-cast solutions of liquid-phase exfoliated h-BN and graphene to form ~8 μm thick heat spreading films with random stacking onto a test chip with similarly sized serpentine heater [40]. Their best result was an 8 °C–10 °C reduction in hot spot temperature at a power density of ~900 $W\,cm^{-2}$ for h-BN/graphene composite films, with h-BN-only films showing reduced heat spreading capability in comparison. For such films with many randomly stacked sheets, the non-continuous nature of the film could lead to significant inter-sheet contact resistance, which can in turn limit heat spreading performance.

While multiple methods of mechanical and liquid-phase exfoliation are known for producing h-BN nanosheets, these are generally not compatible with large-scale production or industrial electronics integration. Hence, methods of obtaining large-area h-BN films via CVD on metallic substrates have received significant attention. Besides superior scalability, the continuous nature of the atomic layers in these CVD films would help reduce the negative effects of inter-sheet contact resistance mentioned above. Alam *et al* measured an in-plane κ value of about 100 ± 10 $W\,m^{-1}\,K^{-1}$ for CVD-grown h-BN films 10 and 20 nm thick, attributing the lower value compared to bulk to growth-related imperfections within the samples [41]. Despite this lower value of κ for CVD h-BN versus mechanically exfoliated h-BN, the superior scalability and integration capabilities of CVD h-BN and its appreciable κ (~100× better than conventional oxide dielectrics) still make it an appealing candidate to achieve device-level heat spreading in electronics. For example, Lin *et al* [42] studied the effect of having CVD-grown h-BN in contact with a high electron mobility transistor (HEMT), with a 2 nm thick h-BN region connected to a much thicker h-BN region alongside the device that served as a heat sink. It was experimentally demonstrated that the presence of this thin-to-thick h-BN material improved important HEMT performance metrics such as maximum available gain and saturation current.

The above studies, while using h-BN from multiple methods, possessing differing internal morphologies (i.e. stacked flakes versus continuous layers, few-layer versus microns-thick) and employing dissimilar thermal characterization approaches, have collectively served to demonstrate that h-BN thin films in general are effective at direct contact heat spreading. However, to the authors' knowledge no study has been published to-date on the ability of CVD-derived h-BN thin films of uniform thickness to serve as a direct contact heater spreader. In this work, continuous thin films are grown on commercially available nickel foil via a simple

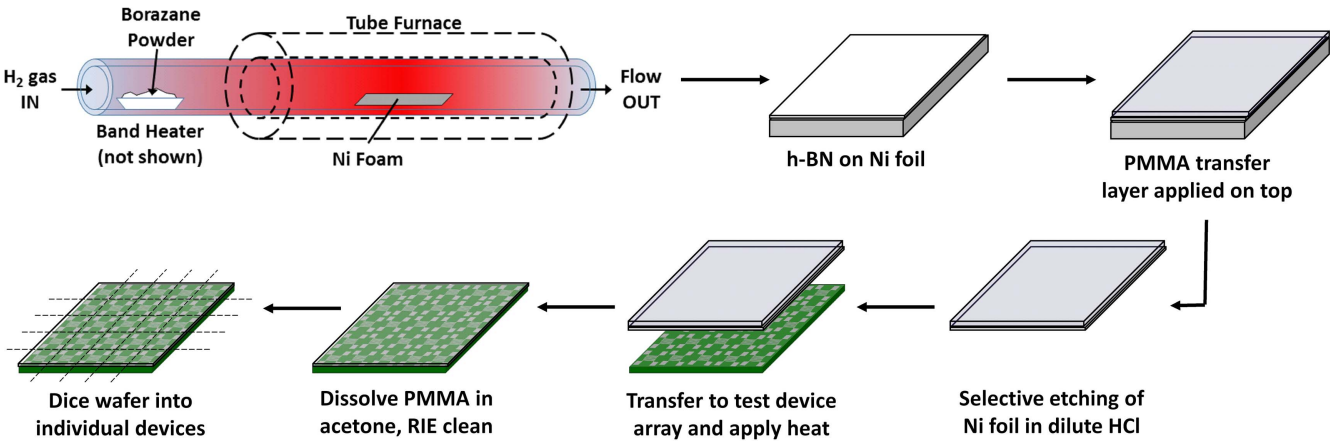

Figure 1. APCVD growth and PMMA-assisted transfer process flow for realizing h-BN thin films on prefabricated microdevice arrays.

atmospheric pressure CVD (APCVD) method and then transferred to a separate silicon/silicon dioxide substrate for further testing. The heat spreading performance of these transferred APCVD h-BN thin films is determined using a microfabricated device that simulates a multi-gate transistor geometry. Besides mimicking an actual transistor, the microdevice facilitates spatial temperature sensing away from a localized heat source via a series of platinum resistance thermometers (PRTs). The h-BN thin films are also characterized via micro-Raman spectroscopy and atomic force microscopy following transfer. Finally, finite element analysis is employed to replicate each experiment, thereby serving to validate the experimental results as well as allow for deeper insights and conclusions to be drawn for each sample.

Methods

The h-BN thin films were grown using an APCVD process adapted from one detailed in our previously published works on foam-like h-BN nanomaterials [43, 44]. First, a section of commercially available 15 mm × 20 mm nickel (Ni) foil (MTI Corp.) was inserted into the center of a 25.4 mm outer-diameter quartz tube furnace (Lindberg/Blue M Mini-Mite). This foil acts as a catalytic substrate for the subsequent surface deposition of h-BN atomic layers. A quartz boat containing 1 g of borane-ammonia complex (also known as borazane) powdered precursor (Sigma Aldrich) was loaded directly upstream of the entrance of the furnace's heating zone. Prior to deposition, the Ni foil was annealed under H_2 gas at 160 sccm flow rate for two hours to remove surface oxide and improve grain structure. The processing pressure and temperature were maintained at ~7 kPa gauge pressure (108 kPa absolute pressure) and 1000 °C, respectively, during both annealing and h-BN deposition processes. For the h-BN growth, the borazane powder was sublimated to vapor by heating to 120 °C via a pair of external band heaters. The band heaters and furnace were turned off after one hour under these conditions and the sample allowed to cool under continuous H_2 flow [43].

Next, the h-BN-on-Ni underwent a procedure that allowed for transfer of the h-BN thin film onto arrays of batch-fabricated microdevices on a 100 mm diameter wafer. Figure 1 illustrates the steps associated with this procedure. First, the h-BN-on-Ni was dipped in a 12 wt% PMMA/chlorobenzene solution and cured at 100 °C for 2 h. The solidified PMMA acted as a protectant for the h-BN during the subsequent etching of the Ni. It also served the purpose of an easy-to-handle mechanical support layer that facilitated transfer of the h-BN thin film to the microdevice array. Selective etching of the Ni foil was performed in 0.5 M hydrochloric acid (HCl) on a hot plate at 100 °C for approximately 2 h until all of the Ni was removed [43]. After the Ni was removed, the PMMA/h-BN was gently rinsed in a bath of deionized water and allowed to air dry before being manually transferred to the microdevice array. The PMMA/h-BN was placed h-BN side down on the wafer-based microdevice array followed by baking on a hot plate for 10 min in order to remove any residual moisture and provide better sample adhesion to the microdevices. This process was repeated with multiple pieces of PMMA-on-h-BN until as many microdevices as possible were observed to be covered by h-BN. The wafer was then placed in a room temperature acetone bath for approximately 12 h to dissolve the PMMA transfer layer. Any residual PMMA was subsequently removed via oxygen-based reactive-ion etching (RIE). During the RIE process, the oxygen plasma was flown at the flow rate of 51 sccm for 10 min and the pressure and power were maintained at 300 mTorr and 400 watts respectively. Finally, the microdevice array was diced into individual 4 mm × 4 mm microdevices for testing. For all tested samples, h-BN film covered the entirety of the microdevice as observable via optical microscopy.

Individual h-BN thin film samples were characterized using micro-Raman microscopy (Horiba Xplora Plus) with a 532 nm wavelength and 10× objective at random locations in order to confirm that the resulting material was indeed h-BN. Additional micro-Raman, energy dispersive spectroscopy, and x-ray diffraction (XRD) characterization of h-BN nanomaterials from this method can be found in our previous works as well [43, 44]. Finally, film thicknesses for measured

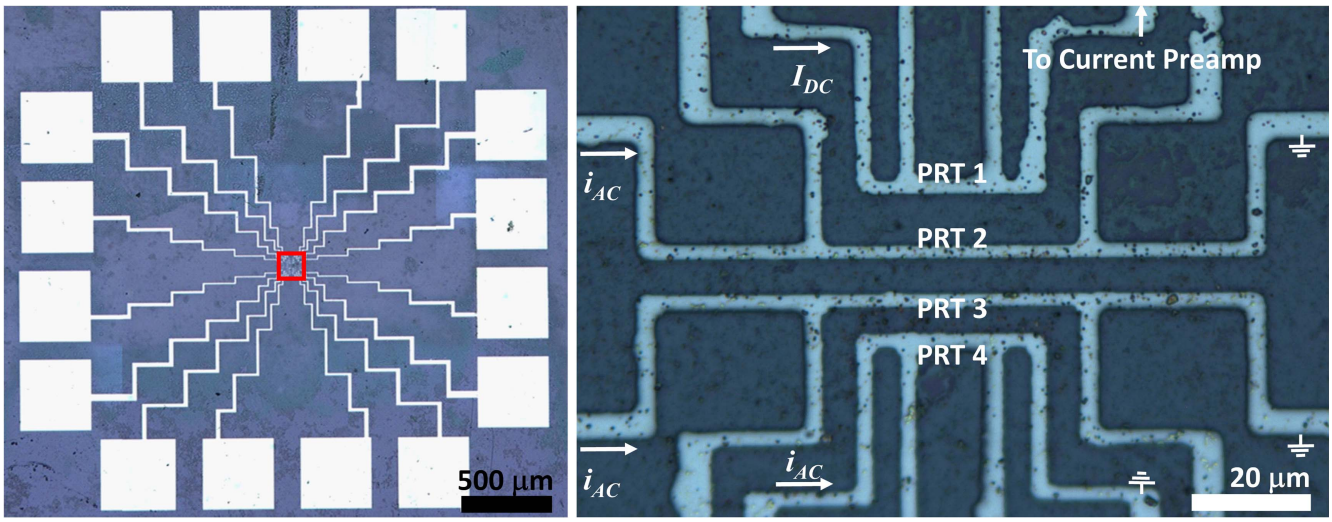

Figure 2. Annotated optical microscope images of a representative sample. (Left) An individual microdevice with transferred h-BN thin film. Large square features around the periphery are contact pads. The central test region with four-probe PRTs is outlined in red. (Right) Detail of the red-boxed region showing the h-BN thin film entirely overlaying the four four-probe PRT lines. Annotations indicate application of DC heating (I_{DC}) and smaller AC sensing (i_{ac}) currents. Inner electrodes without annotation were used for measuring the voltage drops in the four-probe regions of each PRT using either a voltage preamplifier in the case of PRT1 or a lock-in amplifier in the case of PRTs 2–4.

h-BN heat spreader samples were determined via atomic force microscopy (AFM, Agilent Technology 5420). The results of these characterization efforts are presented and discussed within the Results section below.

An annotated image of an individual microdevice with transferred h-BN thin film on top is shown in figure 2. For the microdevice fabrication, a 500 μm thick silicon (Si) wafer having a 1 μm thick layer of silicon dioxide (SiO_2) was used as a substrate. The microdevice design consists of a series of 2 μm wide, 60 nm thick four-probe PRT lines with connecting traces leading to larger contact pads around the chip periphery. To create the device, the lift-off resist LOR 5B was first spin coated onto the 100 mm diameter SiO_2-on-Si wafer to enhance the final metal lift-off process. Shipley 1813 photoresist was subsequently spun on the top of LOR 5B followed by UV exposure through a patterned photomask. After developing the exposed wafer, a 10 nm thick titanium adhesion layer and 50 nm thick platinum (Pt) layer were sequentially deposited using DC magnetron sputtering. The metal lift-off process was performed by soaking the wafer in Remover PG at 80 °C. Once liftoff was complete, the wafer with its microdevice array was complete and ready for the h-BN transfer process described above.

Following dicing of the wafer into individual microdevices, each microdevice was examined via light microscope to identify candidates for measurement. Contiguous sections of h-BN thin film were found to be several square millimeters in size, which was smaller than the parent Ni foil due to losses during the transfer process. For all tested samples, h-BN film covered the entirety of the microdevice as observable via optical microscopy. In addition, the samples chosen for thermal characterization were those whose h-BN thin film had no observable wrinkles, breaks, holes, or cracks. The microdevices with samples selected for measurement were each wire-bonded into a commercial ceramic chip carrier package and loaded into a cryostat (Janis Research) with high precision silicon diode temperature sensor and closed loop temperature control. All testing was done within a turbo pump-provided high vacuum (10^{-5} Torr) condition to ensure 0.01 K temperature stability and prevent convective losses such that the conduction-based heat spreading behavior of the h-BN thin films could be isolated for study. Radiation shielding surrounded the sample space within the cryostat to minimize errors due to radiative heat loss from the sample.

During an experiment, the closed loop control system was first used to set and maintain the temperature of the sample stage T_s within the cryostat to values between 325 and 425 K. Once the temperature within the cryostat was stable at the T_s of interest to within 0.01 K, Joule heating was induced within PRT1 and its outer two lead lines via application of a fixed DC voltage from a high precision power supply. The associated DC current (I_{DC} = 1–5 mA) was measured using an SR570 low-noise current preamplifier (Stanford Research Systems) while the voltage drop across the four-probe region of PRT1 was monitored via an SR560 low-noise voltage preamplifier (Stanford Research Systems) connected to PRT1's inner two electrodes. From this information, the power dissipation and electrical resistance of the four-probe region were directly known. Further, by monitoring the change in electrical resistance of PRT1 relative to the silicon diode-measured base temperature across multiple data sets, a calibration curve of PRT1's change in electrical resistance versus temperature was obtained. Thus, measurement of the changes in PRT1's electrical resistance could then be readily translated into the average temperature rise across its central four-probe region.

Simultaneously, a much smaller AC sensing signal i_{ac} = 500 nA was used to monitor the four-probe electrical resistance changes of the other non-heating PRTs via SR830 lock-in amplifiers (Stanford Research Systems). Similar to the

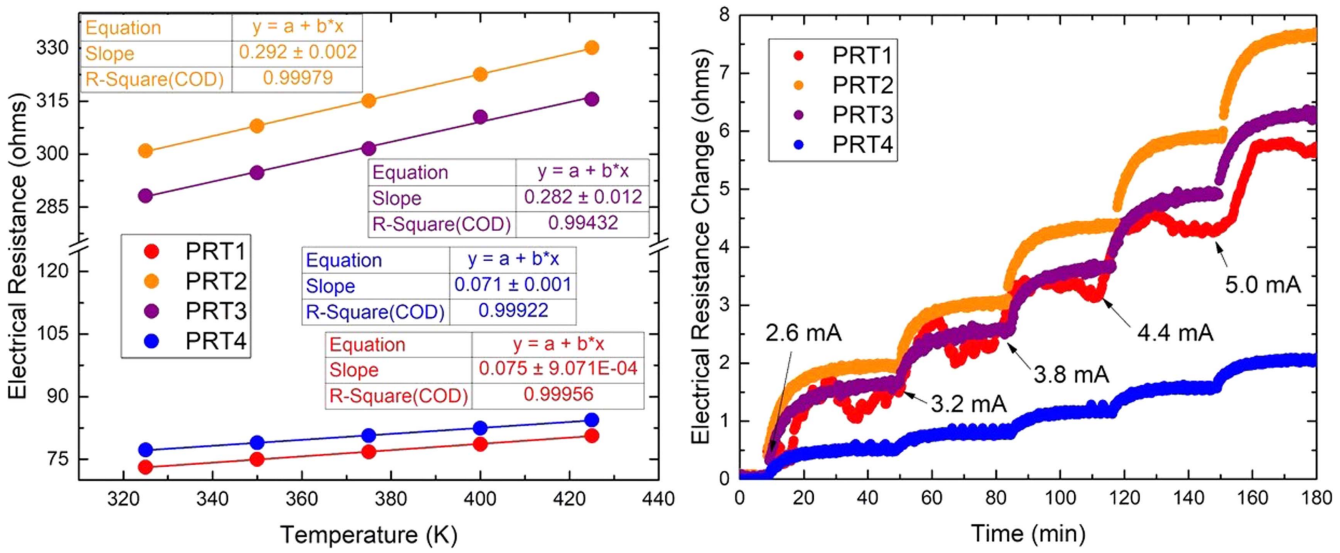

Figure 3. (Left) Representative four-probe electrical resistance values at various stage temperatures for PRTs 1–4. The slope of the linear fit (solid lines) for each PRT is its dR/dT value. (Right) Representative raw data of electrical resistance changes for PRTs 1–4 taken from h-BN-covered microdevice Sample 3 at a stage temperature $T_s = 400$ K. Points in time at which the DC heating current I_{DC} was changed are indicated, with the experiment starting at 0.01 mA.

method for PRT1, the change in electrical resistance versus temperature for each of these non-heating PRTs was determined via calibration against the cryostat's internal stage-mounted silicon diode. This information was later used in post-processing to convert the measured changes in electrical resistance into the average temperature change within the four-probe region of each respective non-heating PRT. The measured changes in electrical resistance (and, hence, changes in temperature) were monitored over time and allowed to reach steady-state before increasing the applied DC heating power to a new level. For each measurement, multiple heating power values were used to order to determine the relationship between temperature rise and heating power for each PRT. All measurements were performed via a computer-controlled data acquisition system external to the setup. Multiple data points were obtained for each sample at T_s between 325 and 425 K in order to capture a wide range of operating temperatures typically associated with electronic devices. Testing was first performed for a 'blank' microdevice without h-BN present to provide a baseline through which the effectiveness of transferred h-BN thin films to act as a thermal management solution could be ascertained.

Representative raw data obtained for one of the sample microdevices at $T_s = 400$ K is shown in figure 3. Note that due to differences in length of the four-probe regions, PRT1 and PRT4 have a ~4× lower electrical resistance than PRT2 and PRT3. For example, for the device whose data is plotted in figure 3, measured electrical resistance values at $T_s = 400$ K and negligible PRT1 heating were 78.62 ohms, 322.60 ohms, 310.50 ohms, and 82.44 ohms for PRTs 1–4, respectively. Similar values were obtained for all other samples measured in this work. As a result, the change in electrical resistance with temperature dR/dT is also ~4× lower for PRT1 and PRT4 compared to PRT2 and PRT3. For the microdevice whose data is plotted in figure 3, dR/dT values of 0.075 ohm K^{-1}, 0.292 ohm K^{-1}, 0.282 ohm K^{-1}, and 0.071 ohm K^{-1} were measured for PRTs 1–4, respectively. Similar values were obtained for all other samples measured in this work. Thus, while the change in electrical resistance for PRT1 shown in the raw data of figure 3 is comparable or slightly lower than those measured for PRT2 and PRT3, its temperature rise at a fixed heating power is actually greater. The temperature change per PRT at various heating power levels is presented later in this paper for multiple measured microdevices. Uncertainty values for the electrical resistance measurements are ±0.01 ohm and for the dR/dT are ±0.005 ohm K^{-1}. For all measured PRTs across all samples, dR/dT calibrations were linear to within a coefficient of determination (COD, also known as R^2) value of 0.99 or greater.

Results

The thermal characteristics of four separate microdevices were measured: one as-fabricated 'blank' microdevice with no h-BN present to serve as a control and three microdevices with h-BN thin film present. These latter three h-BN-covered microdevices are referred to as Sample 1, Sample 2, and Sample 3, respectively, in this work. For each of the three h-BN samples, Raman spectroscopy and AFM were performed after thermal testing activities were completed. Figure 4 given a representative Raman spectrum obtained from Sample 1 after being transferred to a microdevice, with spectra obtained from other samples being almost identical. The observed peak of 1369 cm^{-1} agrees with other spectra reported in the literature for crystalline h-BN [45], while the lack of additional peaks associated with defects or secondary materials is also indicative of high quality h-BN being the sole material identified as resulting from the APCVD growth. AFM was then utilized to determine the average thickness of

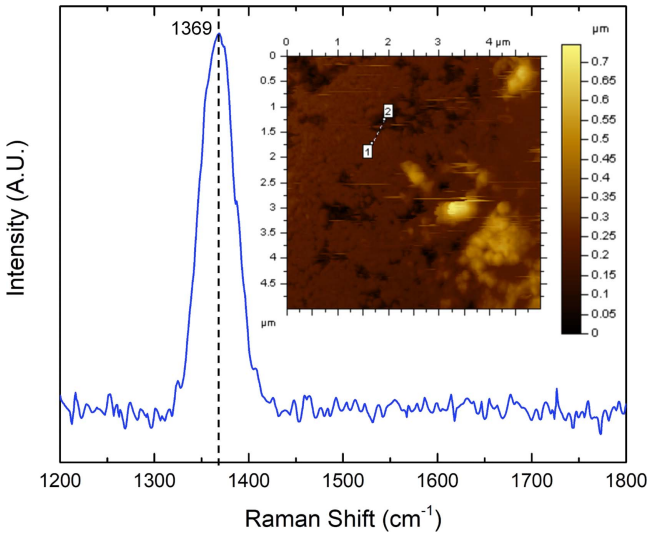

Figure 4. Representative Raman spectrum from h-BN thin film Sample 1. The peak position is consistent with h-BN. Inset: one of multiple atomic force microscopy scan taken from different regions near the outer edges of Sample 3 to determine h-BN thickness relative to the SiO_2 surface. The average thickness for this sample was determined to be 77.7 nm ± 9.2 nm.

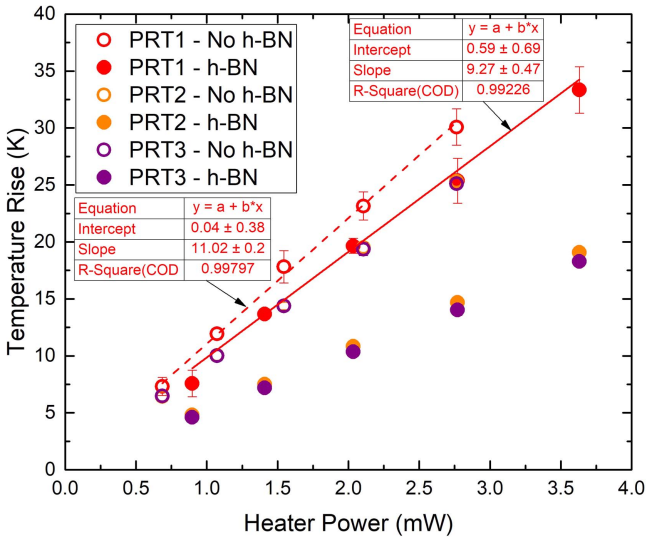

Figure 5. Steady-state temperature rise of PRT1 (heater), PRT2, and PRT3 for Sample 1 (filled symbols) and the blank microdevice (open symbols) at a temperature of 375 K. Blank microdevice data points for PRT2 and PRT3 overlap and are nearly indistinguishable. Error bars for certain PRT2 and PRT3 data points are smaller than the symbol marker used.

each of the three measured h-BN samples. This was accomplished by performing multiple AFM scans at different regions near the outer edges of each h-BN film where its height could be measured relative to an exposed portion of the SiO_2 surface. These exposed regions only existed around the outer edges of a given diced device, but did allow for thickness measurements by using the AFM similar to a profilometer to measure step height of a thin film, but with higher resolution. An example of one such scan is given in the inset of figure 4. The average thickness for the three samples were determined to be 120.1 nm ± 14.2 nm for Sample 1, 125.0 nm ± 9.6 nm for Sample 2, and 77.7 nm ± 9.2 nm for Sample 3. The intervals given here relate to statistical scatter amongst the various measured locations on each sample rather than resolution limitations of the instrument. While XRD was not performed on these three samples specifically, our previous XRD analysis [43] of h-BN from this same growth setup and procedure shows interlayer spacing of 0.344 nm on the (002) plane as calculated via Bragg's law, in close agreement with accepted values for h-BN. In addition, peaks corresponding to cubic or turbotrain structuring were not observed in XRD results.

For each T_s between 325 and 425 K, the PRTs' respective temperature rise versus heater power at steady state was determined for each of the four microdevices tested. Results for Samples 1–3 at a temperature of 375 K are given in figures 5–7, with the observed results from the blank microdevice (no h-BN present) also plotted for comparison. The data taken at a T_s of 375 K with ∼30–35 K of temperature rise is especially technologically relevant as it is this ∼100 °C–140 °C operating range which is the maximum for most modern electronics. For all plots, 'heater power' refers to the power dissipated within the four-probe region of PRT1 and which most closely approximates a transistor source/drain

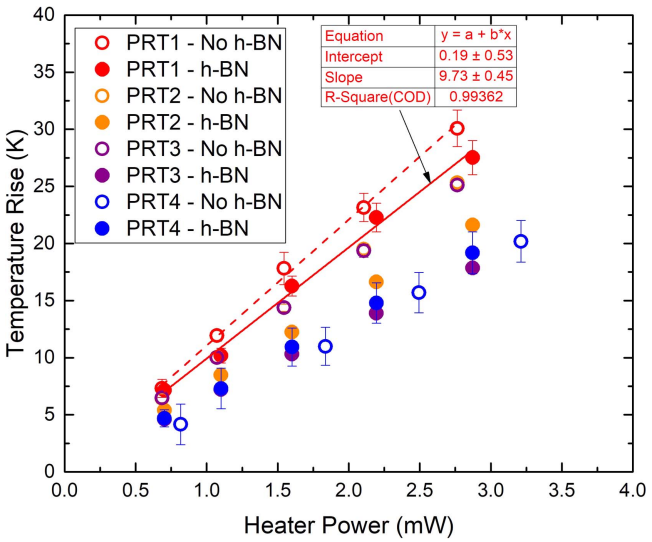

Figure 6. Steady-state temperature rise of PRT1 (heater), PRT2, PRT3, and PRT4 for Sample 2 (filled symbols) and the blank microdevice (open symbols) at a temperature of 375 K. Blank microdevice data points for PRT2 and PRT3 overlap and are nearly indistinguishable. Error bars for certain PRT2 and PRT3 data points are smaller than the symbol marker used.

contact region. Total power dissipated would include the Joule heating in the on-chip leads as well, which is considered in the numerical models presented later in the work.

Figure 5 shows the results for Sample 1 (filled symbols) plotted along with those obtained from the blank microdevice (open symbols). PRT4 for Sample 1 was found to have a broken lead line and thus four-probe resistance change measurements for it were not attainable. For PRTs 1–3, temperature was found to decrease at comparable heater power relative to the blank device, with PRTs 2 and 3 giving larger

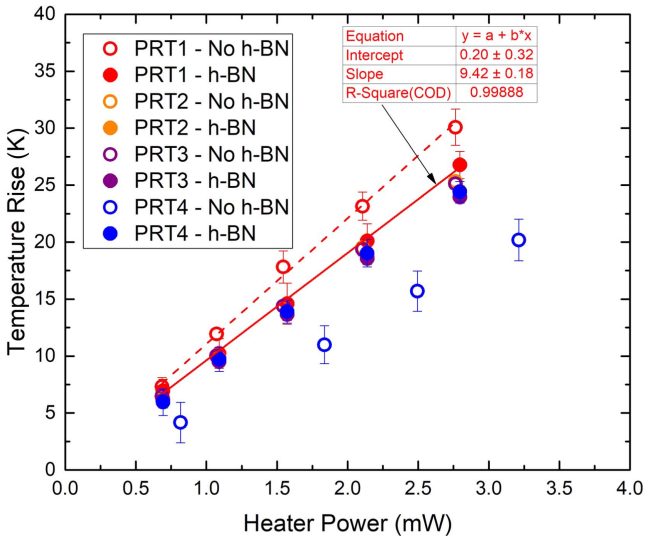

Figure 7. Steady-state temperature rise of PRT1 (heater), PRT2, PRT3, and PRT4 for Sample 3 (filled symbols) and the blank microdevice (open symbols) at a temperature of 375 K. Blank microdevice data points for PRT2 and PRT3 overlap and are nearly indistinguishable. Error bars for certain PRT2 and PRT3 data points are smaller than the symbol marker used.

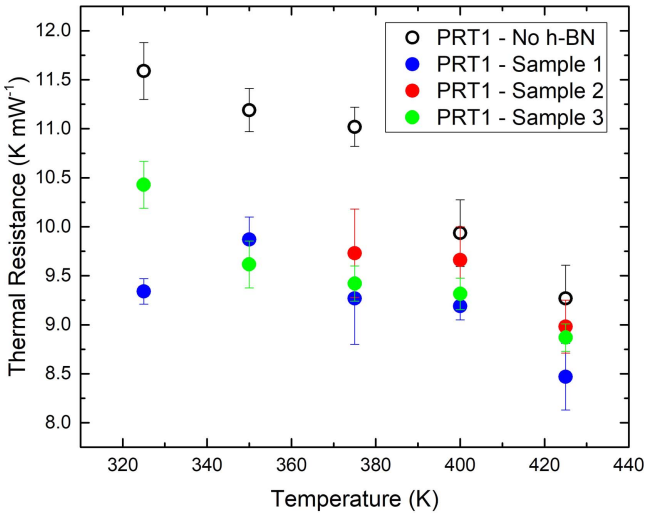

Figure 8. PRT1 effective thermal resistance for all four measured microdevices versus stage temperature.

temperature reductions compared to the heater (PRT1). This is likely due to PRT1's effective thermal resistance comprising lateral pathways for heat spreading along the surface of the microdevice as well as a pathway directly down into the SiO_2/Si substrate. Thus, the relative impact of the h-BN thin film in reducing the effective thermal resistance 'seen' by PRT1 depends not just on its ability to conduct heat independently but also on the other thermal resistances present in the system under study. More will be said on this point within the Discussion section.

The majority of previous studies into using h-BN or graphene for heat spreading in electronics applications have reported results in terms of temperature reduction at a specific power or power density. This makes comparison between studies difficult due to differences in heater design and data reported only at a singular, fixed power level. Here we propose that the effective thermal resistance of a given system—i.e. the slope of the temperature rise of the heat source versus power dissipation—is a more indicative metric for heat spreader performance as it allows temperature reduction to be scaled according to power dissipation. In order to quantify this important metric, linear fits to the PRT1 data for the blank device as well as Sample 1 are plotted in figure 5 and used to determine the effective thermal resistance for each case. These values were found to be 11.02 $\pm$ 0.20 K mW^{-1} and 9.27 $\pm$ 0.47 K mW^{-1} for the blank microdevice and Sample 1, respectively, such that the presence of the h-BN thin film reduced the effective thermal resistance of PRT1 by 15.9% $\pm$ 4.6%.

The data for Samples 2 and 3 at a substrate temperature of 375 K are plotted in figures 6 and 7, respectively. Sample 2, which was of comparable thickness to Sample 1 as revealed via the AFM measurements, demonstrated a PRT1 effective thermal resistance of 9.73 $\pm$ 0.45 K mW^{-1}, which is within the uncertainty interval overlap for Sample 1 but measurably lower than the blank microdevice value. Sample 3, despite being the thinnest of the three samples measured, demonstrated a PRT1 effective thermal resistance of 9.42 $\pm$ 0.18 K mW^{-1}, comparable to that of Samples 1 and 2. In addition, while Samples 1 and 2 showed distinct temperature decrease in PRT2 and PRT3 temperatures compared to the blank microdevice at the same power dissipation, Sample 3's temperature distribution was much more spatially uniform.

Data taken at other stage temperatures for the four measured microdevices were similar in terms of magnitude and linearity to what is depicted figures 5–7, but with differences in slope. Rather than plotting the twenty data sets individually, the temperature dependence of each h-BN sample's heat-spreading performance is most efficiently illustrated by plotting the PRT1 effective thermal resistance versus temperature T_s as given in figure 8. The effectiveness of the h-BN thin films in reducing thermal resistance is most notable between 325 and 375 K, where the average *reduction* in PRT1 effective thermal resistance is 1.86 $\pm$ 0.32 K mW^{-1}. This represents an average reduction in effective thermal resistance of approximately 16.5% $\pm$ 2.8% relative to the blank microdevice. At higher temperatures, the h-BN thin films become less adept at reducing the effective thermal resistance compared to the blank microdevice, with the values becoming closer and uncertainty intervals of one or more h-BN-covered microdevices overlapping those of the blank microdevice.

Discussion

The experimental results presented here demonstrate that h-BN thin films grown via APCVD can be effective in reducing thermal resistance of a heat source similar to those encountered in modern electronics. Now we seek to gain further insight into the important factors that influence

performance of said thin films, identify future paths for improvement, and discuss their viability in industrial settings.

First, the temperature dependence of PRT1 effective thermal resistance shown in figure 8 indicates that the thermal pathways present within the microdevices change in relative magnitude and importance with temperature. These changes are related to the temperature-dependent thermal conductivities of the Si substrate, SiO_2 insulating layer, and h-BN thin films. While both h-BN and Si have thermal conductivity that decrease with increasing temperature within this range of operation due to increasing phonon–phonon scattering, the amorphous SiO_2 has thermal conductivity that increases with increasing temperature while still being roughly two orders of magnitude smaller ($\sim$1.3–1.4 $W\,m^{-1}\,K^{-1}$ [46]) than the values associated with Si and bulk h-BN. Along the top plane of the device where the PRT is situated, the SiO_2 and h-BN thin film (when present) represent a fin-like situation in which the ratio of heat that is conducted within the plane versus that which is conducted into the substrate at any given distance from the heater line depends on the thermal resistances in each direction. The relatively low thermal conductivity SiO_2 layer thus strongly affects thermal resistance in both directions, and, in turn, the effective total thermal resistance seen by the PRT. As a result, even a modest increase in the SiO_2 thermal conductivity with temperature would allow additional heat conduction across the 1 μm film thickness and into the Si substrate. Thus, as temperature increases, the in-plane heat spreading enhanced by the presence of h-BN gradually become less influential and thermal conduction into the substrate dominates, hence the apparent converging of data seen in figure 8.

In reality, the qualitative fin analogy employed above is not entirely applicable. The geometry and experimental conditions associated with this microdevice are more complex than can be effectively handled via a simple analytical 1D or 2D fin model. Besides needing to account for three-dimensional conduction in a multilayer system, the heat generated within the lead lines connected to the four-probe heating region of PRT1 must be taken into account. Thus, a numerical simulation approach is required to better understand these results. The extraction of the in-plane κ of each of the APCVD-grown h-BN film samples is of particular interest. The κ of CVD-grown thin films such as h-BN and graphene is strongly affected by the grain size and quality of the material, which in turn is directly related to the growth process and conditions [47, 48]. Thus, knowledge of the κ of the h-BN films studied here can be used as a measure of sample quality and determine if further improvements in κ are possible via modified CVD growth. The use of numerical simulations to compliment experimental data and extract κ values has previously proven successful in studying thermal transport in graphene [16, 18].

With the heat generation and resulting on-chip temperature distributions known via the conducted experiments, the κ of each h-BN thin film sample was extracted through numerical simulations. A finite element model was built using ANSYS finite element analysis software with the same geometry as the microfabricated devices. A full description of the modeling approach employed including physical parameters used for all materials, temperature dependence, and method for matching temperatures is given in supplementary information is available online at stacks.iop.org/NANO/28/505705/mmedia. Briefly, a symmetry plane was used to reduce computational expense and for simplicity, reducing the domain to half of the actual experiment. The boundary conditions for the finite element analysis were defined based on the experiment, i.e. a fixed substrate temperature at the outer boundaries while an adiabatic boundary condition was applied on the symmetry plane. The volumetric heat generation rate measured within the four-probe region of the heating PRT for each specific experiment was applied to the corresponding feature of the simulation, while heating within the leads was applied via scaling according to each line's width. Finally, the κ of the h-BN film under study was adjusted via trial-and-error until the temperature at each PRT matched that measured by the corresponding PRT in the experiment. Representative temperature contour results are shown in figure 9. Note that inclusion of heating within the leads on the left induces a complex distribution that would be difficult to capture with an analytical model or a simplified computational domain that neglected these effects. From these simulations, κ values of 18.0–21.3 $W\,m^{-1}\,K^{-1}$, 13.7–15.1 $W\,m^{-1}\,K^{-1}$, and 62.9–77.4 $W\,m^{-1}\,K^{-1}$ were determined for Samples 1, 2, and 3, respectively. These ranges include both microdevice measurement uncertainty intervals and variation in h-BN thin film thickness outlined above in the discussion of AFM measurements.

As noted in the Introduction, bulk h-BN has in-plane κ of 350 $W\,m^{-1}\,K^{-1}$ at 300 K [25], while CVD-grown h-BN 10–20 nm thick has been reported with in-plane κ value of about 100 $\pm$ 10 $W\,m^{-1}\,K^{-1}$ [41]. In comparison, of the APCVD h-BN thin films measured here Sample 3 showed the most comparable κ of 62.9–77.4 $W\,m^{-1}\,K^{-1}$. We attribute the lower κ values found here compared to these works to defects and/or small grain size within the h-BN thin films, which are themselves directly related to the APCVD process. The strong influence of grain size on κ in CVD-derived van der Waals materials has recently been demonstrated by Lee *et al* where a $\sim$4$\times$ difference in κ was experimentally observed in CVD-derived graphene with grain sizes from 0.5–4.1 μm near 325 K [47]. Mortazavi *et al* have calculated κ of polycrystalline h-BN sheets for different grain sizes at 300 K [48] and a similarly strong dependence was reported. The average grain size for each h-BN thin film sample grown in this work was estimated by comparison with their results. The average grain sizes estimated in this way are $\sim$2 nm for Sample 1, $\sim$1.5 nm for Sample 2, and $\sim$6 nm for Sample 3. Thus, one possible avenue for improving h-BN heat spreader performance is to improve the CVD process and, as a result, obtain films with larger grain size and high κ. The relationship between CVD parameters and grain size for h-BN has been presented previously by Tay *et al* [49] amongst others.

Besides small grain size, another factor which is often cited as limiting vdW-based materials' thermal transport properties is interfacial thermal resistance with the underlying substrate. However, as recently pointed out by Choi *et al* in

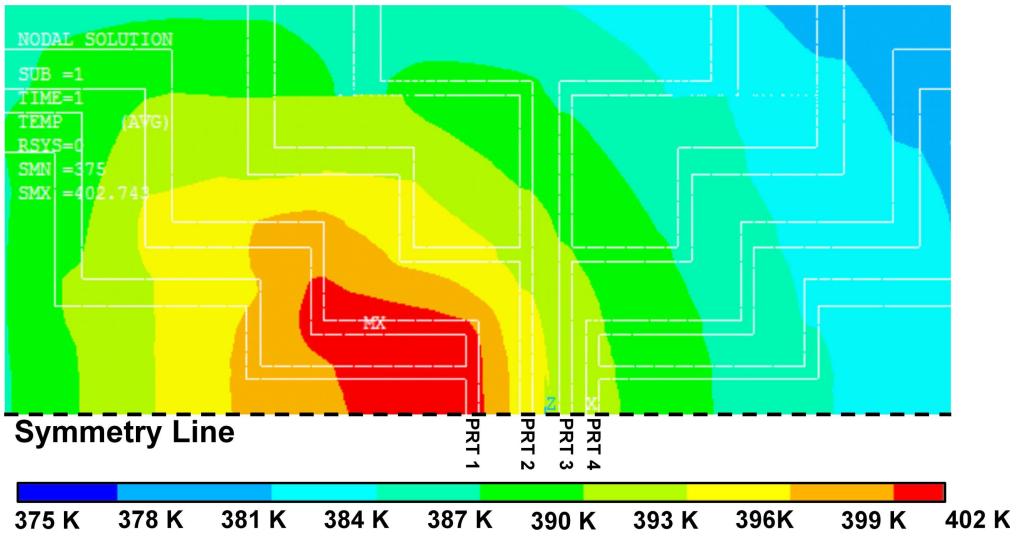

Figure 9. Temperature contour details from an ANSYS finite element model that replicates the microdevice experiments and allows for estimation of the h-BN thin film thermal conductivity by matching the PRT-measured temperature distribution at the same heat generation used in a given experiment.

their study of self-heating graphene, the interfacial thermal resistance may only be a limiting factor in the case of a very thin insulating dielectric layer [50]. Specifically, this condition is only true if the ratio of interfacial thermal conductance (G_{int}) to oxide layer thermal conductance (G_{oxide}) is less than about 5. If this ratio is large, then modification of G_{int} by chemical functionalization or other methods may have little or no positive impact on heat transfer. For our case, G_{int} is found by taking the inverse of the measured interfacial thermal resistance for h-BN/SiO_2 of $3.4 \times 10^{-8}\,\text{m}^2\,\text{K}\,\text{W}^{-1}$ from literature [51]. This gives $G_{\text{int}} = 2.9 \times 10^{7}\,\text{W}\,\text{m}^{-2}\,\text{K}^{-1}$. The oxide layer thermal conductance $G_{\text{oxide}} = k_{\text{oxide}}/t_{\text{oxide}}$, where t_{oxide} is the oxide layer thickness and κ_{oxide} is its thermal conductivity. Using the 1 μm oxide thickness for our microdevices and literature values for thermal conductivity of SiO_2, the result is $G_{\text{oxide}} = 1.4 \times 10^{6}\,\text{W}\,\text{m}^{-2}\,\text{K}^{-1}$. Thus, for our case $G_{\text{int}}/G_{\text{oxide}} = 21.8$ which indicates that the interface thermal resistance between the h-BN and SiO_2 is not a limiting factor compared to the conduction resistance of the SiO_2 itself. Thus, if the oxide layer cannot be significantly thinned due to electrical isolation requirements, emphasis should be put on improving κ through h-BN synthesis modifications.

Finally, we consider the use of h-BN thin films as near-junction heat spreaders in industrial applications. First, the reduction in thermal resistance seen in these measurements translates to significant improvements in electronic device lifetime. For example, for a GaN HEMT operating at 150 °C, the ~5 °C reduction in temperature observed at the highest powers tested in this work and shown in figures 5–7 would represent a factor of 3 improvement in device mean time to failure [52]. This improvement may even be greater with proper power scaling of the temperature reduction via the effective thermal resistance or improvements in h-BN κ. Another important point to note is that the experiments reported here were conducted within a vacuum environment. If this experiment were implemented in an environment more typical of commercial usage such as in air, encapsulated within an epoxy, or covered by multiple layers of insulating and metal interconnects, additional avenues of heat transfer would be available in parallel and in series to the h-BN, which could help or hinder its performance depending on the specific details of the integration architecture. Specifically, scenarios by which the fin effect is enhanced (air exposure, for example) could lead to superior performance, whereas scenarios with inherently efficient in-plane heat conduction networks (such as high metal content interconnect layers) might make the h-BN's presence ineffective in enhancing an already highly conductive device.

As mentioned in the Introduction, CVD-based methods already offer strong scalability and cost benefits compared to other forms of producing electronics integration-compatible thin films. As a result, if further advances in CVD-based growth of high quality, large-grained h-BN can be made without reducing yield or significantly increasing cost, h-BN thin films have strong potential to serve as an economically viable means of achieving direct contact near-junction thermal management of individual electronic devices.

Conclusion

In this work, the viability of using large area, continuous h-BN thin films as direct contact, near-junction heat spreaders for electronic devices was demonstrated. Continuous h-BN thin films were synthesized via a simple APCVD method and subsequently transferred onto a microfabricated test device that simulated a multigate transistor. Results showed that:

1. APCVD h-BN thin films with thicknesses of 77–125 nm are capable of significantly lowering microdevice temperatures and the effective thermal resistance of said devices, with the best sample showing

the presence of the h-BN thin film reduced the effective thermal resistance by 15.9% ± 4.6%.

2. The effectiveness of h-BN heat spreaders is both temperature- and device/design dependent. At temperatures of 400 K and above, the effectiveness of the h-BN thin films to reduce thermal resistance relative to blank microdevice results was diminished due to changes in constituent material thermal conductivity. In addition, it was shown that for this specific microdevice that the interfacial thermal resistance is not a limiting factor in heat spreader performance but that this is not necessarily true for all cases.
3. Through finite element simulations, the in-plane thermal conductivity of each h-BN thin film sample was determined and found to be significantly lower than bulk h-BN and comparable or lower than values associated with CVD h-BN. The correlation of thermal conductivity values with grain size suggests these APCVD-synthesized samples have grain sizes of 1.5–6 nm and that improvements in film quality via changes in synthesis procedure could lead to improved heat spreader performance as well.

Besides underscoring the need to improve the grain size/quality of CVD-derived h-BN materials, this work also highlights how the results of this work apply to the potential use of h-BN thin films in industrial/commercial settings in terms of differing environments, scalability, cost, and impact on device reliability.

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