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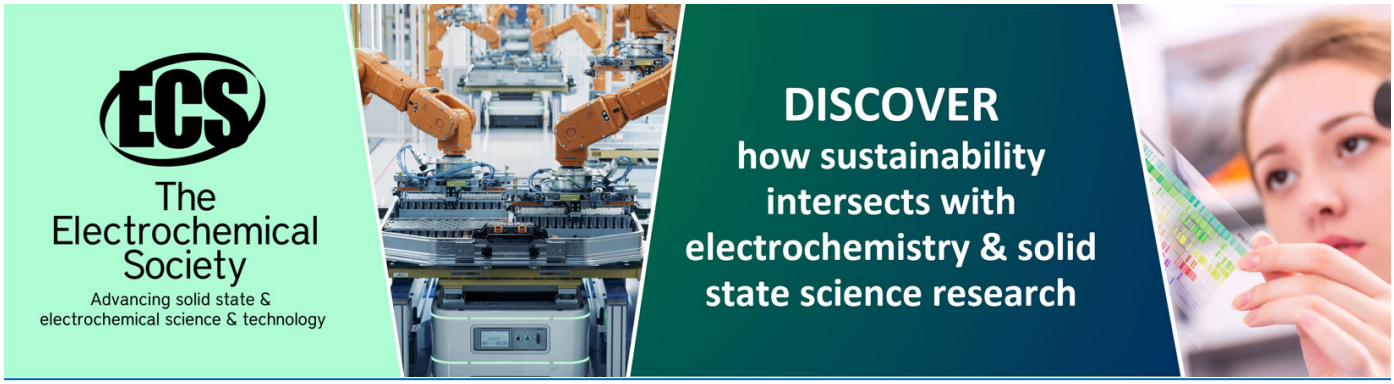

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A low-temperature parylene-to-silicon dioxide bonding technique for high-pressure microfluidics

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Abstract

We introduce a new low-temperature (280 °C) parylene-to-SiO_2 bonding process with high device yield (>90%) for the fabrication and integration of high-pressure-rated microfluidic chips. Pull tests demonstrate a parylene-to-SiO_2 bonding strength of 10 ± 3 MPa. We apply this technique for bonding Pyrex and silicon wafers having multiple metal layers to fabricate standard packaged microfluidic devices. By performing electrochemical impedance spectroscopy of electrolyte solutions in such devices, we demonstrate that electrodes remain functional after the etching, bonding and dicing steps. We also develop a high-pressure microfluidic and electrical integration technology, eliminating special fluidic interconnections and wire-bonding steps. The burst pressure of the integrated system is statistically shown to be 7.6 ± 1.3 MPa, with a maximum achieved burst pressure of 11.1 MPa, opening perspectives for high-pressure applications of these types of microfluidic devices.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The improvement of detection sensitivity and analysis time has been a key motivation for the development of analytical microsystems. Many studies have presented biomedical and chemical applications based on microsystem technology, like electrical and optical cytometers [1], HPLC devices [2–4], and other chromatography instruments [5–11]. Moreover, the size reduction results in reduced processing volumes (1 pL to 1 nL), possibly compromising an assay's detection limit and throughput, especially for low flow rates (50 nL s^{-1}) [1]. The latter are limited by the maximum allowed pressure for reliable operation and integrity of the microfluidic device. When the increasing fluidic resistance due to size reduction and the demand of higher flow rates for maximizing throughput are considered together, the need for high-pressure microfluidic systems is evident.

A number of fabrication methods for high-pressure microfluidic applications have already been introduced in the literature [12]. One is the injection moulding of cyclo-olefin copolymer (COC) devices and the cyclohexane-based bonding into devices that can withstand up to 34.6 MPa [13]. However, integration of micro-machined metals with low feature size has not been demonstrated until now. In addition, the channel dimension non-uniformity is large (up to ±3 μm) for low feature-size channels and tooling costs are high. Glass–glass fusion-bonded devices withstanding up to 34.0 MPa have also been demonstrated [14]. One can use conventional fusion or anodic bonding techniques for high-burst pressure microchannels, but electrode integration is challenging, as the bonding interfaces are composed of refractory materials and the induced topography changes do not tolerate proper bonding [15]. Alternatively, bonding glass or silicon wafers with polymer glue is possible, even in the presence of topography, as the polymer layer is elastic and/or can be easily heated above its glass transition temperature. Polymers may be permeable to gases like CO_2 and H_2, which is a drawback for hermetic packaging but useful for many biomedical applications [16]. Unfortunately, maximum reported working pressures with such polymer glue-bonded

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Table 1. Comparison of burst pressures reported in the literature for different bonding techniques.

Reference	Maximum burst pressure (MPa)	Mean (± st. dev) of burst pressure (MPa)	Material and bonding method	Bonding temperature (°C)
Mair *et al* 2007 [13]	34.6	18 (±5)	Cyclohexane solvent-mediated bonding of two COC injection moulded parts	Room temperature
Hasselbrink *et al* 2002 [14]	34.0	20.7	Glass/glass bonding	Not reported
Metz *et al* 2004 [23]	2.0	Not reported	Polyimide/polyimide bonding by lamination	300
Yussuf *et al* 2007 [40]	N/A	1.2	PMMA/PMMA and PC/PC bonding by microwave heating of a poly-aniline interface layer	120
Mark *et al* 2008 [41]	0.69	Not reported	PDMS/PDMS bonding	Room temperature
Paul *et al* 2007 [42]	0.35	Not reported	COC/COC bonding by lamination	130

microfluidic devices are only around 2 MPa [17]. In fact, microfluidic devices with polyimide–polyimide lamination holding up to 20 MPa of pressure were also presented, but this result relied on an external macro-clamping setup. Virtually, with such external clamping, the pressures reported with most techniques could be improved, but at the cost of complex packaging. Table 1 summarizes the maximum burst pressures reported in the literature for microfluidic channels, which were defined by microfabrication techniques in a first substrate that is subsequently bonded to a second substrate. As shown, bonded glass or silicon wafers using polymer glue typically exhibit burst pressures lower than 2 MPa. If we could increase bonding strengths of polymer glues to a level of 10 MPa using a low-complexity and low-temperature bonding alternative, this would allow more affordable microfluidic applications with higher throughput, metallization and possible integration with CMOS.

An important question is the selection of the optimum polymer material to be used as glue and at the same time as channel structure. The required properties are (i) a uniform polymer film thickness for keeping the bonding yield high, (ii) choice of a low-stress polymer to enable a low feature size and to avoid cracks, and (iii) having a large bonding window, defined as the temperature range between the glass transition and melting points of the polymer [18]. In this interval, bonding is possible without melting and hence the structural features are maintained. In addition, bonding of a silicon to a glass wafer without stress can be achieved by performing bonding in a temperature window of 60 °C around the stress-free temperature of 270 °C [19]. Therefore, the polymer bonding window should also include this 'stress-free' temperature. Popular polymer bonding materials in the literature are benzo-cyclo-butene (BCB) [20–22], photo-definable polyimides and non-photo-definable polyimides [17, 23, 24], and parylenes [8, 18, 25, 26]. BCB can provide low-temperature (90 °C) bonding, but it melts during bonding, which makes small etched features in the polymer disappear. Polyimides, in contrast, can preserve their features, since bonding occurs by a glass-transition mechanism. Yet

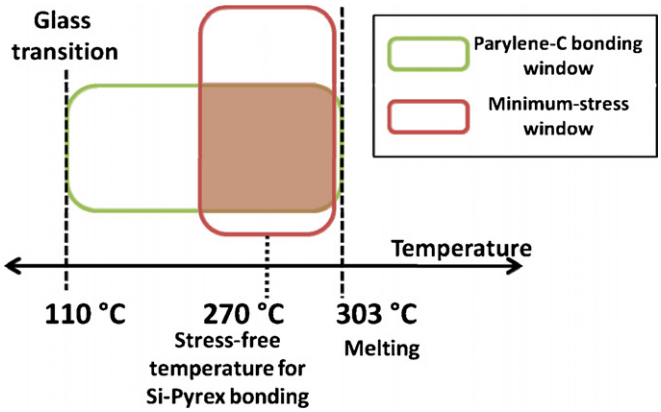

Figure 1. Compatibility of the parylene bonding temperature window with the minimum stress window for the bonding of Pyrex–silicon wafers. The temperature data are taken from [18, 19].

polyimides need spin coating and baking steps, resulting in possible film non-uniformity and void generation by curing processes due to outgassing [18].

As an alternative, the polymer parylene-C has shown the ability to perform polymer bonding based on the glass-transition mechanism [8, 18, 25, 26]. An advantage of using parylene-C is that it is vapour depositable to uniform thicknesses at room temperature, it has low stress, and it requires no thermal annealing and baking cycles [8, 18, 25–28]. Although it has a weak adherence to common solid surfaces, silanization-based surface pre-treatment can improve adhesion between polymers and polar surfaces [28]. Figure 1 shows the temperature window for the bonding operation with parylene-C [18, 19], showing that the former is nicely located around the stress-free temperature, while bonding can be performed at low temperature (<300 °C), compatible with CMOS processing. Existing low-temperature bonding methods based on thermo-compression of parylene-C resulted in bonding strengths lower than 3.8 MPa [18]. In this work, physical bonding occurred at the parylene/parylene

interface, after coating two wafers with parylene-C and bonding them by thermo-compression at 230 °C. An alternative parylene-C bonding technique based on microwave heating was also proposed [29], which also uses a parylene-C layer on each substrate, but it is a non-standard technique and metallization issues have not been addressed.

We propose a low-temperature (<300 °C), polymer/polymer interface-free parylene-C bonding that can allow fabrication of 10 MPa rated microfluidic devices. Moreover, the technique is compatible with dense and multiple metallization patterns interfacing with the microfluidic channels, which still remains a challenge when combined with high-pressure requirements. Such bonding technology can significantly improve the traditionally low throughput of fluids in microfabricated devices by allowing very high volumetric flow rates. We also focus on fast and reliable high-pressure system integration, since combining the electrical and fluidic circuits may be essential [30, 31]. Indeed, if reliable high-pressure integration can be easily combined with electrical contacting and device replacement can be facilitated, time-to-output of analytical microfluidic devices will be reduced significantly.

2. Fabrication and experimental procedure

2.1. Wafer selection

While glass–glass wafer bonding results in devices with good optical transparency, using silicon wafers is still very advantageous when highly developed silicon micromachining tools for conventional MEMS structures like deep reactive ion etching (DRIE) are considered. Therefore, we have chosen to bond a silicon to a glass wafer. Note that the whole process that is going to be explained can be performed starting from two silicon or two glass wafers, except that, for the glass–glass case, DRIE hole openings should be made by another technique like powder blasting [32, 33].

2.2. Standard methods

Before moving on with the microfabrication process, commonly used steps during microfabrication like resist stripping, deionized (DI)-water washing and lithography are explained here in detail to avoid repetition.

2.2.1. Washing. The wafers are first washed with DI-water in a quick dump rinse (QDR) bath during resistivity monitoring. The step is repeated if the resistance of water is lower than 10 MΩ. Next washing is performed in an ultra-clean (UC) bath until 14 MΩ is reached. Wafers are dried with a spin-drier system rotating at 5 krpm under N_2 environment.

2.2.2. Resist stripping. Resists are stripped by first dipping the wafer into a hot resist remover (Shipley Microposit Remover 1165, from Shipley Company, USA) at 70 °C for 12 min, and then washed. Finally, O_2 plasma (PVA Tepla 300 Microwave Plasma System) at 500 W under 400 sccm O_2 flow for 10 min is applied to remove any resist residues.

2.2.3. Standard lithography. First, wafers are spin coated using AZ 1512 HS resist (from Clariant GmbH, Germany) with a thickness of 1.1 μm at 6 krpm for 30 s. Then soft bake is done for 90 s with a hotplate at 112 °C. After alignment, the wafer is exposed at a constant lamp power of 340 W for 1.4 s. Note that the exposure duration is adjusted ±0.1 s, depending on the reflection coefficient of the film underneath the resist. The latter is developed by applying developer (Shipley microposit developer 351, from Shipley Company, USA) using a 5 s spray and a 20 s dispense protocol, followed by hard baking for 90 s on a hotplate at 112 °C. Wafers are then washed.

2.3. Microfabrication process

2.3.1. Initial steps. The fabrication flow is illustrated in figure 2. It was started with one 4 inch silicon wafer with a 1.5 μm oxide layer made by wet oxidation and one Pyrex wafer. The oxide layer on the silicon wafer prevents the direct electrical contact of the silicon to the electrodes that will be deposited. A 200 nm silicon dioxide (SiO_2) layer was also sputtered (Pfeiffer SPIDER 600) onto the Pyrex wafer, so that the dielectric and surface properties of the two substrates match. The Pyrex wafer was piranha cleaned by dipping it into the piranha solution (96% H_2SO_4, 2% H_2O_2) at 100 °C for 12 min, and then washed. Next, 200 nm Cr was e-beam evaporated (Leybold-Optics LAB 600H) onto the backside of the Pyrex wafer to provide a conductive layer for later electrostatic clamping and handling of the wafer.

2.3.2. Metallization steps. From the literature we know that platinum is inert in contact with most electrolyte solutions [34], i.e. the dissolution time in the liquid is very long, which is the reason we adopted it as an electrical contact material to the fluid. First, 10 nm Ti, 100 nm Pt and 10 nm Ti were evaporated onto both wafers. The last Ti layer is essential for adhesion of the subsequent isolating SiO_2 layer. Next, standard lithography was applied to both wafers and Ti/Pt/Ti was structured using Cl_2/Ar chemistry in a reactive ion etching (RIE) system (STS Multiplex Inductively Coupled Plasma (STS-MICP)). After this, resist was stripped and wafers were washed (see figure 2(*a*)). The following steps involve coating and patterning of an inter-metal insulation layer for forming contact holes between two metal layers, as illustrated in figure 2(*b*). 0.5 μm SiO_2 was RF-sputtered on both wafers (Pfeiffer SPIDER 600) and etched by RIE using CF_4 chemistry (STS-MICP) after standard lithography. After etching the holes in the insulating layer, the resist was stripped. Note that the layer thickness can be varied according to dielectric isolation requirements between the two metals. For the second metal layer, aluminium is favourable, since it has a high conductivity and an established process flow is available. Hence, 0.5 μm Al on top of the 0.1 μm Ti adhesion layer was deposited by dc sputtering (Pfeiffer SPIDER 600) on both wafers. The conformal nature of sputtering is good enough to form proper and reproducible contacts between the Pt and Al layers through the openings in the oxide insulating layer (metal vias). Defining of this second metal layer was performed

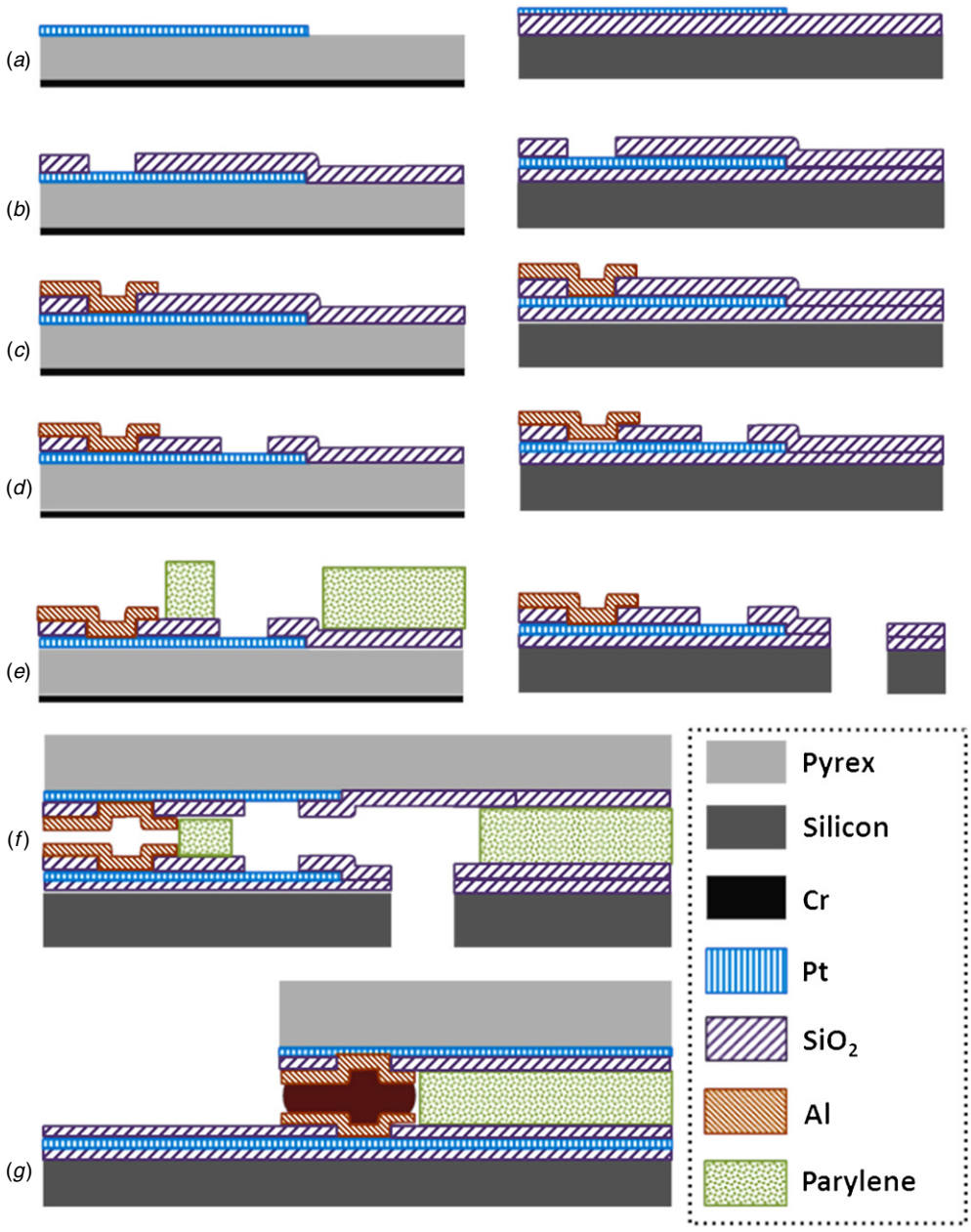

Figure 2. Processing of the Pyrex and silicon wafers, followed by low-temperature parylene-to-silicon dioxide bonding. (*a*) Evaporation of 10 nm Ti, 100 nm Pt and 10 nm Ti on both wafers as a first metal layer and patterning through lithography and RIE etching. (*b*) Sputtering of 0.5 μm SiO_2 as an insulating layer between multiple metal layers and patterning. (*c*) Sputtering of 100 nm Ti and then 0.5 μm Al as the second metal layer and shaping by RIE etching. (*d*) Opening of 'fluidic contacts' by dry etching the oxide over platinum to electrically contact the fluids. (*e*) Deposition and patterning of 10 μm (up to 20 μm) parylene using 200 nm of a sputtered amorphous silicon hard mask for the Pyrex wafer. Opening of fluidic inlets in the silicon wafer with DRIE. (*f*) Parylene-to-SiO_2 bonding. (*g*) Half-dicing to open electrical contact pads and conductive silver-epoxy filling for realizing electrical contact between upper and lower metallizations.

by standard lithography and the layers were structured using Cl_2 chemistry with RIE (STS-MICP), which was followed by cleaning the wafers, as illustrated in figure 2(*c*). In a subsequent step, standard lithography and etching (identical as in previous SiO_2 etch) were used for defining the so-called fluidic contacts, i.e. access holes in the isolation layer that later will permit electrical contact between the Pt and fluid (see figure 2(*d*)). After etching of SiO_2, the resist was stripped and the 10 nm Ti layer on Pt was removed by a Ti wet etchant. Figure 3(*a*) shows the SEM pictures of metal and contact structures at this stage of fabrication, with indication in the corresponding scheme in the fabrication flow.

2.3.3. Channel forming steps. The next processing steps involve parylene-C coating, hard masking and patterning on the glass wafer only (figure 2(*e*)). As indicated before, the native adhesion of the parylene-C films to a polar substrate is quite poor and should be improved. A conventional way is to use silanization before deposition [28]. In this method, a silicon-based self-assembled silane monolayer is formed by

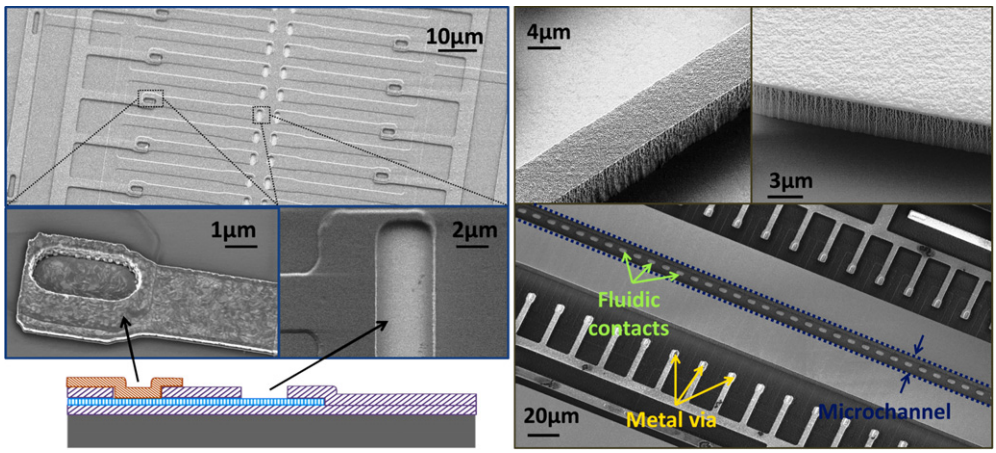

Figure 3. (*a*) SEM pictures of metal electrodes and contact openings after completion of metallization, corresponding to situation (*d*) of the fabrication flow of figure 2. (*b*) SEM pictures before bonding, corresponding to situation (*e*) of the fabrication flow of figure 2. After parylene etching, the wall profile is vertical, while no back-sputtering of the hard mask is observed.

dipping the glass substrate into a solution composed of 1% A-174 silane (Comelec SA, Switzerland), 5% water and the rest being isopropanol. This method has proven to provide strong adhesion between parylene-C and the substrate. Another adhesion promotion method is called recrystallization [35], which is a type of baking at around 300 °C after parylene-C deposition and involves multiple coating steps for obtaining thick layers. We have selected silanization due to the fact that single layer coating is enough and it avoids the temperature cycling, which is known to induce stress in parylene-C [36, 37]. After dipping the glass wafer into an A-174 silane solution, it was washed with pure isopropanol and baked in an oven kept under N_2 flow at 100 °C for 10 min.

Parylene-C deposition was done after silanization and dehydration using the Comelec Parylene Deposition system with 35.5 g of parylene-C dimer, which results in a thickness of the film of around 10 μm. Before deposition, the backside of the wafer was coated with dicing tape to prevent coating. After deposition, this tape was lifted by hand.

For selection of the hard mask for definition of the fluidic microchannels in the parylene-C layer, we preferred a 200 nm amorphous silicon film, whereas aluminium and silicon dioxide are the common choices in the literature [38]. Aluminium was not preferred here, since during removal of the hard mask, metal layers underneath may also be attacked. In addition, the literature suggests that Al redeposits itself back onto wafers during RIE processing [28]. For the silicon-dioxide case, in contrast, the compressive residual stress of an oxide film is observed to detach the parylene-C layer from the substrate after etching. Also, during the hard mask stripping, the oxide layer underneath may also be attacked. In addition, local heating during etching is more severe (which compromises transparency of the parylene-C layer) when an insulating material like SiO_2 is used. Consequently, a 200 nm amorphous silicon mask, pattered using RIE with SF_6, was used to etch parylene-C in RIE using O_2 gas. We observed that parylene-C had an etch rate of 1.25 to 1.5 μm min^{-1}, depending on the exposed area. Some of the etched channels are shown in figure 3(*b*), indicating a vertical wall profile and the absence of back-sputtered amorphous Si. The thickness of the parylene-C layer was also measured after channel definition. The thickness variation of a 10 μm thick parylene-C layer over the wafer surface was found to be $\pm$100 nm. Due to the fact that the resist layer is automatically cleaned during parylene-C RIE etch, the resist stripping process mentioned in section 2.2.2 was not needed after parylene-C deposition, thereby avoiding any reaction with the parylene-C layer.

The next processing step involves a straightforward DRIE etching for creating through-hole fluidic inlets in the silicon wafer only. This was realized using a 10 μm AZ9260 photoresist and 40 min of DRIE (Alcatel 601E) for a 525 $\pm$ 5 μm thick single-side polished wafer, after which the resist was stripped (figure 2(*e*)). We found that the effective etching rate was highly etch area dependent, the etching time increases with higher number of holes.

2.3.4. Bonding. The bonding process starts with washing both wafers to get rid of any obstacles (particles and dust) that may locally avoid bonding. Then, both wafers were O_2 plasma-treated (Tepla 300) for 15 s at 200 W under 400 sccm O_2 flow for surface activation of the parylene-C layer. Low power was chosen to prevent over-heating and extensive etching of the parylene-C layer. This plasma application corresponds to a maximum thickness reduction of 100 nm of the parylene-C layer, a number which is close to the statistical variation in parylene-C deposition. Next, wafers were aligned (Süss Microtec MA6 & BA6, Mask & Wafer Aligner, approximately $\pm$0.5 μm accuracy) and bonded with Süss SB6 Substrate Bonder. It is critical to start bonding within 1 h after O_2 plasma surface activation, or the activation step has to be repeated. The bonding was performed at 280 °C for 40 min with a force of 800 N for 4 inch wafers. The detailed temperature-bonding pressure graph of the realized bonding process is given in figure 4 and typically bonded wafers comprising 44 microfluidic devices have 90–95% of yield.

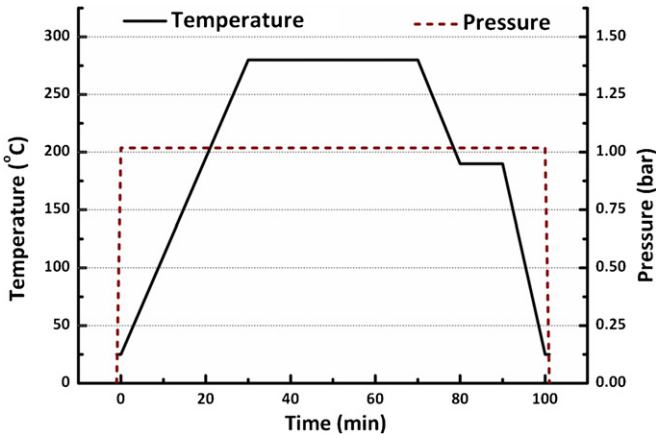

Figure 4. Bonding temperature and pressure conditions for the low-temperature parylene–SiO_2 bonding process.

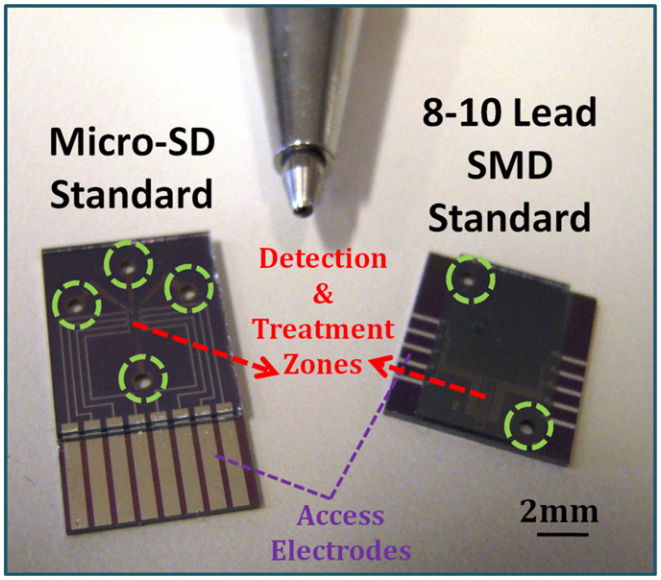

Figure 5. Photographs of finalized devices in micro-SD card standard and eight-lead SMD device footprint standard.

3. Device preparation and system integration

The devices were diced (Disco–Dad 321) with a resinoid blade (25 krpm, 1 mm s^{-1} dicing). At the same time, metal contact pads were opened by half-dicing the bonding stack, by only cutting the Pyrex part at the contact pad areas. In order to realize a contact between the top metals on the Pyrex part and electrode pads on the silicon part, a conductive epoxy was filled by capillary forces into predefined cavities, as illustrated in figure 2(*g*). A photograph of finalized devices in the micro-SD card standard and the eight-lead SMD device footprint is shown in figure 5.

For integration purposes, a PMMA adapter, connecting the microfluidic device with commercial HPLC fittings, was made using classical machining tools. Devices are mounted by simply squeezing them between a printed circuit board (PCB)

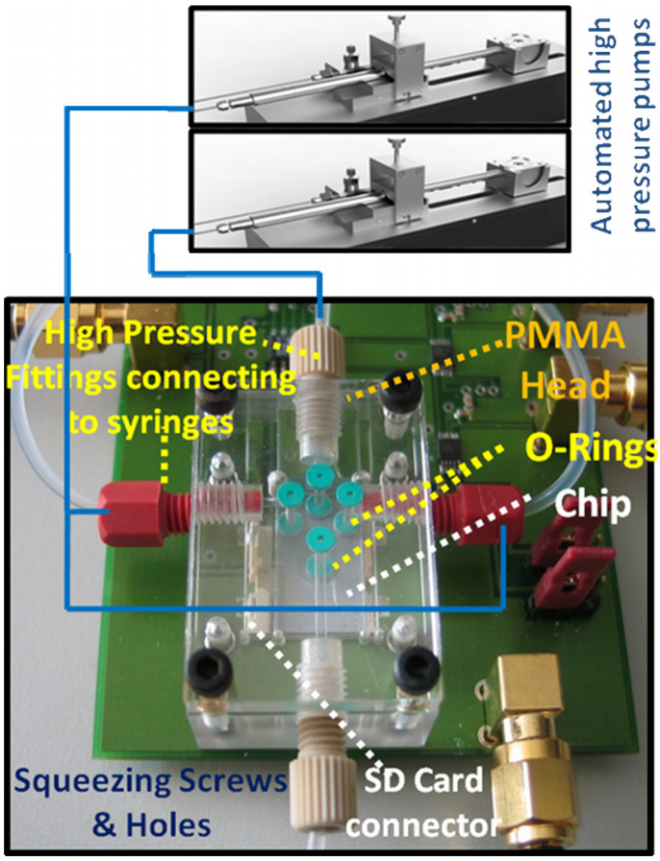

Figure 6. Illustration of device integration, indicating parts of electrical and microfluidic circuits together with the PMMA adapter, which is compatible with commercial microfluidic fittings and tubing.

and the PMMA adapter by mechanical screws. Fluidic inlets were interfaced with the PMMA adapter via sealing o-rings, while electrical connections are simultaneously realized with the PCB. A photograph of an integrated system is shown in figure 6.

All fluidic connections were made by screwing standard UNF $\frac{1}{4}-28''$ connectors and using $1/16''$ PEEK® tubing (UpChurch Scienfic) having 160 μm inner-diameter. PEEK tubing is hard enough to prevent swelling in the required pressure range (rated up to 48.3 MPa by manufacturer). 20.7 MPa rated fluidic fittings were used to connect the PMMA adapter and the PEEK tubing. We used a high-pressure metal syringe controlled by a NeMESYS® automated pump structure. The high-pressure metal syringe with 2.5 mL volume (Harvard Apparatus, USA), which can generate up to 25.0 MPa pressure, was used to induce the main flow. The overall pressure of the system was monitored with a sensor integrated with the NeMESYS® syringe pump (Cetoni GmbH, Germany) structure. Such an integration scheme has the advantage that utilization of special microfluidic interconnections is prevented, which avoids post-fabrication processes as well as wire bonding. In addition, the devices can be replaced without disconnecting any of the (high dead volume) connections in less than a minute.

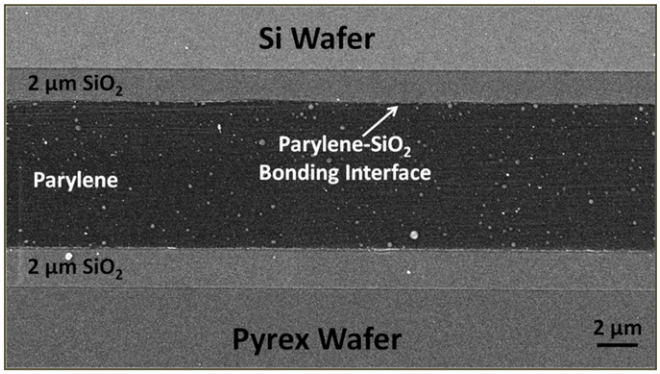

Figure 7. SEM image of a cross-section of the bonding stack and the parylene–SiO_2 bonding interface.

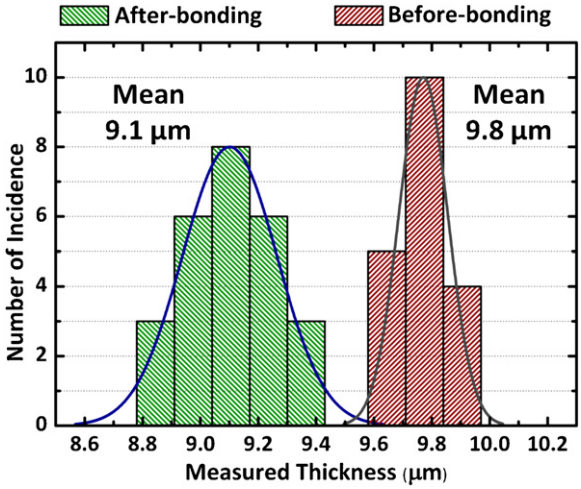

Figure 8. Histogram of parylene-C thickness measurements before and after the bonding, obtained from cross-section observations. Before bonding, measurements indicate a thickness of 9.77 ± 0.07 μm, while after bonding a thickness of 9.10 ± 0.16 μm is observed, corresponding to a 7% thickness reduction on average.

4. Results and discussion

4.1. Cross-sectional observation and thickness measurements

In order to observe the bonding interface, cross-sections of the bonding stack were realized by dicing the wafers as described above, followed by polishing and thermal evaporation of a 20 nm thick carbon layer for SEM observation. Figure 7 shows a SEM image, showing the parylene-C/SiO_2 bonding interface together with top and down oxide layers. We can observe that the parylene-C/SiO_2 bonding interface is not different from the SiO_2 interface onto which parylene-C was vapour deposited (interface at the opposite site). Note that the bright spots on the parylene-C are Al particle residues from the polishing paper.

Figure 8 shows a comparative histogram of parylene-C thickness measurements before and after the bonding, obtained from cross-section observations. These values are obtained using three different samples and for different cross-sections located at 26 different points along a distance of 1 cm. The full lines in figure 8 indicate Gaussian curve best fits, with a mean of 9.10 μm and a standard deviation of 0.16 μm after the bonding. When compared to thickness measurements of as-deposited parylene-C layers for wafers of the same batch (mean of 9.77 μm and standard deviation of 0.07 μm) we can conclude that there is a 7% thickness decrease during the bonding process.

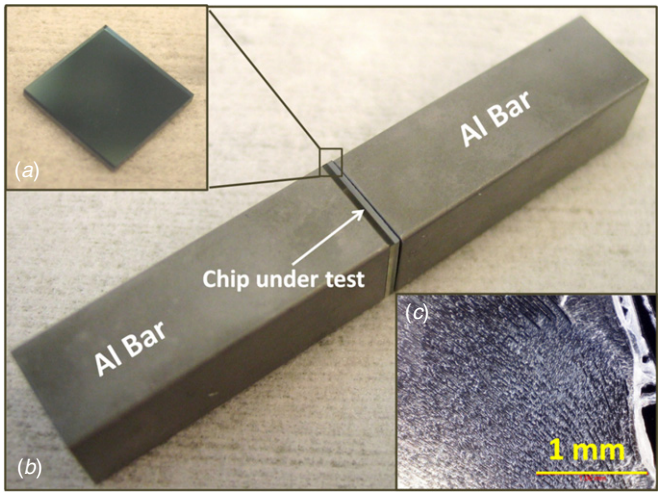

Figure 9. Samples prepared for pull-testing. (*a*) 95 mm^2 size parylene–SiO_2 bonded sample without etched features. (*b*) Assembly of sample with aluminium pulling bar. (*c*) Optical microscope image of the fractured interface after pull-testing. In general, fracture occurs in the form of cracks in the parylene layer.

4.2. Bonding strength measurements

To perform the pull tests, the wafers were bonded, as described before, but without any feature etched in the parylene-C layer; instead, the bonded wafers were diced in square pieces with dimensions of 10 mm by 10 mm (see figure 9(*a*)). In fact, due to the 0.25 mm blade thickness of the dicing machine (Disco Dad 321), the area of a die was approximately 95 mm^2 instead of 100 mm^2. Then, aluminium pulling bars (10 mm × 10 mm × 30 mm) were used to fix the dies to the pull-test equipment (see figure 9(*b*)). For this, a two-part Araldite 2010 Epoxy was mixed 1:1 (1.5 g each) for 1 min at room temperature. Then, the mixed epoxy was applied to the metal bars and die surfaces, and the parts were aligned. Hereafter, the epoxy was cured for 3 h at 70 °C in an oven, a temperature low enough not to affect parylene-C properties.

The tests were performed in a Zwick 100 kN electromechanical computer-controlled universal testing apparatus (Zwick GmbH, Germany) with 0.1 mm min^{-1} pull rate and the force was recorded via a computer-controlled interface. After mounting the sample, the force and torque were automatically adjusted to ensure that the pull force was perpendicular to the die surface. With constant pull rate, the fracture point was calculated by the data point where the observed force suddenly decreases. Then, this force is divided by the die area (95 mm^2, as previously calculated) to find the bonding strength. Figure 10 shows the histogram of the

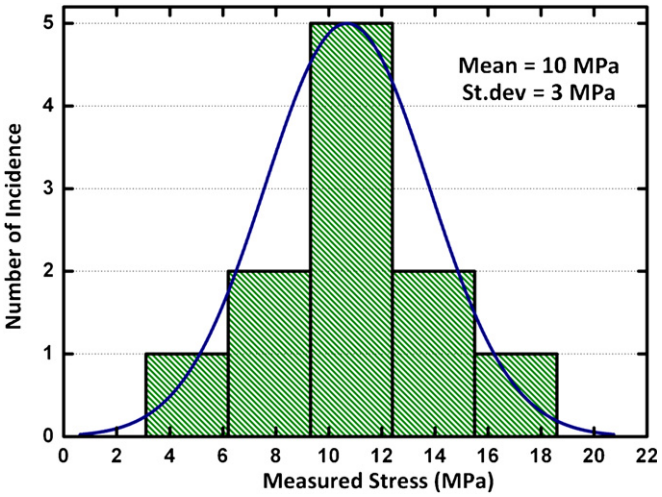

Figure 10. Results of the pull-test measurements. Histogram of the measured bonding strength and fit to a Gaussian curve, indicating a mean bonding strength of 10 MPa with a standard deviation of 3 MPa.

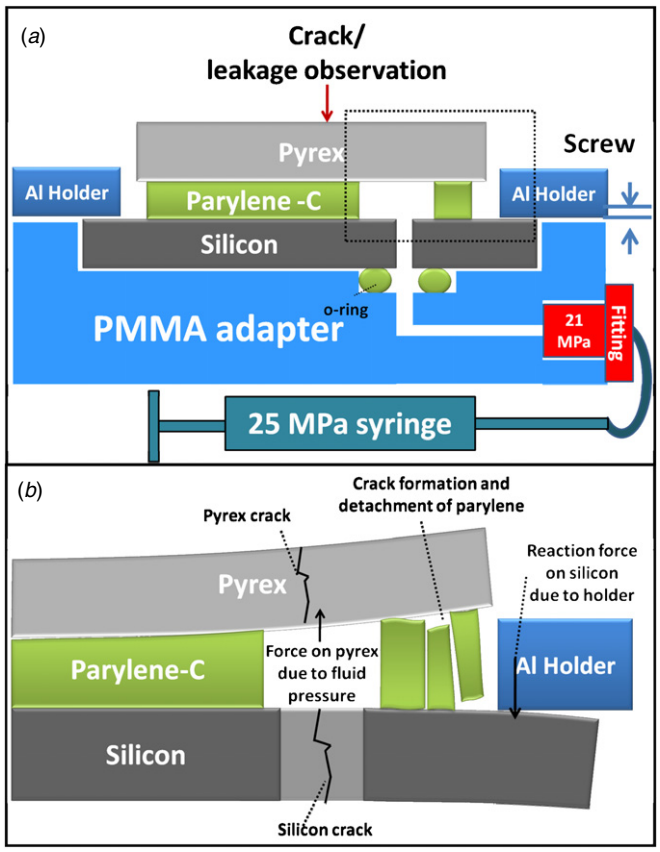

Figure 11. Schematic of (*a*) the burst pressure measurement setup, where the Pyrex part of the device is neither clamped nor assembled by any force other than that due to the parylene–SiO_2 bonding process. (*b*) Schematic indication of possible burst pressure failure events, which can occur either in the parylene layer, or in the Pyrex or silicon parts.

pull-test measurements, indicating that such bonding of parylene-C to SiO_2 demonstrates a mean strength of 10 MPa with a standard deviation of 3 MPa. The statistical variability of the measured bonding strength is possibly due to a non-uniform pressure distribution at the interface during bonding. Indeed, the non-uniformity of the parylene-C thickness (measured to be $\pm$100 nm) results in deviations of the locally applied pressure at the interface and, hence, certain areas will have more intimate bonding than others. In addition, while not always preventing bonding, nanometer size particles and dust may have an effect on the bonding strength.

Figure 9(*c*) shows a light microscope image of a fractured interface, where the parylene-C is seen to be detached under formation of cracks. The fracture patterns were observed equally on the bonding interface and the vapour deposition interface, implying that both interfaces are equally strong after the bonding process. This suggests that the oxygen plasma treatment of the parylene-C layer before bonding generates carbon radicals and C–O linkages on the parylene-C surface [39], which convert to strong bonds during the 280 °C heating step, similar to siloxane bond formation in a silanization process.

The novelty of our process is that bonding between Pyrex and silicon wafer with electrodes was achieved by coating only one substrate by parylene-C. In our process, bonding occurs between a parylene-C layer that is vapour deposited onto the Pyrex wafer and a SiO_2 layer deposited on the silicon substrate, as shown in figure 2(*f*). In contrast, the literature suggests that, to perform parylene-C bonding, both of the substrate surfaces should be coated with parylene-C [8, 18, 26] and bonding occurs physically at the parylene/parylene interface by polymer chain entanglement. Previously, it has also been reported from pull-tests that the bonding failure occurs at the parylene/parylene interface [18], at 3.8 MPa. Instead, our work demonstrated a significant increase to 10 MPa in the bonding strength, when compared with state-of-the-art parylene-bonded structures, which probably can be explained by the absence of a polymer/polymer interface in the bonding stack and the strong siloxane-like linkages of the oxygen plasma activated parylene-C to the SiO_2 surfaces. Here, the bonding strength is higher, which implies higher burst pressures in microfluidic channels, as tested by experiment in the next section.

In addition to the improvement of bonding strength and burst pressure, performing bonding with a single parylene-C layer has a number of advantages. First of all, since one of the wafers does not need to be coated and processed other than in a short oxygen plasma, the low-stress packaging of suspended MEMS structures with electrodes can be easily realized at low temperature. Such a packaging can be a low-temperature alternative that allows the realization of metal interconnects through the bonding interface, in contrast to anodic bonding where high temperature and voltage are required to directly bond glass to silicon. The technique can also be exploited in 3D device integration and integration of microchannel cooling systems for electronics. In addition, the advantage of easier processing is evident when structural features are to be realized in parylene-C. Moreover, when creating microfluidic channels with the existing bonding method based on a double parylene-C layer, channel geometry distortions can occur

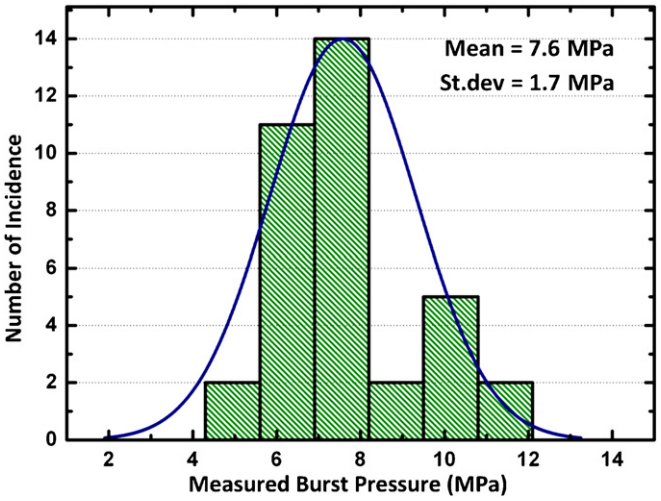

Figure 12. Results of the burst pressure measurements. Histogram of the measured burst pressures and fit to a Gaussian curve, indicating a mean bonding strength of 7.6 MPa with a standard deviation of 1.7 MPa.

due to bonding alignment mismatches (± 1 μm) in small featured channels (10 μm), which may be important for some applications, where the channel geometry is critical.

4.3. Burst pressure measurements

For burst pressure experiments on microfluidic devices comprising channels and electrodes, the devices were squeezed with a thick aluminium frame as shown in figure 11(*a*). The Pyrex part of the bonding stack did not have any support from an external clamping structure, so the integrity of the device solely relies on the bonding properties of the parylene-C layer. The high-pressure syringe was filled with DI-water, which was degassed by leaving it under vacuum at least 12 h prior to the experiments. After filling the microchannels with fluid, a clogging part was installed at the microfluidic system exit in the PMMA adapter. The high-pressure syringe was configured to increase the pressure at a rate of 0.01 MPa s^{-1}, as observed by a digital sensor at the entrance of the PMMA adapter inlet. During experimentation, the devices were observed for failures with a Zeiss Imager non-inverted A1m microscope (Zeiss AG, Switzerland) through a CCD camera (Hamamatsu ORCA-ER, Hamamatsu Photonics, Japan). Pressure and video data were simultaneously recorded with a computer. The moment just before the occurrence of a sharp pressure decrease defined the burst pressure. Figure 12 shows the histogram of the measured burst pressures for 36 devices. The results indicate that the burst pressure of the realized process has a mean value of 7.6 MPa with a standard deviation of 1.7 MPa. The statistical variations in the burst pressure can be explained by the variability of the bonding strength over the wafer. In addition, the minimum measured burst pressure was 5.0 MPa, while the maximum was as high as 11.1 MPa. When compared with the reported maximum pressure of 2.0 MPa [17] found for microchannels realized by polyimide/polyimide lamination, our results indicate that there is a 150% increase for the minimum and 270% increase for the average burst pressure.

For devices with a measured burst pressure below 8 MPa, we observed that the parylene-C has failed due to cracks propagating from the edge of the device where large inlet openings are placed, as shown in the video sequence images of figures 13(a_1)–(a_6). This can be explained by the fact that the pressure-induced force on interfaces between parylene-C and SiO_2 is maximum at places where the large area inlet openings are located. We also observed that crack patterns propagate from the right to the left in figure 13(*a*), which can be understood by the increased displacement of the Pyrex lid at the edge, as illustrated in figure 11(*b*). In contrast, in devices where the bonding strength is high enough to withstand the force generated by the high-pressure inlet, device failure occurs by development of a crack in the silicon or Pyrex. A photograph of a device which failed following the latter process is shown in figure 13(*b*). In several experiments, we have successfully used the devices around pressures corresponding to 80–90% of the burst pressure for more than 1 h.

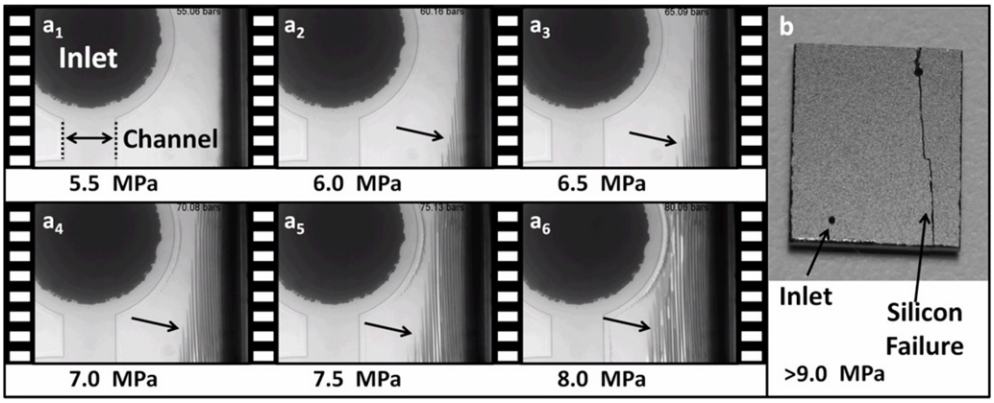

Figure 13. Optical microscope images extracted from a video sequence of a burst pressure failure experiment. (*a*) Snapshots of propagating cracks (indicated by arrows) due to parylene failure around the inlet area for a typical device with a burst pressure of 8 MPa. (*b*) Silicon failure occurs in the case of a high parylene–SiO_2 bonding strength (>9 MPa).

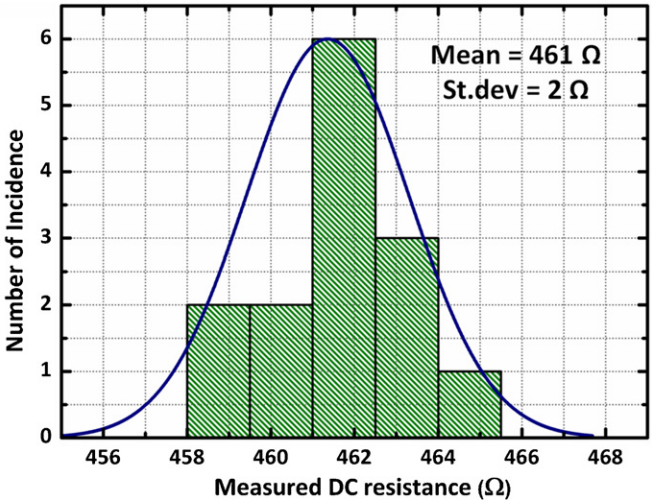

Figure 14. Histogram of measured dc resistance values for multiple pad-to-pad contact test structures after bonding and fit to a Gaussian curve.

4.4. Electrical characterization and measurements

In order to verify that the electrodes and contact structures are fully functional after the bonding process, dc resistance measurements were made using an Agilent 34410A multimeter on a special pad-to-pad electrode test structure, which included some long electrode connections and a number of metal-to-metal contacts. Figure 14 shows the histogram of the measured dc resistances for multiple test structures. It can be seen that the measured resistances are very reproducible with 2 Ω of standard deviation. AC electrochemical impedance spectroscopy (EIS) analysis was also made to confirm that fluidic contacts were properly working when in contact with a phosphate buffered saline (PBS) solution. The analysis was realized using an Agilent 4294A impedance analyser under 5 mV excitation. At first, the 10X concentrated PBS solution (Sigma-Aldrich) was diluted to lower concentrations. After the microchannels were filled with the solution, the impedance and phase data were recorded. Figure 15(*a*) shows the equivalent electrical circuit model for an electrochemical cell. In this model, C_{cell} is the capacitance of the detection cell including the highly polarizable aqueous solution ($\varepsilon_{\mathrm{r}} \approx 80$) and parasitic capacitances in the chip [43]. The interface between the solution and the electrodes is represented by a circuit, where R_{sol} is the solution resistance, C_{dl} is the electrical double layer capacitance, R_{ct} is the charge transfer resistance and W is the Warburg impedance. Figure 15(*b*) shows the Nyquist plots corresponding to impedance measurements of a device for 0.1X concentrated and 0.38X concentrated PBS together with the EIS analysis conducted by fitting curves with the given equivalent electrical circuit model. Using this method, it was possible to estimate the model parameters with a precision of 2%. Figure 15(*c*) shows the plot of the measured solution conductance ($1/R_{\mathrm{sol}}$) versus the used PBS concentration, where a very good linear agreement is observed for concentrations higher than 0.1X. We want to stress that the present electrical characterization was merely to demonstrate the functionality of the microfluidic chip with platinum electrodes, rather than doing a full electrochemical characterization. In the light of this technology-oriented paper, these results indicate that the parylene-C to SiO_2 bonding process is fully compatible with a technological process for realization of this type of microfluidic device.

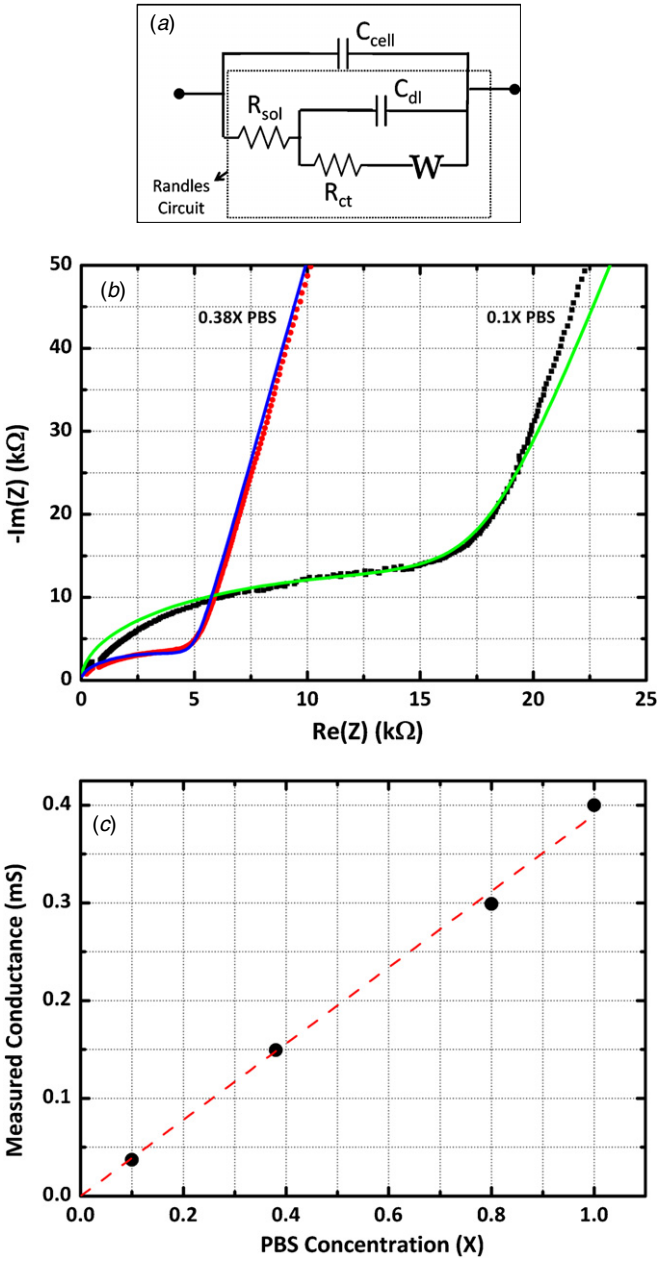

Figure 15. EIS analysis results for different PBS concentrations. (*a*) The equivalent electrical circuit model for an electrochemical cell. In this model, C_{cell} is the capacitance of the detection cell, R_{sol} is the solution resistance, C_{dl} is the electrical double layer capacitance, R_{ct} is the charge transfer resistance and W is the Warburg impedance. (*b*) Nyquist plots of the impedance measurements of a device for 0.1X concentrated and 0.38X concentrated PBS together with the EIS analysis conducted by fitting with the given equivalent electrical circuit model. Full lines indicate the model fits, while the squares and circles represent experimental data for 0.1X and 0.38X PBS, respectively. (*c*) Plot of the measured solution conductance ($1/R_{\mathrm{sol}}$) versus the used PBS concentration. The full line is a linear fit with a slope of 0.39 mS/X.

5. Conclusion

We have demonstrated the feasibility of a polymer glue bonding technology for realization of high-pressure microfluidics (11.1 MPa) using small cross-sectioned microfluidic channels (10 μm × 10 μm) interfaced with multi-layer microelectrodes having small feature size (2 μm). This was achieved by a new low stress parylene-C/SiO_2 bonding process, which is based on bonding an oxygen plasma-activated parylene-C layer that is vapour deposited on a single substrate with a second wafer. Pull tests revealed that the bonding strength was as high as 10 MPa ± 3 MPa with a minimum yield of 90% per wafer after dicing. The burst pressure of the bonding stacks was on average 7.6 MPa with a standard deviation of 1.7 MPa. We have either identified parylene-C crack generation and propagation or silicon failure as the origin of the device failure, rather than bonding interface failure. Moreover, we reported a microfluidic interface and a wire bonding-free integration approach for our devices, by which high-pressure connections can be reliably established in less than 1 min. Consequently, the overall system improves the burst pressure characteristics, while being compatible with dense metallization and preserving fast and plug-and-play-like fluidic and electrical integration. It is anticipated that our approach can significantly enhance the throughput of experimentation in biomedical microsystems, possibly leading to reduced cost-per-throughput, one of the key parameters in microsystems commercialization.

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