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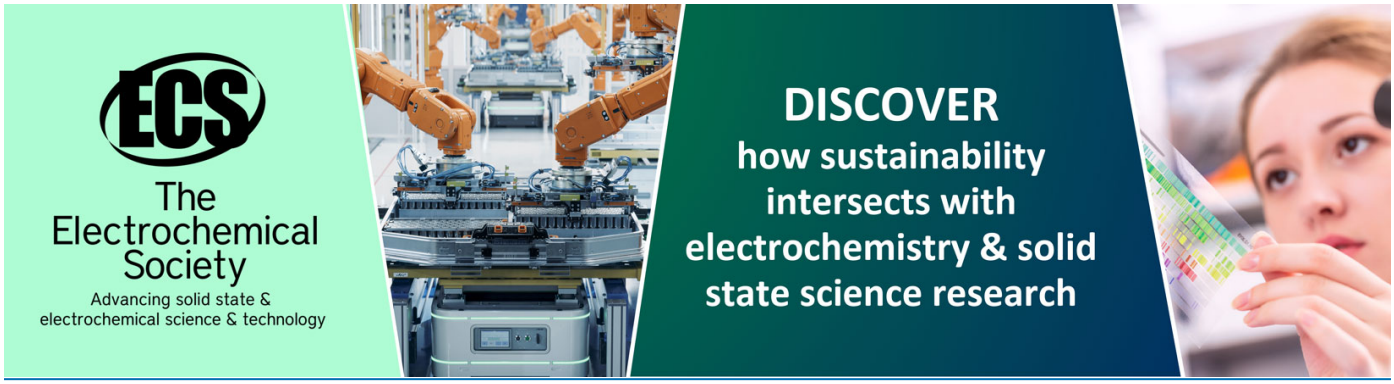

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Electrical properties of GaSb/InAsSb core/shell nanowires

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Abstract

Temperature dependent electronic properties of GaSb/InAsSb core/shell and GaSb nanowires have been studied. Results from two-probe and four-probe measurements are compared to distinguish between extrinsic (contact-related) and intrinsic (nanowire) properties. It is found that a thin (2–3 nm) InAsSb shell allows low barrier charge carrier injection to the GaSb core, and that the presence of the shell also improves intrinsic nanowire mobility and conductance in comparison to bare GaSb nanowires. Maximum intrinsic field effect mobilities of 200 and 42 $cm^2 Vs^{-1}$ were extracted for the GaSb/InAsSb core/shell and bare-GaSb NWs at room temperature, respectively. The temperature-dependence of the mobility suggests that ionized impurity scattering is the dominant scattering mechanism in bare GaSb while phonon scattering dominates in core/shell nanowires. Top-gated field effect transistors were fabricated based on radial GaSb/InAsSb heterostructure nanowires with shell thicknesses in the range 5–7 nm. The fabricated devices exhibited ambipolar conduction, where the output current was studied as a function of AC gate voltage and frequency. Frequency doubling was experimentally demonstrated up to 20 kHz. The maximum operating frequency was limited by parasitic capacitance associated with the measurement chip geometry.

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Keywords: GaSb, InAsSb, heterostructure nanowires, frequency doubler, MOSFET, ambipolar conduction, core/shell nanowire

(Some figures may appear in colour only in the online journal)

1. Introduction

The GaSb/InAs heterostructure has recently been examined intensely in quantum physics studies as well as in device applications [1–5]. The heterostructure alignment is type-II broken gap, where the bottom of the InAs conduction band lies 150 meV below the top of the GaSb valence band [6–8]. The broken band alignment leads to accumulation of intrinsic carriers on either side of the junction [9, 10]. High electron and hole density can thus be achieved without intentional doping, accompanied by high carrier mobility due to the absence of impurity scattering [11]. The unique electronic properties of the GaSb/InAs heterostructure have been used in development of a wide range of novel electronic and photonics devices such as high current density tunnel diodes [8, 12–14], tunnel field effect transistors (FETs) [15], infrared photodetectors [3], lasers [16], complementary metal-oxide –semiconductor FET [5, 17] and frequency multipliers [18].

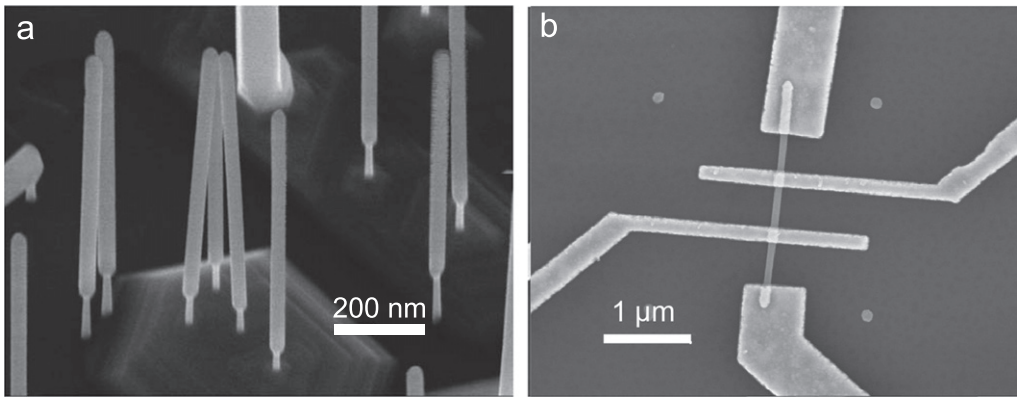

Figure 1. (a) A SEM image of as-grown GaSb/InAs core/shell nanowires. (b) A SEM micrograph of a fabricated four-terminal nanowire device with a source-drain and inner probe separation of 2 μm and 500 nm, respectively.

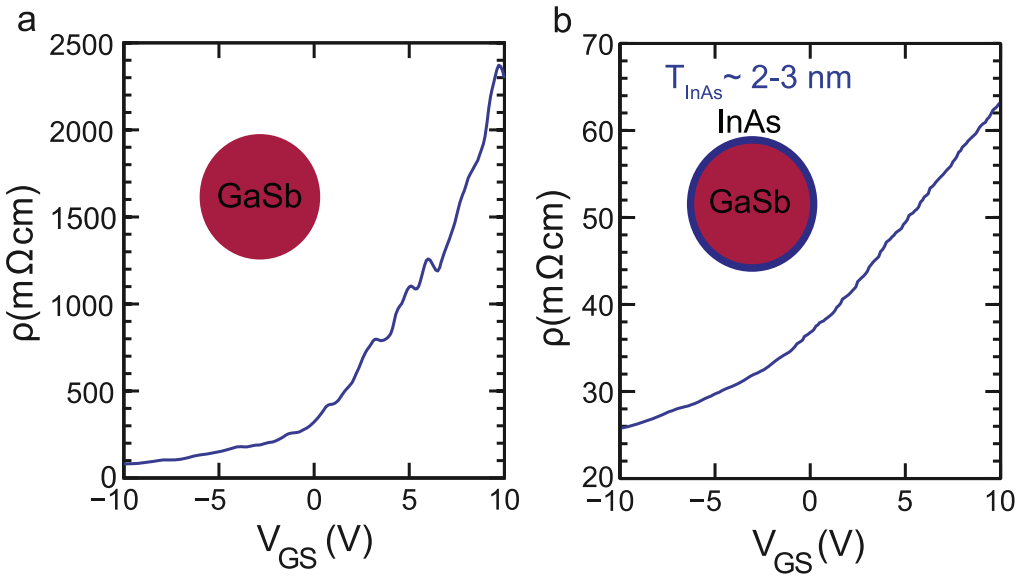

Figure 2. Room temperature intrinsic (four-probe) wire resistivity versus V_{GS} for (a) bare GaSb and (b) GaSb/InAs core/shell with a thin InAs shell.

In a recent study, we reported on the electrical properties of radial GaSb/InAsSb junctions formed in core/shell nanowires (NWs), characterized using a two-probe configuration [10]. It was found that the transport path and charge carrier type of such core–shell nanowires could be tuned by the InAsSb shell thickness and applied gate voltage [10]. It was also found that the presence of a shell significantly reduced the two-probe resistivity and improved the *I–V* characteristics of basic transistor structures. Similar results were also recently reported for thin InGaSb-InAs lamellas [19]. In the present work we have revisited this material system, utilizing primarily a four-probe setup in order to separate between contact-related (extrinsic) and nanowire-related (intrinsic) transport properties, as well as further investigating the ambipolar nature of the structure for the purpose of frequency multiplication. From the four-probe measurements we find that the addition of a shell improves *both* the injection of carriers into the GaSb and the intrinsic hole mobility. In particular, we find that the intrinsic hole mobility of core/shell NWs increases with decreasing temperature, whereas the opposite behavior is observed for bare-GaSb NWs. This suggests a cross-over in the dominant scattering mechanism, from ionized impurity scattering in bare nanowires, likely associated with the GaSb surface, to phonon scattering in the case when the GaSb surface is covered by a thin InAsSb layer.

Table 1. Averaged values for contact resistance and wire resistivity (at zero gate bias) for GaSb and GaSb/InAs core/shell NWs.

T_{InAs}	Wire resistivity (mΩcm)	Contact resistance (kΩ)	Number of devices
0	280 ± 40	70 ± 15	5
2–3 nm	39 ± 5	1.6 ± 0.5	10

In addition to improving the transport properties of the underlying GaSb *p*-channel, the InAsSb shell can at the same time be utilized as an active *n*-channel. Nanowires with an InAsSb shell thickness (T_{InAs}) of 5–7 nm were processed into

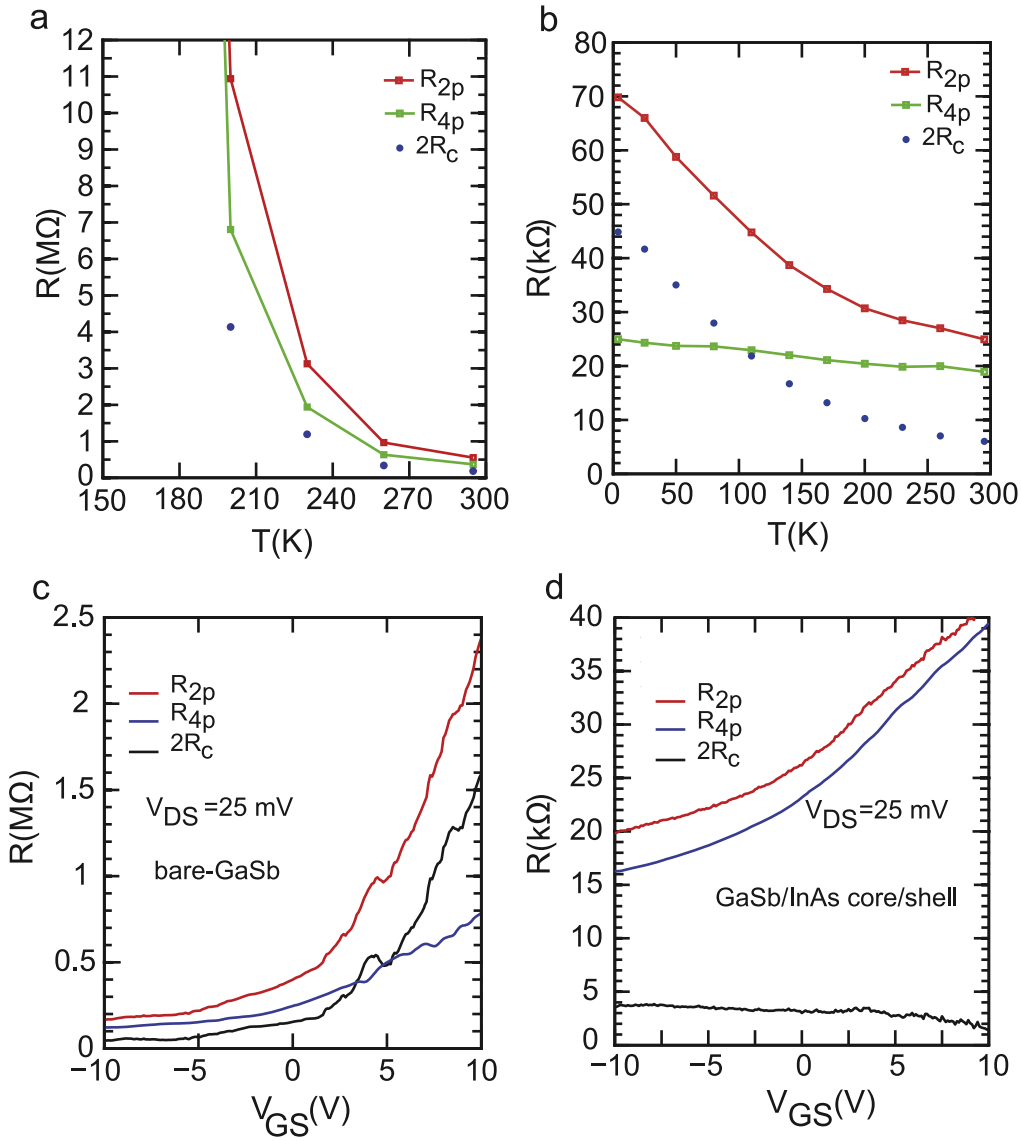

Figure 3. (a) Device (R_{2P}), wire (R_{4P}) and contact ($2R_C$) resistances of a bare GaSb nanowire device for $V_{DS} = 50$ mV versus temperature ranging from $T = 295$ to 200 K. (b) Corresponding device (R_{2P}), wire (R_{4P}) and contact ($2R_C$) resistances of a GaSb/InAs core/shell nanowire device with a thin InAs (2–3 nm) shell for $V_{DS} = 25$ mV and temperature ranging from $T = 295$ to 4.2 K. (c) Device (R_{2P}), wire (R_{4P}) and contact ($2R_C$) resistances of a bare GaSb nanowire device for $V_{DS} = 25$ mV versus gate voltage. (d) Corresponding device (R_{2P}), wire (R_{4P}) and contact ($2R_C$) resistance of a GaSb/InAs core/shell nanowire device with a thin InAs (2–3 nm) shell for $V_{DS} = 25$ mV versus gate voltage.

FETs with top-gate electrodes that covered both source and drain contacts. The transfer characteristics of such nanowire field effect transistors (NW FETs) showed ambipolar behavior [10], where the *n*-type shell contributes to the transport for positive gate voltages. For such core–shell nanowires we demonstrate a new nanowire-based frequency-multiplier device with interesting properties. First, the device is very simple and compact, and second, almost perfectly symmetric ambipolar *I–V* characteristics can be obtained for certain core and shell dimensions.

2. Experiment

GaSb/InAsSb core/shell and bare-GaSb nanowires were grown from Au aerosols on a GaAs substrate by means of metal organic vapor phase epitaxy (MOVPE). First, Au aerosol particles with a nominal diameter of 30 nm were dispersed onto the GaAs substrate. After a short annealing step at 700 °C in the MOVPE reactor, a short GaAs nanowire stem was first grown in order to facilitate the nucleation of the GaSb segment [23]. GaSb was grown at 460 °C using trimethylgallium (TMGa, molar flow of 20.55×10^{-6} Mol min^{-1}) and trimethylantimony (TMSb) as precursors at a V/III ratio of 1.1, and a growth time of 50 min was used to obtain around 2 μm long GaSb segments. Subsequently, for growth of the InAsSb shell, the temperature was reduced to 460 °C and overgrowth of the GaSb core with an InAs shell was initiated by turning on both the trimethylindium (TMIn, molar flow of 2.6×10^{-6} Mol min^{-1}) and arsine (AsH_3) flows with a V/III ratio of 42 simultaneously. The InAsSb shell was grown for

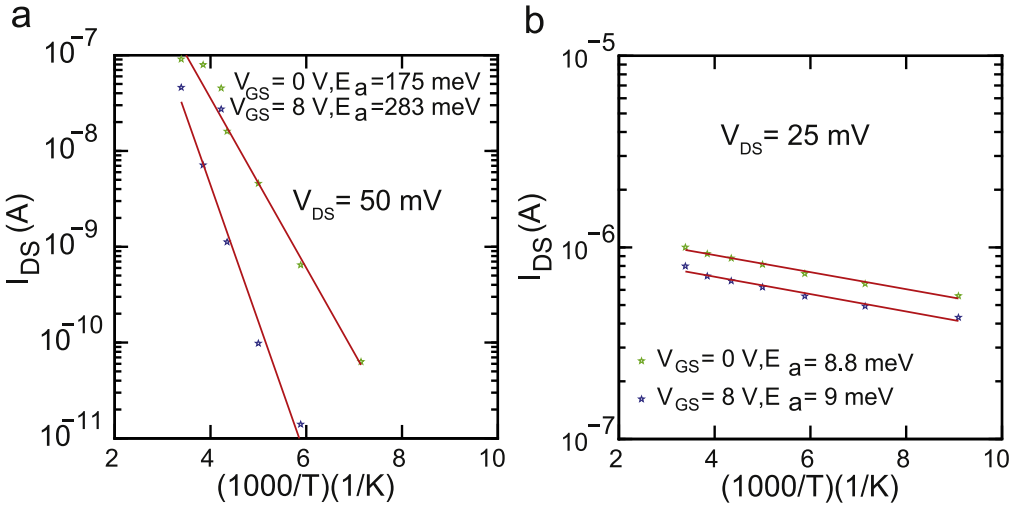

Figure 4. Current at $V_{GS} = 0$ V and 8 V as a function of 1000/T. (a) Activation energies of 175 and 283 meV were extracted for bare-GaSb at $V_{GS} = 0$ and 8 V, respectively. Such values indicate the formation of a significant Schottky barrier at the metal-semiconductor contact. (b) In the case of a core/shell nanowire, a negligible activation energy of ~9 meV is extracted, suggesting that the InAs shell provides an excellent low barrier contact to the GaSb core.

10 min. During growth of the InAs shell, an axial InAsSb segment also formed, for which the properties are reported elsewhere [8, 24]. The nanowires have a defect-free zinc-blende GaSb core with a diameter of 60–70 nm. The shell contains trace amounts of Sb [25], but for simplicity we still refer to this as InAs in the text.

In the device fabrication, micron-size metal pads and markers were first patterned onto a silicon wafer with 100 nm thick SiO_2 layer. NWs were then dry deposited onto the substrates followed by SEM inspection, electron beam lithography and lift-off to electrically connect the nanowires to the predefined micron-size metal pads used for wire bonding. Before contact metallization on the selected NWs, the contact areas were etched to remove native oxides. The etching process and contact metals were different for the core/shell and bare GaSb NWs: the bare GaSb NWs were etched with HCl: H_2O (1:10) solution for 35 s followed by rinse in H_2O prior to 100 nm Pd deposition. The core/shell NWs were etched in buffered HF for 5 s followed by H_2O rinsing, and 20 nm Ni and 80 nm Au metal evaporation. Figure 1(b) shows a SEM image of a fabricated four-terminal device. For some devices the InAs shell was selectively removed after the first round of electrical measurements. In this case a citric acid: hydrogen peroxide (2:1) solution was used for 12 s followed by a rinse in H_2O (SEM images of nanowires with selectively etched InAs shell are shown in supplementary information). Room temperature electrical measurements were performed in vacuum with the heavily doped silicon substrate acting as a back-gate, whereas a He ambient was used for temperature dependence measurements.

3. Result and discussion

To separate between intrinsic properties and contact-related properties, both four-probe and two-probe electrical measurements were carried out. In a two-probe configuration, the measured resistance contains contributions from the contacts in addition to the NW resistance, while in a four-probe configuration the measured resistance ideally represents the intrinsic NW resistance. For this reason, four-probe measurements were carried out over a range of temperature from 300 to 4.2 K to extract the intrinsic temperature behavior of conductance, mobility and carrier concentration.

Figures 2(a)–(b) show intrinsic resistivity ($\rho = \frac{RA}{L}$, where R, A and L are the wire resistance, cross sectional area and length, respectively) at a source-drain bias, $V_{DS} = 25$ mV, versus back-gate voltage, V_{GS}, for a bare GaSb (a) and a core/shell NW (b). The two cases exhibit similar gate dependence, although with very different values for the resistivity. The average intrinsic NW resistivity (at $V_{GS} = 0$) is 280 mΩ cm for the bare-GaSb case, and 39 mΩ cm for the core/shell case. The resistivity is thus reduced an order of magnitude by radial growth of a thin InAs shell, which we primarily attribute to a reduction in trap density at the GaSb surface and surface oxide.

Values for room-temperature contact resistance were extracted for the two cases in figure 2, and listed together with nanowire resistivity in table 1. A similar contact length (200 nm) was used in both cases. The much lower contact resistance in the case of a thin InAs suggests a significant reduction in the barrier for carrier injection into the GaSb. However, it should be pointed out that the contact metals here were different (Pd for GaSb, Ni/Au for GaSb/InAs) as we found that Pd resulted in a better contact to bare GaSb NWs than Ni/Au.

To elucidate how the presence of the InAs shell in the core/shell system affects the electrical properties of the system, the temperature dependence of the four-probe resistance, R_{4p}, and the two-probe resistance, R_{2p} were studied. The results are depicted in figures 3(a) and (b), respectively, obtained at zero gate voltage. R_{4p} is thus the intrinsic NW

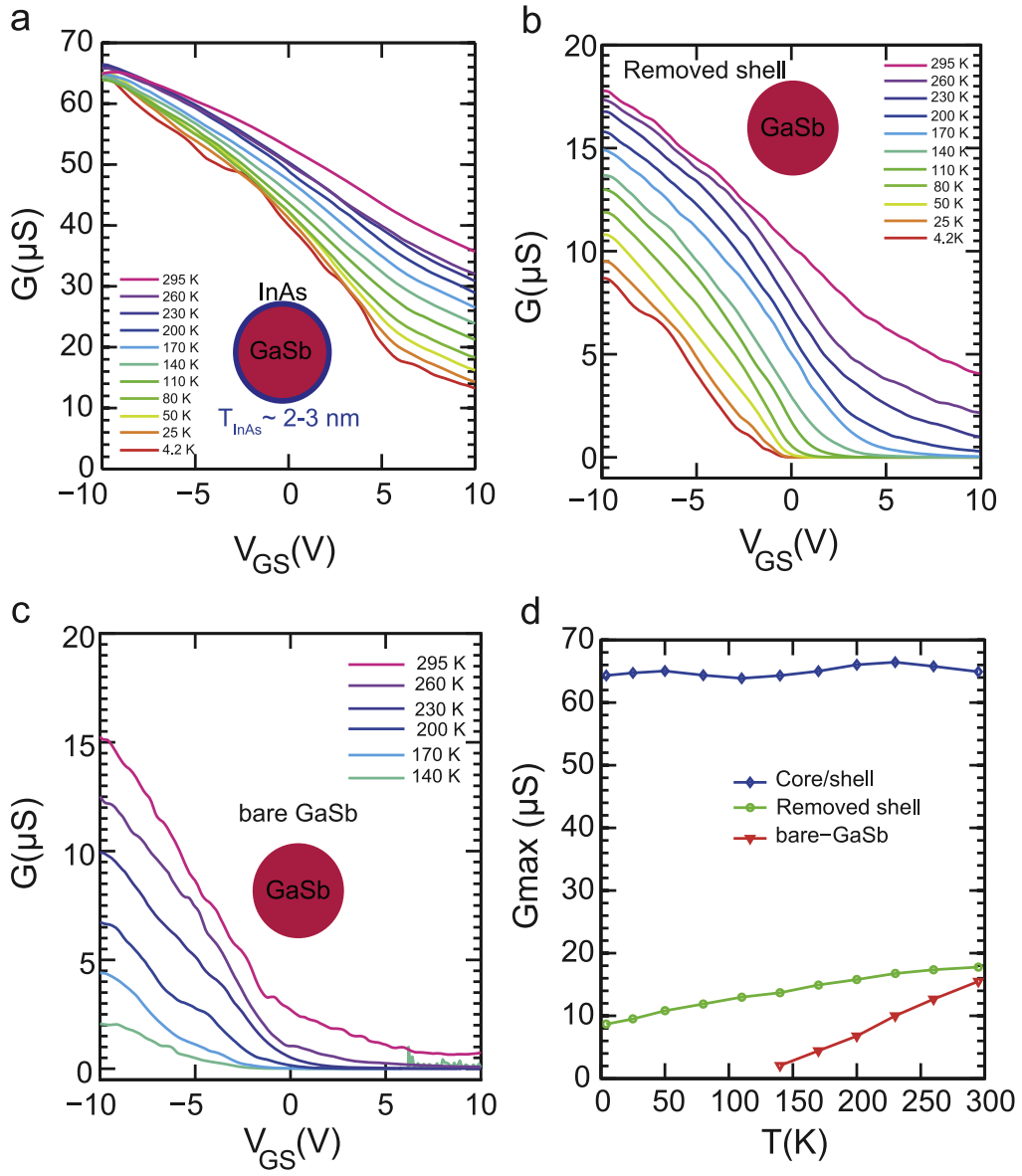

Figure 5. The channel conductance versus V_G at different temperatures for (a) GaSb/InAs core/shell NWs, (b) removed shell NWs and (c) bare-GaSb NWs. (d) The on-state conductance ($V_{GS} = -10$ V) of removed shell and bare-GaSb NWs is a decreasing function of temperature, whereas that of GaSb/InAs core/shell NWs is almost independent of temperature.

resistance. Also shown is the extracted contact resistance, R_C, which is obtained by $R_{2P} = 2R_C + R_{4p}$.

For bare GaSb, both contact and intrinsic wire resistances drastically increase with decreasing temperature, figure 3(a). This indicates a significant barrier at the metal/nanowire interface which blocks carrier injection at low temperature. The higher intrinsic NW resistances at low temperature can be attributed to the depletion of the NWs. For the GaSb/InAs core/shell NWs, figure 3(b), both contact resistance and intrinsic resistance also increase with decreasing temperature, but much more slowly. In particular, the intrinsic resistance shows a very weak temperature dependence. Below 100 K the contact resistance become larger than the intrinsic resistance, and R_{2p} follows the contact resistance trend, which clearly emphasizes the need for four-probe measurements also in this case. Figures 3(c), (d) shows the gate-dependence of R_{2P}, R_C and R_{4p} at room temperature, where it is noted that R_C of the core/shell NWs shows opposite gate dependence compared to that of bare-GaSb NWs.

To better understand transport across the metal/nanowire interface, the current measured from two-probe configuration at different temperatures were studied by Arrhenius plots at $V_{GS} = 0$ and $V_{GS} = 8$ V (OFF-states), shown in figures 4(a) and (b). Activation energies of 175 and 283 meV were extracted for bare-GaSb at $V_{GS} = 0$ and 8 V, respectively. Such large activation energies explain the large contact resistance to the bare GaSb, likely due to formation of a significant Schottky barrier at the metal-semiconductor contact that blocks carrier injection. Correspondingly, an activation energy (E_a) of ~9 meV is extracted for GaSb/InAs for $V_{DS} = 25$ mV at both $V_{GS} = 0$ V and 8 V. The small activation energy can be explained by a much reduced barrier for carrier injection in

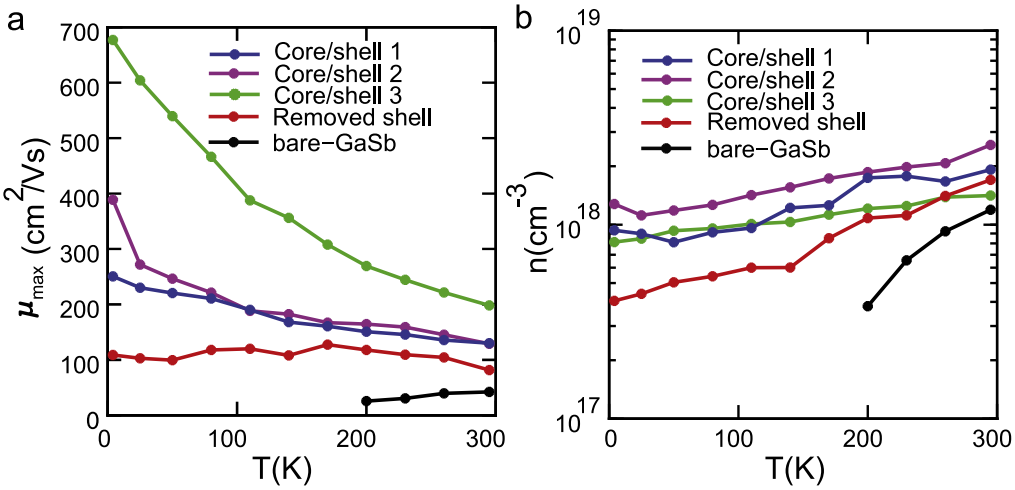

Figure 6. (a) Plot of the maximum mobility versus temperature for GaSb/InAs core/shell NWs with a thin InAs shell, bare GaSb and removed shell GaSb. (b) Temperature dependence of the average carrier concentration (averaged over the entire gate voltage range) for GaSb/InAs core/shell NWs with a thin InAs shell, bare GaSb and removed shell GaSb.

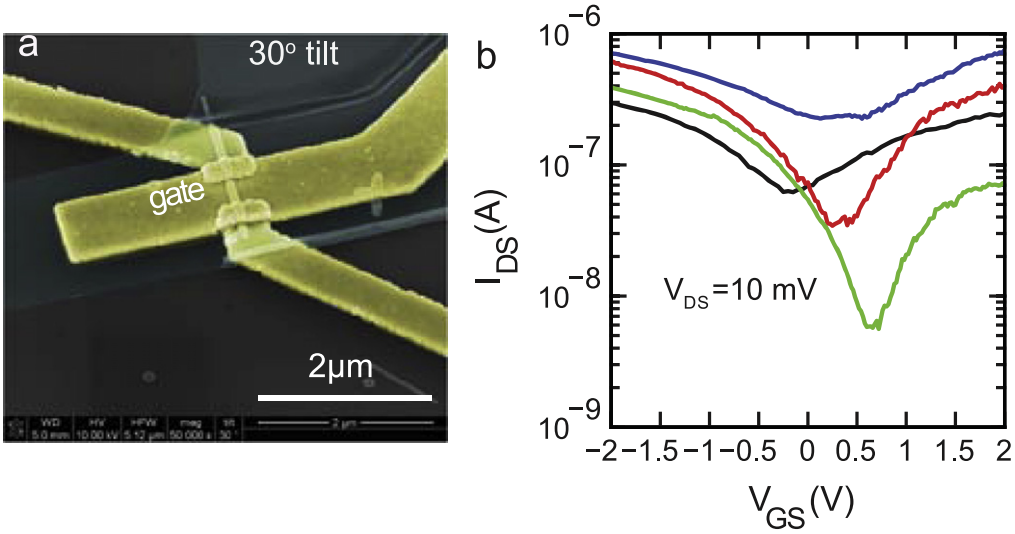

Figure 7. (a) SEM micrograph of a fabricated GaSb/InAs core/shell nanowire field-effect transistor structure. (b) Transfer characteristics of four different GaSb/InAs core/shell nanowire field effect transistors at $V_{DS} = 10$ mV showing almost symmetric ambipolar properties.

the GaSb/InAs core/shell nanowire due to presence of the InAs shell. It should be noted that the extracted activation energies here reflect activation of both contact and carriers in the channel. (See supplementary information for independently extracted contact activation of core/shell nanowires)

Figure 5 presents the intrinsic nanowire conductance, G, versus V_{GS} at different temperatures from 295 to 4.2 K for bare-GaSb, GaSb/InAs core/shell and GaSb NWs from which the InAs shell was selectively removed from the channel after device fabrication. The measured intrinsic conductance is defined as $G = I/(\Delta V)$, where I is the current flowing between two outer contacts (source-drain current) and ΔV the voltage difference between the two inner probes. At room temperature, the on-state conductance (conductance at $V_{GS} = -10$ V) of the core/shell NWs is found to be four times higher than that of the removed shell and bare-GaSb NWs. As the temperature is lowered from room temperature to 4 K, the on-state conductance of the core/shell NW is almost constant while a large drop is observed for the other two cases, especially in figure 5(c).

In the case of the removed-shell NWs, we speculate that InAs here still remains under the contacts leading to improved carrier injection, such that the devices are still conducting at 4.2 K. This is in contrast to the bare-GaSb NWs which showed almost no conduction below 100 K. A thin InAs contact layer thus seems to facilitate probing of electrical properties down to low temperatures for this material system.

Next, the temperature dependence of the average carrier concentration and mobility are investigated. Carrier concentrations for core/shell and bare GaSb nanowires are estimated at different temperatures and averaged over the entire gate voltage range (figure 6(b)). The carrier concentration, n, is obtained from $\sigma = \mu n e$ where σ is the intrinsic NW conductivity, μ field-effect mobility and e is the hole charge. Values for field-effect mobility, μ, at different temperatures were estimated from $\frac{L^2}{C_G}\, dG/dV_G$, where G is the conductance

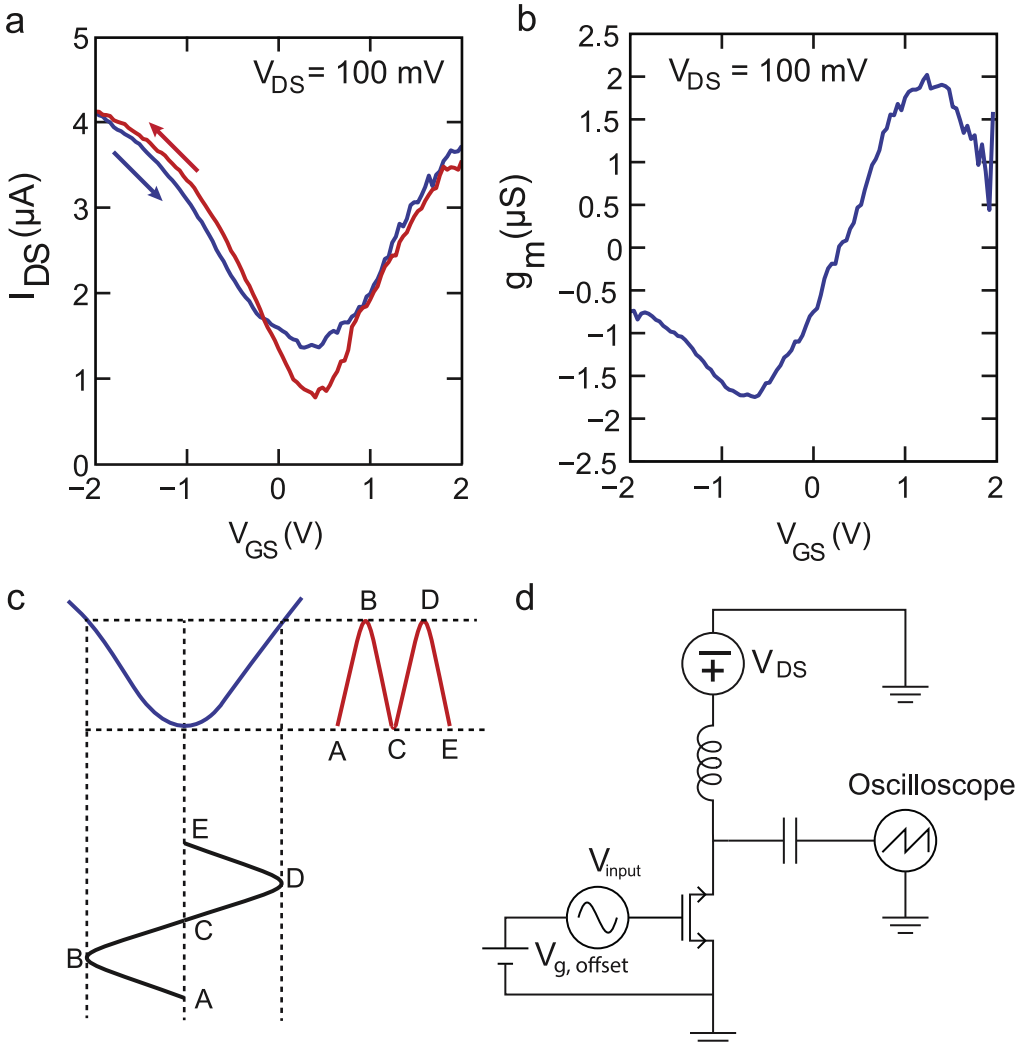

Figure 8. (a) Transfer characteristic of a fabricated GaSb/InAs core/shell nanowire field effect transistor with a channel length of 400 nm for $V_{DS} = 100$ mV. (b) Transconductance, g_m, of the device extracted from the two linear-region slopes of $I_{DS} - V_{GS}$ in *p*- and *n*-branch. (c) and (d) schematic diagrams showing the working principle and measurement setup.

in the linear region, L is the device active length (inner contact separation), and C_G the nanowire to the back-gate capacitance. C_G was obtained by Poisson simulation, and ranged from 5.4×10^{-11} to 6.6×10^{-11} F m^{-1} for the NW diameters in this work [20].

A maximum intrinsic field effect mobility of 200 and 42 cm^2 Vs^{-1} was extracted for the GaSb/InAs core/shell and bare-GaSb NWs at room temperature, respectively. The maximum field effect mobility of the core/shell nanowires is a few times higher than the bare GaSb nanowires reported here as well as other reports on bare-GaSb nanowires [21, 22]. In figure 6, the extracted mobility of the core/shell NWs increases with decreasing temperature, while the mobility of the bare NW decreases from 42 cm^2 Vs^{-1} at room temperature to 25 cm^2 Vs^{-1} at 200 K. The difference in the temperature dependence of the mobility indicates that the presence of a thin InAs shell suppresses the contribution from ionized impurity scattering such that phonon scattering becomes dominant.

In figure 6(b) the temperature dependence of the average carrier concentration is displayed. For GaSb nanowires without an InAs shell the carrier concentration decreases with decreasing temperature by an order of magnitude. The decrease in mobility together with a decrease in the free carrier concentration here seems to explain the diverging intrinsic resistivity of the bare GaSb NWs, which was illustrated in figure 3(a). On the other hand the average carrier concentration in the GaSb nanowires with an InAs shell is only slightly reduced with temperature.

We have now seen that adding a thin InAs shell to the GaSb nanowires improves their *p*-type transport properties. However, if the shell thickness is increased further, the InAs not only acts as a passivating layer, but can also be directly populated with negative charge carriers at sufficiently positive gate voltages. In [10] we found that the crossover from a depleted to populated InAs shell was around 5 nm for $V_{GS} = 0$ V.

To demonstrate how this ambipolar behavior can be utilized in an actual device, top-gates were fabricated onto GaSb/InAs core/shell NWs with shell thickness in the range 5–7 nm (see [10] for further details). A 10 nm layer of HfO_2

was deposited using atomic layer deposition at 100 °C followed by electron beam lithography and Ni/Au metallization for the gate contact. Figure 7(a) shows a SEM micrograph of a fabricated GaSb/InAs core/shell NW FET structure. Electrical measurements were carried out at room temperature. Drain current versus top-gate voltages of four different devices are illustrated in figure 7(b). The contacted NWs show nearly symmetric ambipolar $I_{DS} - V_{GS}$ characteristics. However, the details in the charge transport here strongly depend on relative thickness of the shell and core, which varies from nanowire to nanowire, primarily due to the random nanowire-nanowire separation during epitaxial growth under the conditions used here.

The device characteristics in figure 7(b) are attractive for gate-modulated frequency multipliers, where an oscillating potential on the gate, from positive to negative, leads to oscillations in the output current with twice the frequency. Here, the almost symmetric ambipolarity, with a *p*–*n* transition close to $V_{GS} = 0$ V, is particularly attractive in the device operation. Compared to other nanoscale materials for which frequency multipliers have been demonstrated, such as graphene and nanotubes, the minimum conduction point here can be tuned, in this case by changing the InAs shell thickness.

Figure 8(a) shows the transfer characteristics of another core–shell device, operated at $V_{DS} = 100$ mV. A maximum transconductance of $g_m = 33\ \mu S\ \mu m^{-1}$, normalized to the nanowire diameter and extracted from the linear region of the transfer characteristics, is obtained for both the *p* and *n*-branch (figure 8(b)). This device was used to implement frequency multiplication discussed below.

The basic operation of the NW frequency multiplier is as follows (figure 8(c)): at point A of the input signal, the current in the NW FET is at its lowest value, resulting in minimum current in the output which can be related to its output voltage. The input signal is then driven to point B, corresponding to its *p*-region, and reaches its maximum hole current value in the $I_{DS} - V_{GS}$ curve and hence the maximum point B in output signal. After B, the input signal again moves to its minimum point, and the output current decreases to its lowest value at point C. Beyond point C, the NW FET operates in its *n*-region and the output signal reaches its maximum point C. Finally, the input signal goes back to its minimum value at point E, and the output signal decreases back to its minimum value. In essence, there are two output signal periods for every single period of AC input signal, and thus frequency multiplication is realized as a result of the ambipolar-transport properties of the NW FET. Figure 8(d) shows a schematic of the measurement setup used in these measurements.

The AC characteristics of the NW FET were measured and depicted in figure 9(a). A DC gate voltage $V_{g,offset} = 0.7$ V and source-drain voltage $V_{DS} = 200$ mV were applied to gate and drain electrodes, respectively. Here, the comparatively small $V_{g,offset} = 0.7$ V was applied to shift the bias operating point of the NW FET to the minimum conduction point. For a 5 kHz input waveform signal (superimposed on $V_{g,offset}$) with a peak-to-peak value $V_{PP} = 2.1$ V, a sinusoidal output signal of $V_{PP} = 300$ mV with a doubled frequency of 10 kHz and voltage gain of 0.14 was observed.

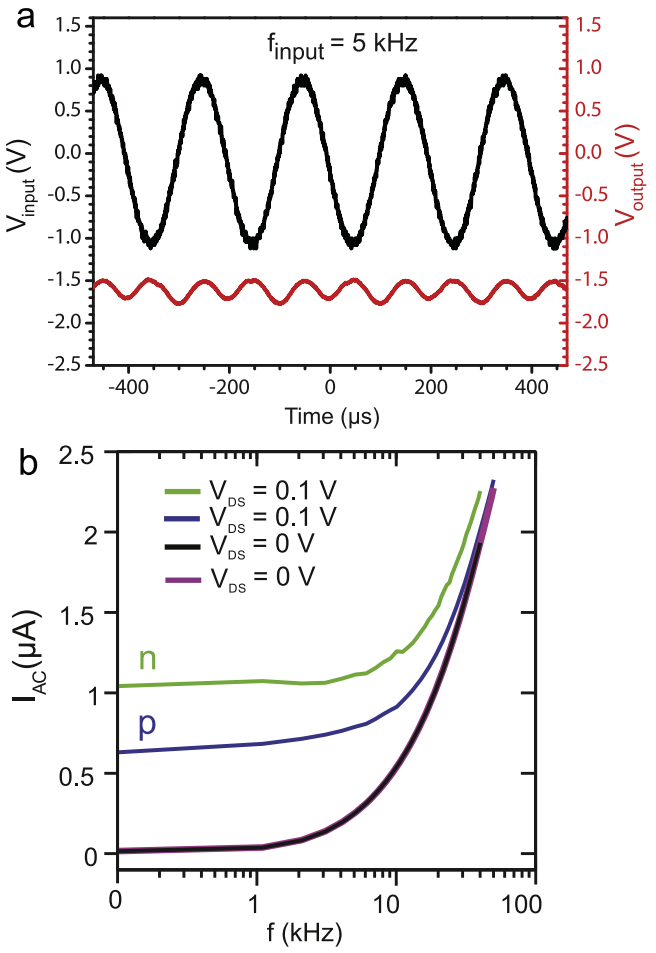

Figure 9. AC characteristics of a GaSb/InAs core/shell nanowire FET-based frequency multiplier. The device is biased at $V_{DS} = 200$ mV and $V_{g,offset} = 0.7$ V was applied at the gate. (a) Input and output sinusoidal waveforms for an input frequency of 5 kHz with input and output peak-to-peak voltages of 2.1 V and 0.3 V, respectively. (b) Frequency dependence transfer characteristics of an ambipolar GaSb/InAs core/shell NW FET at $V_{DS} = 100$ and 0 mV. DC bias values of $V_{g,offset} = +1.3$ V (electrons) and $V_{g,offset} = -1.0$ V (holes) were applied to the gate to shift the operating point into the electron and hole regimes, respectively. An AC voltage of $V_{g,RMS} = 0.75$ V was then applied at the gate and current was measured as a function of frequency.

As the input signal frequency increased beyond 20 kHz the output waveform signal become increasingly distorted (supplementary information), which can be attributed to parasitic capacitance of the large electrode pads on the measurement chips, estimated to 10 pF.

To shed light on the parasitic capacitance, the frequency response of the source-drain current under electron and hole accumulation was studied in separate measurements. Here, the core–shell transistors were operated at $V_{DS} = 0$ and 0.1 V, with a DC gate bias of $V_{g,offset} = -1.0$ V (holes) and $V_{g,offset} = +1.3$ V (electrons) respectively. An AC voltage of $V_{g,RMS} = 0.75$ V was then applied at the gate, and current was measured (lock-in) as a function of frequency (figure 9(b)). Both *p*- and *n*-branch source-drain current significantly increase with increasing frequency for both V_{DS} of 0 and 0.1 V. The frequency dependence of the current at $V_{DS} = 0$ V

is a measure of the RC-time constant for the charging of the parasitic capacitors towards the source and drain. The data show that the circuit is influenced of the parasitics above 1 kHz in its present implementation. Improved performance is expected by using RF-compatible electrodes and chip design, and by placing several nanowire channels in parallel.

4. Conclusion

Based on temperature-dependent four-probe measurements we found that the presence of a thin InAs shell improved the transport properties of GaSb/InAs core/shell NWs compared to bare-GaSb NWs. As the temperature was progressively reduced from 295 to 4.2 K, the extracted mobility of the GaSb/InAs core/shell NWs increased, while that of bare-GaSb NWs decreased. The results suggest a change in the dominant scattering mechanism from that of ionized impurity scattering to phonon scattering when a thin InAs shell is epitaxially grown around a GaSb nanowire core. Finally, GaSb/InAs frequency multipliers based on core–shell nanowires with a 5–7 nm InAs shell thickness were fabricated and characterized. The specific core–shell dimensions here resulted in almost symmetric ambipolar *I–V* characteristics, ideal for demonstrating the basic functionality of frequency doubling. The nonlinear characteristics and potential for high *p*- and *n*- carrier mobility make this heterostructure an excellent candidate for high frequency electronic applications.

Acknowledgments

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