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Supercond. Sci. Technol. **24** (2011) 095010 (6pp) doi:10.1088/0953-2048/24/9/095010

Investigation of the relationship between the gray zone and the clock frequency of a Josephson comparator

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Received 8 April 2011, in final form 22 June 2011
Published 5 August 2011
Online at stacks.iop.org/SUST/24/095010

Abstract
The Josephson comparator is one of the fundamental building blocks of rapid single flux quantum (RSFQ) electronics. Within this circuit family it is the exclusive device which provides logical data processing. The Josephson comparator is also the basic decision element for very fast analog-to-digital converters and sampler circuits for low input power and high-bandwidth signals based on the RSFQ technique. The performance of those devices is fundamentally determined by the characteristics of the Josephson comparator. In this study the gray zone dependency on the clock frequency of a Josephson comparator is investigated by simulations concerning the influence of thermal noise. This investigation is performed for a series of operating points defined by the bias current and different noise levels defined by the operating temperature. In contrast to former investigations, we analyzed the comparator embedded in a realistic environment for output data processing. We identified a characteristic clock frequency f_c for a comparator topology designed for a 1 kA cm^{-2} niobium fabrication technology. The gray zone of 8 μA remains constant for clock frequencies below $f_c = 15$ GHz and starts to increase for larger frequencies. We also found out that this characteristic frequency is independent of the intensity of thermal noise and therefore independent of temperature.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Today, rapid single flux quantum (RSFQ) electronics is the most promising quantum-based microelectronics [1]. It provides an intrinsic digital coding which represents information by the presence or absence of a magnetic flux quantum $\Phi_0 = \frac{h}{2e}$ (Planck constant h and elementary charge e) in a superconducting loop [2]. The exchange of flux quanta between superconducting loops is performed by switching events of Josephson junctions. By Faraday's law each switching leads to a single flux quantum (SFQ) pulse. RSFQ electronics provides very high switching speed in combination with very low power consumption. Natural quantization of magnetic flux, quantum accuracy and low noise of superconducting circuits enables fast and accurate data conversion between the analog and digital domains too [3, 4]. The logical data processing in RSFQ circuits is performed by the Josephson comparator. This structure consists of two Josephson junctions represented by J_2, J_3 in figure 1. Bias current sources in RSFQ electronics are realized by voltage sources in series with on-chip resistors as assumed for the simulations. The comparator circuit is driven by a clock pulse which is transmitted to the comparator by switching of J_1. Only one of the two junctions (J_2 or J_3) is able to switch when a clock pulse triggers the comparator. The signal current I_{in} determines which one will switch. Ideally, if $I_{in} > I_{th}$, J_3

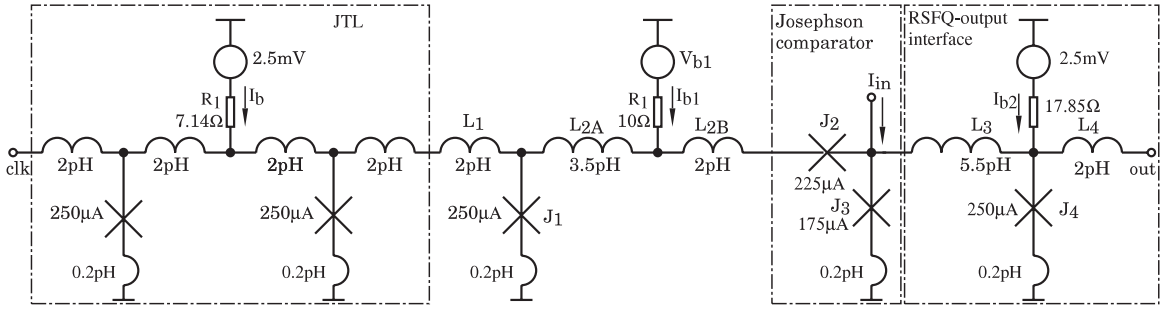

Figure 1. The equivalent circuit of the investigated Josephson comparator. Crosses denote resistively shunted Josephson junctions. V_{b1} is chosen to control I_{b1}.

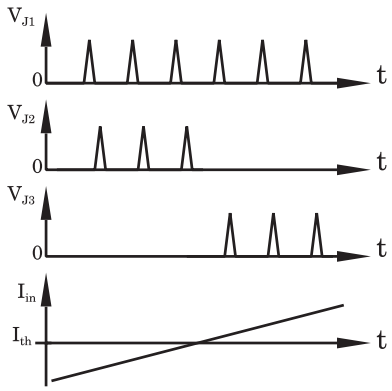

Figure 2. Transient response of the comparator for an increasing input current.

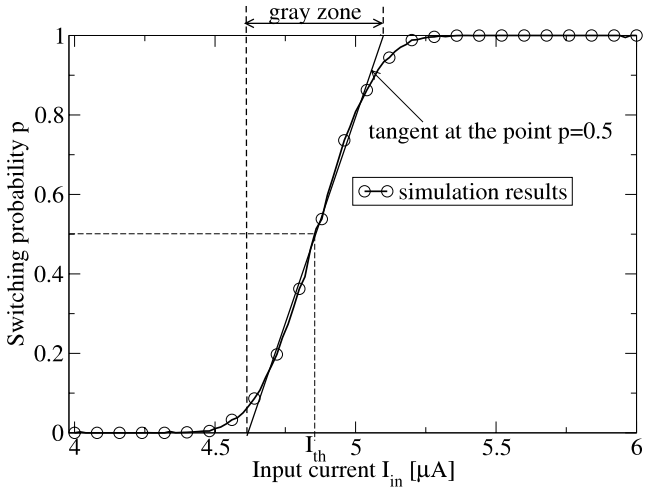

Figure 3. Switching probability p of J_3 versus the signal input current I_{in}.

switches otherwise J_2 switches, where the parameter I_{th} is the threshold current of the comparator.

Figure 2 illustrates the functionality of the Josephson comparator and shows schematically the SFQ pulses, which are produced by the switching of J_1, J_2, J_3 depending on the input signal current I_{in}.

Superconductive analog-to-digital converters [3, 4] and Josephson sampler circuits [5] for low input power and high-bandwidth signals based on the RSFQ technique are the most important applications of the Josephson comparator as a basic decision element [6]. The performance in these applications is often restricted by the decision behavior of the Josephson comparator. The limiting parameter, which is investigated in this paper, is the gray zone (GZ), which describes the decision uncertainty of the comparator. The decision of the comparator is affected by thermal noise, which causes the gray zone [7], i.e. a finite transition width between logical '0' and '1' with respect to the input signal. A typical curve progression of the switching probability p of the comparator junction J_3 versus the input current is illustrated in figure 3. The gray zone is defined as GZ $= 1/m$ where m is the slope of the tangent at $p = 0.5$ of the curve. The thermal noise is caused by shunt resistors of Josephson junctions as well as by resistors of the bias network. In previous investigations the influence of the design parameters (inductances, critical current of Josephson junction and bias current) on the GZ was investigated. Finally, experimentally verified design guidelines to minimize the GZ were derived [8, 9]. In this paper the influence of the clock frequency on the GZ is analyzed. The GZ is used as the performance benchmark in terms of sensitivity with respect to the input signal. The investigations are done by means of JSIM_n, which is a circuit simulator with the ability to simulate thermal noise in the time domain [10]. The device under test is a Josephson comparator which is in accordance with the mentioned design guidelines. The design parameters are appropriate to the 1 kA cm^{-2} fabrication process of FLUXONICS Foundry [11], which corresponds to a characteristic voltage of $I_c R_n = 256\ \mu$V. Typical parasitic elements resulting from the fabrication process are shown in figure 1 and are considered in the simulation. All used junctions in the circuit are designed with a value of McCumber parameter $\beta_c = 1$. We use a parasitic inductance in series with the shunt resistor, as described in [12]. In section 2 the investigation of the gray zone and its dependence on the clock frequency of the comparator is described and the simulation results are shown. We derive a characteristic clock frequency f_c, which defines a new performance benchmark in terms of speed for a particular comparator. In section 3 the abovementioned investigation is repeated for several temperatures to derive the temperature dependence of the GZ and f_c.

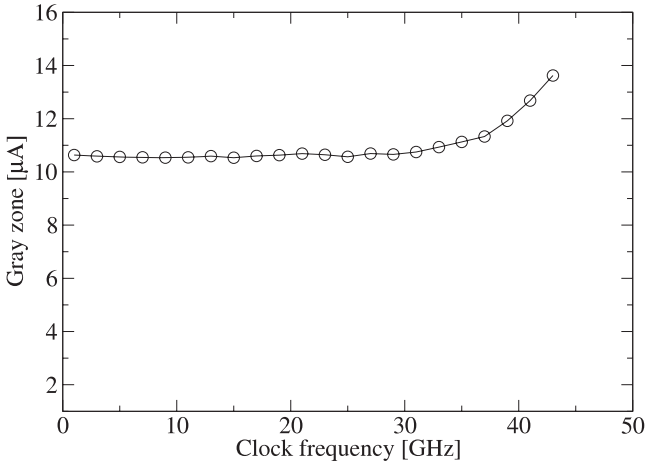

Figure 4. Simulation results of the investigated circuit without RSFQ output interface (see figure 1).

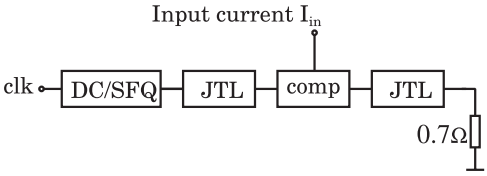

Figure 5. The block diagram of the simulation test bench.

2. Gray zone versus clock frequency of a comparator

In the last few years the Josephson comparator has been the subject of various investigations. A comprehensive experimental analysis was published in [13], which was carried out for a comparator realized in the 1 kA cm^{-2} fabrication process. In this study the Josephson comparator was investigated without an RSFQ output interface (see figure 1). The simulation data of our comparator circuit (figure 1) with $I_{b1} = 170\ \mu$A is in very good agreement with the experimental data in [13], if the output interface is not considered. Figure 4 shows the corresponding simulation result. The gray zone remains constant till a frequency of 35 GHz and for higher frequencies the gray zone increases. Consequently, the Josephson comparator as unloaded circuit element is hardly restricting the maximum frequency of an RSFQ circuit of $f_{max} = I_c R_n / 3\Phi_0$ ($f_{max} = 41$ GHz [14]).

For practical applications of comparators, for example in analog-to-digital (AD) converters or RSFQ electronics, the SFQ output signal has to be recorded and processed. Therefore an RSFQ output interface, which is an adapted Josephson transmission line (JTL), will be connected to the comparator. So, in real applications the comparator output has to handle a low-impedance load.

The gain of our investigation is that we analyzed the performance of the comparator together with peripheral devices necessary to read out the information from the comparator. We studied the gray zone dependence on the clock frequency and one particular bias current $I_{b1} = V_{b1}/R_1$. Our previous analysis of different Josephson comparators [9]

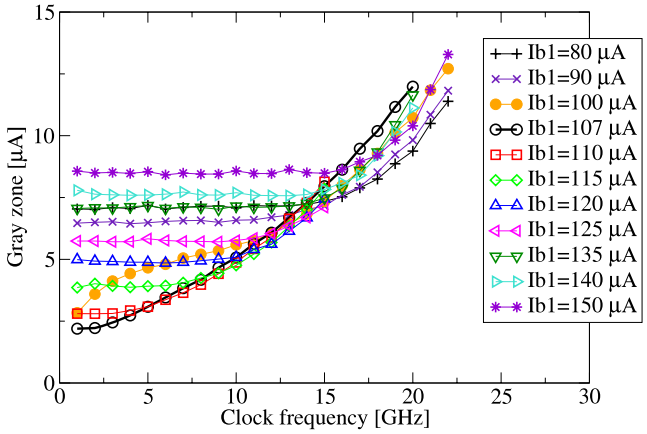

Figure 6. The gray zone versus the clock frequency for several bias currents.

has shown that for fixed critical currents of the Josephson junctions, the gray zone is most sensitive to I_{b1}. The second bias current I_{b2} affects only the threshold current I_{th}. In figure 5 the test bench that we used for the simulations is shown. It contains the comparator (comp), a DC/SFQ converter, which generates the clock pulses and the JTL, which transmits the clock signal. The JTLs are utilized to avoid interactions between the comparator and the DC/SFQ converter. To create a reflection-free termination of the output a 0.7 Ω resistor is used. For the first study a noise temperature of 4.2 K was assumed. The circuit was simulated over 10 000 clock cycles which ensures 10 000 switching events of junction J_1 and the number n_{J3} of switching events of J_3 was counted. The switching probability of J_3 was computed by $p(I_{in}) = \frac{n_{J3}}{10\,000}$. It is well known that this switching probability can be described by [15]:

$$p(I_{in}) = 0.5 + 0.5 \times \mathrm{erf}\left((I_{in} - I_{th})\frac{\sqrt{\pi}}{GZ}\right), \qquad (1)$$

where I_{in} is the input current (see figure 5) and 'erf' is the error function. The simulation was repeated for several bias currents I_{b1} and several clock frequencies. The bias current I_{b1} was varied from 80 to 150 μA. The results showing the influence of the bias current I_{b1} on the gray zone can be recognized in figure 6. Related to the sensitivity there is an optimal I_{b1}, which ensures the smallest gray zone. For this specific topology the optimal bias value is $I_{b1} = 107\ \mu$A providing a gray zone of 2.2 μA and for all other values of I_{b1} the gray zone increases. Above this optimal bias value the reduction of the bias current I_{b1} results in smoother clock pulses [13]. The longer duration of the pulse enables the Josephson comparator to have a longer decision time. This reduces the maximum speed, but also improves the sensitivity, because the longer time allows us to average out high frequency noise and reduces thereby the effective bandwidth in equation (3). For the bias current values below 107 μA this effect is no longer dominant and the gray zone increases with decreasing current values. However, the investigations show also that the gray zone is only constant up to a certain clock frequency, which we call f_c. In contrast to the results of the comparator without RSFQ output (figure 4) this characteristic frequency f_c is reduced from 35 to 18 GHz.

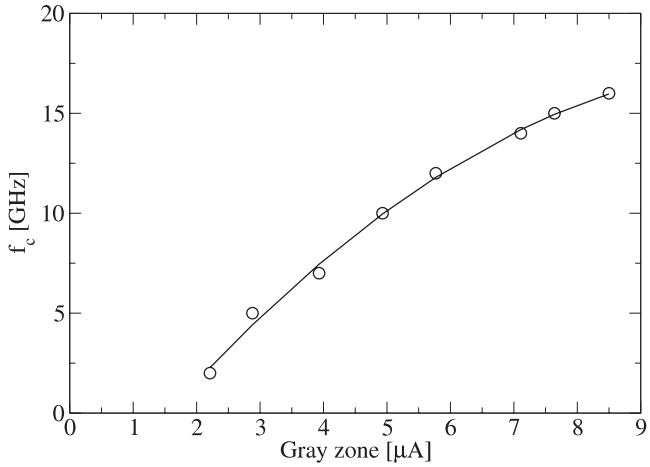

Figure 7. The characteristic clock frequency f_c versus the gray zone.

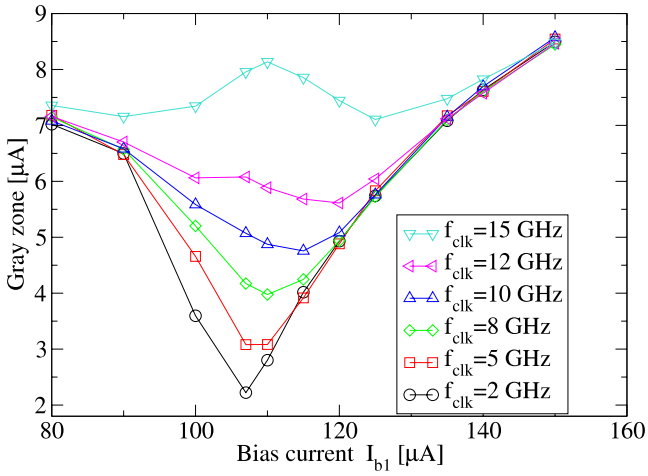

Figure 8. The gray zone versus the bias current.

Table 1. The results of the simulation (f_c, GZ) for several bias currents.

I_{b1} (μA)	GZ (μA)	f_c (GHz)
80	7.15	16
90	6.55	13
100	Not defined	Not defined
107	2.21	2
110	2.88	5
115	3.93	7
120	4.93	10
125	5.77	12
135	7.11	14
140	7.64	15
150	8.5	16

From the curves in figure 6 the value of f_c was determined for every value of bias current in such a way that the difference of the gray zone values between two neighboring points is not larger than 0.2 μA. The criteria of 0.2 μA was chosen in order to neglect the small random variations of gray zone, which appear in simulations. At $I_{b1} = 100$ μA no plateau appears in the gray zone versus clock frequency function. Consequently no f_c value could be defined. The following table 1 and figure 7 illustrate the extracted values of f_c and gray zone. Within the region where the gray zone is constant versus the frequency the average of all values of the gray zone was calculated and is listed in table 1. By a nonlinear curve fitting the relation between f_c and the gray zone is fitted with a quadratic function, as illustrated in figure 7. As a result, this relation is well described by

$$f_c\,(\mathrm{GHz}) = -5.9622 + 4.1279\mathrm{GZ}\,(\mu\mathrm{A}) - 0.18\,205\mathrm{GZ}^2\,(\mu\mathrm{A})^2. \quad (2)$$

Above this characteristic clock frequency the gray zone starts to rise. This effect cannot be explained by the influence of thermal noise. In our opinion it results from the correlation of consecutive flux quanta. Consequently, there is always a compromise between speed and sensitivity. So, the design is an optimization process between the clock frequency and the gray zone. The highest sensitivity can only be ensured for relative low frequencies (<2 GHz). A high clock frequency leads inevitably to increased values of the gray zone and thereby to a reduced sensitivity. In figure 8 the relationship between the gray zone and the bias current I_{b1} is displayed for various frequencies. This illustration is especially helpful to design the comparator for an application with a well defined clock frequency, for example in AD converter applications. For a given clock frequency the operating point with the lowest possible gray zone can be chosen. The main result of this section is: the analyzed comparator provides a small gray zone GZ = 2.2 μA only for a singular operating point and for low frequencies. Because of the parameter spread caused by the fabrication process it is improbable to hit this operation point. For AD converters with a small number of quantizers it is practicable to utilize separate tuning currents to adjust the operation point individually. Consequently GZ = 2.2 μA is a realistic lower bound for the sensitivity of a quantizer in the analyzed topology and technology. In RSFQ circuits a certain margin for all parameters is required to ensure a stable operation of the fabricated circuit and the designed circuit should work with the same characteristics for various frequencies. In this case it is wise to accept the higher gray zone and to use a higher bias current. We suggest I_{b1} = 140 μA which has a moderate gray zone (GZ = 7.6 μA) up to a clock frequency of 15 GHz.

3. Characteristic clock frequency versus operating temperature

Generally the gray zone increases with rising temperature because of the relation between temperature and thermal noise [15, 16]. In previous sections the simulations were done for the temperature 4.2 K and were in this section repeated for different temperatures (2 and 8 K) in order to obtain the abovementioned characteristic clock frequency f_c. Figure 9 shows the dependence of the characteristic clock frequency on the gray zone for several temperatures. This confirms the well known fact that the gray zone can be reduced by reducing the temperature. The thermal noise was taken into account by the

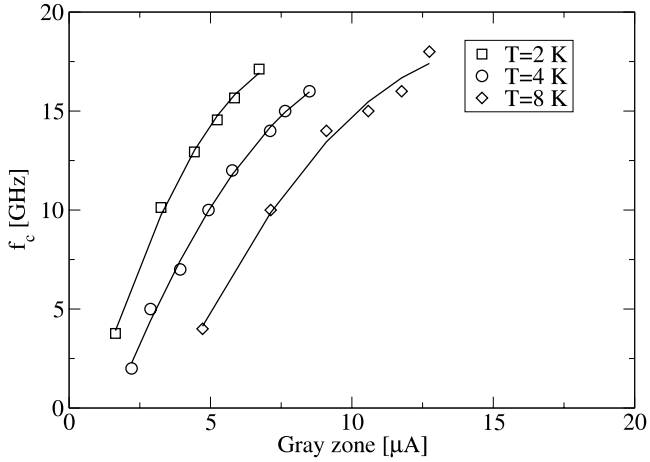

Figure 9. The characteristic clock frequency f_c versus the gray zone for several temperatures.

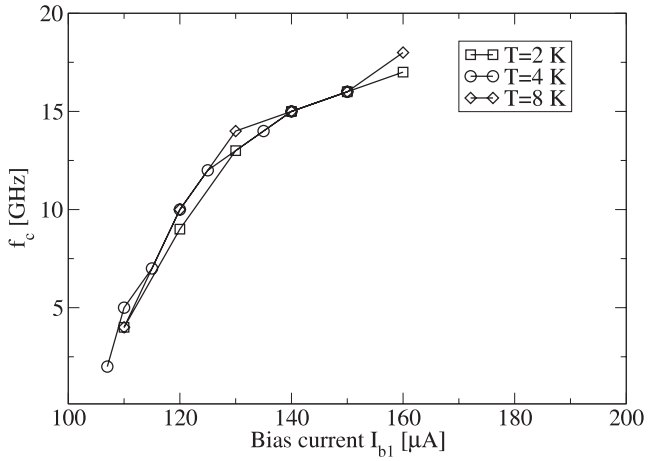

Figure 10. The characteristic clock frequency f_c versus bias current I_{b1} for several temperatures.

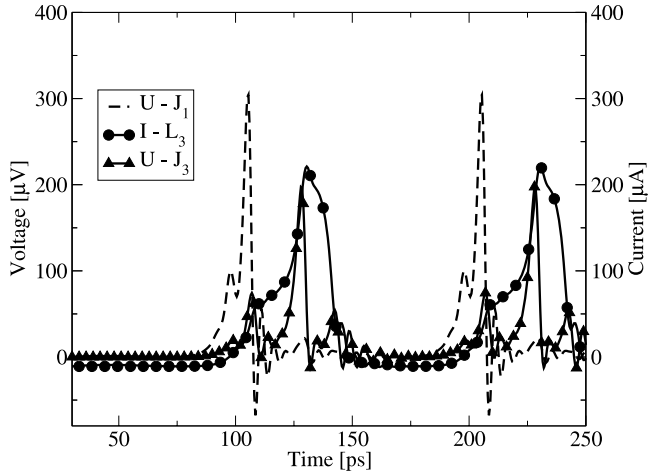

Figure 11. The results of the time domain simulation of the comparator for $f = 10$ GHz.

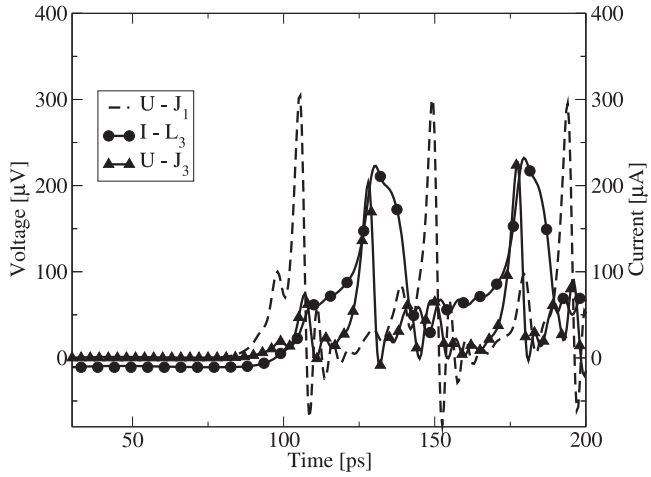

Figure 12. The results of the time domain simulation of the comparator for $f = 25$ GHz.

simulator as a noise current according to the equation [17]:

$$i_n = \sqrt{\frac{4k_B T B}{R}}, \tag{3}$$

where k_B is the Boltzmann constant, T is the temperature and B is the bandwidth.

Consequently, the sensitivity of an AD converter could be enhanced by reducing the temperature. In figure 9 the relation between the characteristic clock frequency and the gray zone is illustrated for various temperatures. Another result of this work is the simulated relation between the bias current I_{b1} and the characteristic clock frequency f_c for several temperatures displayed in figure 10. It becomes obvious that f_c is independent of the temperature and thereby it is independent of the thermal noise too. This result confirms that f_c is not determined by the thermal noise, but rather by the dynamic properties of the comparator. To understand the internal mechanism leading to the increase of the gray zone and to demonstrate the influence of the RSFQ output interface on the Josephson comparator the results of the time domain simulation for $f = 10$ GHz (figure 11) and $f = 25$ GHz (figure 12) with $I_{b1} = 120$ μA are illustrated. To achieve a plain illustration the thermal noise was not considered in this simulation. The figures 11 and 12 show the voltage across the junctions J1 and J3 of the comparator and the current flowing in the inductance L3 (see figure 1). For low frequencies, such as for example $f = 10$ GHz at $I_{b1} = 120$ μA , the comparator has enough time to return to a stable initial state and to dissipate the current flowing in L3. This does not happen for higher frequencies. According to figure 12 there is still a higher current flowing in L3 than in the initial state while the next input pulse triggers the comparator. The current flowing in L3 is relieving junction J3, thus for the next decision process junction J2 is at an advantage. This effect results in an anti-correlation for high frequencies. That means the chance of a switching of J2 becomes higher if J3 switches in the trigger event before. Consequently, the decision of the comparator is not balanced for higher frequencies. It is triggered before the comparator is returned to the initial state. This results in a distorted transition curve. The effect can only be avoided

by increasing the switching speed of the comparator and the RSFQ output interface.

4. Conclusion

In this work a specific topology of a Josephson comparator was simulated and the relationships between gray zone, clock frequency, bias current and temperature were investigated. We utilized the gray zone as the first benchmark for Josephson comparators representing its sensitivity to detect weak input signals. We found, related to our investigated circuit, that the lowest gray zone was achieved for a low bias current ($I_{b1} = 107\ \mu A$). Any different value of this bias current results in a larger gray zone. This is in agreement with the suggestion of soft clock pulses [13, 18]. But in our results there was no local maximum, as reported in [13]. We defined a new characteristic clock frequency f_c for Josephson comparators, functioning as a second benchmark in terms of speed. Our simulations identified a clear relation between clock speed and gray zone. The gray zone remains constant for all clock frequencies below the characteristic clock frequency f_c. Above this frequency an increase of the gray zone can be recognized which is temperature independent. To hit the lowest possible gray zone in circuit design will require a careful adjustment of the bias current. This is only suitable for one or a very few comparators, as used in AD converters or sensor systems. This is different in the case of higher frequencies. For a clock frequency of 15 GHz, the gray zone is almost constant between 80 and 140 μA. This fact is very important for the design of comparators in digital circuits, because the bias current requires some margin to allow complex circuits to work in the presence of process variability.

Acknowledgment

The authors thank Tishreen University in Syria for financial support.

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