Low-jitter on-chip clock for RSFQ circuit applications

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Low-jitter on-chip clock for RSFQ circuit applications

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Abstract. The ultra-narrow linewidth of a long Josephson junction (LJJ) oscillator offers low timing jitter as a clock source. In this paper, we will discuss the improvement of an LJJ clock by using an annular geometry. We demonstrate the integration of an annular LJJ with a clock decimator which consists of a serial chain of toggle–flip–flops (TFFs). Each TFF divides its input frequency by a factor of 2. We have also developed a clock frequency selector. The clock selector circuit can choose either the master clock f_m or one of its sub-harmonics ($f_m/2^m$, $m = 1$ to n), based on the select inputs. The generation of a set of clocks will enable us to integrate the on-chip LJJ clock with a flash analogue-to-digital converter.

1. Introduction

The need for generation and distribution of a stable, low-jitter, on-chip, clock is well known in the superconducting electronics community. The RSFQ technology is based on the presence or absence of a *fluxon* (a quantum of magnetic flux, $\Phi_0 = h/2e = 2.07$ mV ps) in a circuit with respect to a clock. Almost all RSFQ circuits are clocked. The timing of the clock pulse, also in the form of a fluxon, is very important. Currently, high-performance RSFQ circuits, such as a digitizer employing a wide bandwidth ADC [1, 2], derive the fluxon clock from an external signal generator. There are two problems with this approach: (1) the external clock source is expensive and adds to the system complexity, and (2) at high frequency, external clock jitter affects the circuit performance. The first problem is of immediate concern for commercialization of digitizer instruments with 10–20 GHz bandwidth. The second problem is expected to impede the development of higher performance superconducting technology in the future.

It is well known that a very stable, high-frequency oscillator can be made using the propagation of sine–Gordon solitons in a nonlinear system—the long Josephson junction (LJJ). The long junction has some unique features that are unattainable by overdamped RSFQ circuits, such as a very narrow radiation linewidth. For an LJJ working in the resonant soliton mode, a linewidth less than 40 kHz is obtainable at 12 GHz [3]. Fluxons generated at one junction end can provide very narrow clock pulses for RSFQ circuits. We have demonstrated both experimentally [3] and numerically [4] that the RSFQ pulses generated by an LJJ can be successfully launched into RSFQ circuits. This shows that an LJJ-based soliton oscillator can provide adequate power for clocking SFQ circuits.

Currently, we are developing a low-jitter on-chip clock for ADC circuit applications. A block diagram of the wideband ADC with on-chip clock is shown in figure 1. The LJJ oscillator acts as the master clock source. The clock frequency is decimated using a chain of toggle–flip–flops (TFFs). The clock selector chooses either the master clock (f_m) or one of its sub-harmonics, based on the select inputs, and supplies the stream of SFQ clock pulses to the ADC. In this paper, we demonstrate for the first time the integration of an annular long junction oscillator with SFQ circuits; some unique features by using an annular junction instead of a linear one-dimensional LJJ are discussed. We also show the test results for a clock frequency selector circuit

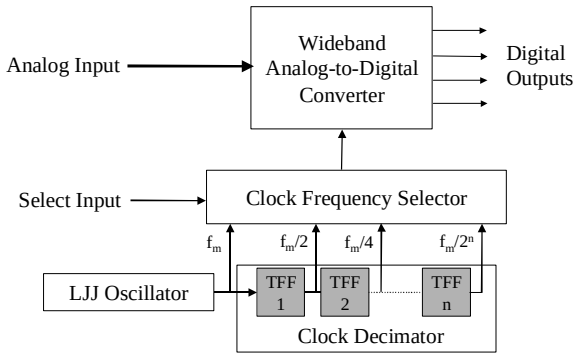

Figure 1. A proposed flash ADC with integrated LJJ clock.

2. Annular long junction coupled to SFQ elements

A long Josephson junction can be formed not only by a linear one-dimensional geometry, but also by an annular or ring-shaped geometry [5, 6]. An annular LJJ not only eliminates boundary effects, but also, due to flux quantization, makes it possible to trap a single soliton. The trapped solitons can

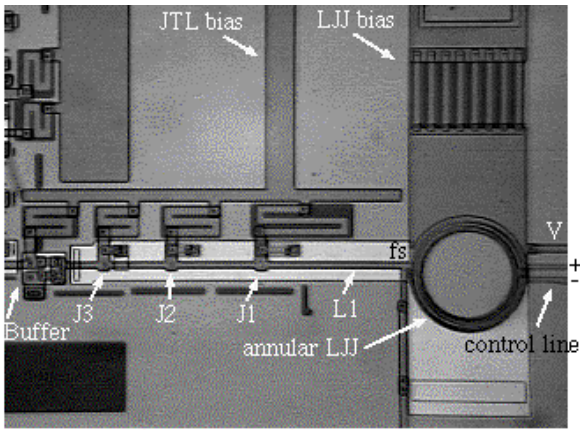

Figure 2. An optical micrograph of a fabricated annular long junction that is coupled to the SFQ circuit. The length of the junction is 230 μm, and the width is 5 μm. The circuit was fabricated using a HYPRES 1 kA cm^{-2} Nb/AlO$_x$/Nb junction fabrication process.

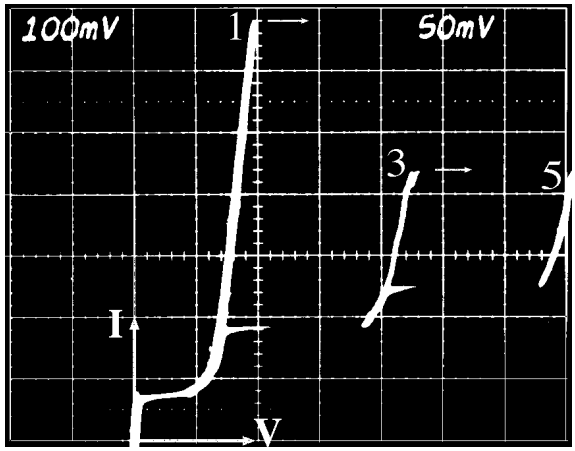

Figure 3. Current against voltage for various numbers of solitons at 4.2 K. There is one trapped soliton. The number next to each curve is the total number of solitons and antisolitons moving to produce that curve.

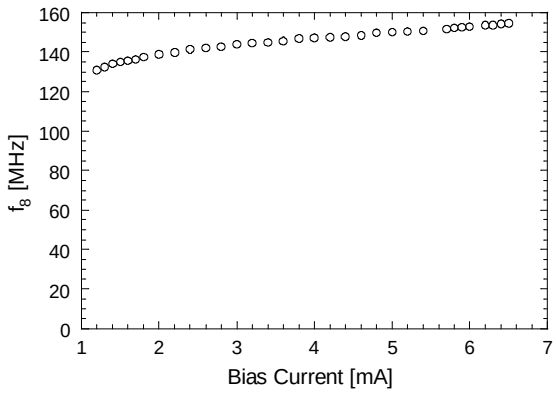

Figure 4. Resonance frequency at the eighth TFF output f_8 against bias current of the annular long junction biased on the $n = 1$ step ($I_{CL} = 9$ mA).

move under an infinitely small bias current, and therefore this eliminates the supercurrent.

Figure 2 shows the circuit that integrates an underdamped annular LJJ with RSFQ circuits. The circuit is very similar to the previous circuit [3] except the long junction is now in an annular geometry. The long junction is terminated with a Josephson transmission line (JTL) at one point. Another end of the JTL is connected to a chain of an eight-stage TFF. All Josephson junctions in the RSFQ cells are resistively shunted. A superconducting control line is designed above the LJJ to apply a dc current I_{CL} in the control-line and create a magnetic field in the long junction.

Dc characterization of this integrated long junction shows similar behaviour to an isolated annular LJJ. It shows a series of evenly spaced voltage steps, each step corresponding to a discrete number of solitons and antisolitons circulating around the junction. These steps correspond to resonant soliton modes. The step voltage is related to the soliton propagation velocity u by [6]

$$V_n = (nu/l)\Phi_0 \qquad (1)$$

where n is the total number of solitons and antisolitons and l is the junction length (circumference) of the junction. For the annular junction, n satisfies the relation $n = n_0 + 2i$, where $i = 0, 1, 2, \ldots$, and n_0 is the number of solitons initially trapped. With no trapped soliton ($n_0 = 0$), an even series of voltage steps is observed and the supercurrent reaches its maximum (7.0 mA) when there is no applied field ($I_{CL} = 0$). With one trapped soliton $n_0 = 1$, however, an odd series of the voltage steps is observed, see figure 3 for step $n = 1, 3, 5$. The odd series is associated with a very small (0.8 mA) supercurrent.

For the application as an on-chip clock, an annular LJJ with one trapped soliton seems the preferred choice. The small supercurrent makes the long junction oscillator much easier to bias. We noticed that the first resonant mode ($n = 1$) in figure 3 has a bias range from 1 to 7 mA while for a linear LJJ the bias range is from 3.5 to 5.5 mA [3]. Also, for a linear LJJ, our measurement shows that it is difficult to (1) bias on the first soliton step due to a large Josephson current, (2) keep the bias on the resonant step for a long time before it switches to the zero-voltage or the normal states. Both problems disappear for the annular LJJ with one trapped soliton.

The even series was obtained by careful cooling through the transition temperature with zero bias current, to ensure that flux was not trapped in the film or the junction. To trap one soliton in the annular junction, two methods have been used in the experiment. In the first method, we leave a suitable bias current present while cooling. Since it is hard to determine the bias current, the process is difficult to control. In the second method, we first cool the circuit to 4.2 K without any bias, producing an even series of soliton modes. We then apply an external magnetic field using a control current (I_{CL}). The supercurrent I_C suddenly drops from a constant value (7.2 mA) to a minimum (about 0.8 mA for the sample shown in figure 2) when I_{CL} reaches a certain level (9 mA). At this field, one soliton (2π kink) is trapped in the junction; the even series disappears and the odd series appears simultaneously. The second method is very reproducible and figure 3 was obtained via this method.

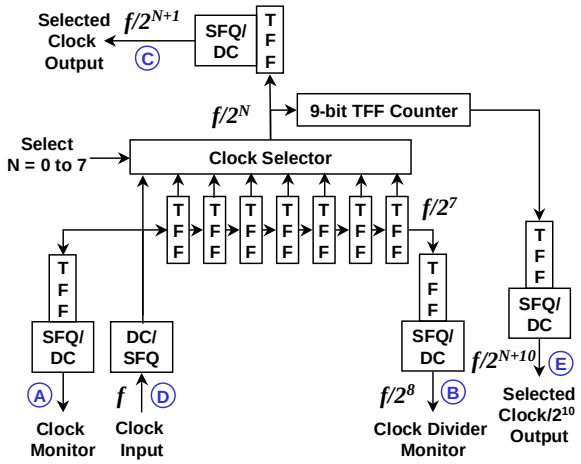

Figure 5. The clock-frequency selector circuit.

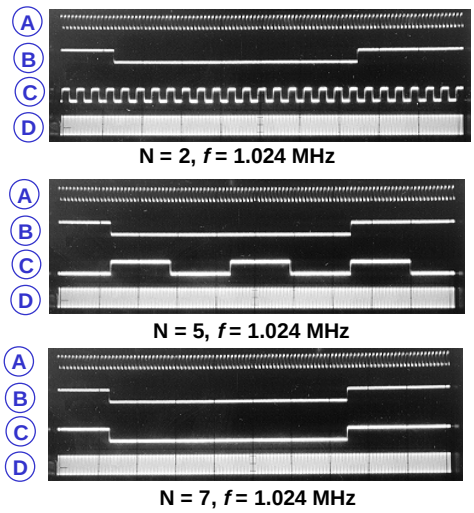

Figure 6. Four different selected clock outputs ('C' with a frequency of $f/2^{N+1}$) for $N = 2$, 5 and 7 are shown.

When we bias the LJJ on the soliton steps, we observe a digital output at the eighth TFF output. This indicates the fluxons in an annular LJJ can be successfully launched into a Josephson transmission line and coupled to RSFQ TFFs. With a microwave spectrum analyser, we measured the radiation frequency accurately from the TFF output. Figure 4 shows the radiation frequency at the eighth TFF output when the LJJ is biased on the first step shown in figure 3. Since each TFF divides the frequency by 2, we can calculate the oscillation frequency inside the LJJ as $f_S = f_8 \times 2^8$. An RSFQ pulse is generated in the first JTL junction J1 when the soliton in the LJJ passes the interface point. For a bias current of 6 mA, $f_8 = 152.96$ MHz, corresponding to $f_S = 39.16$ GHz, in good agreement with the first step voltage shown in figure 3.

3. Clock frequency selector

The performance of an ADC circuit is usually characterized over a wide range of sampling clock frequencies [1]. In order to incorporate an LJJ on-chip clock into the ADC circuit, a clock-frequency selector circuit was also developed. The clock selector circuit facilitates the circuit characterization as well as improving testability. The clock frequency is decimated using a chain of TFFs. The clock selector chooses either the master clock (f_m) or one of its binary sub-harmonics, based on the select inputs. We have implemented a version of this circuit where eight different clock frequencies ($f/2^N$, $N = 0, 1, 2, \ldots, 7$) can be generated and selected (figure 5). We added a 9 bit TFF counter to decimate the selected clock frequency down by a factor of 2^9 to be able to monitor the outputs (E) on a low bandwidth oscilloscope. Figure 6 shows selected clock outputs for $N = 2$, 5 and 7. The clock selector circuit also operates over a wide range of input clock frequencies. Figure 7 shows the selected clock outputs at different master clock frequencies.

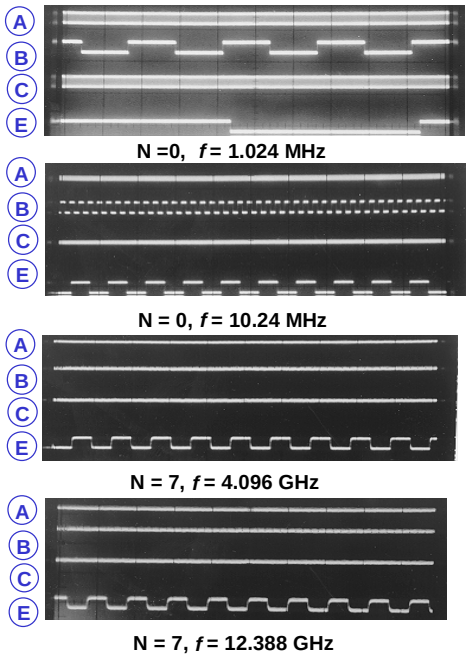

Figure 7. The selected clock outputs at different master clock frequencies.

4. Conclusions

In conclusion, our experiments confirm that an underdamped annular long junction can be used as a stable on-chip master clock for ADC circuits. Measurements from the LJJ/RSFQ hybrid circuit show clear resonant steps in the I–V curves. With one trapped soliton, the annular junction has a very *wide stable bias range* on the first soliton resonant step that has oscillation frequencies around 40 GHz. A 2π phase leap at the LJJ/JTL interface creates one RSFQ pulse during each oscillator period for the single soliton mode. We also developed a clock-frequency selector circuit that operates over a wide input clock frequency range.

Acknowledgments

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