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Recent progress in Ga$_2$O$_3$ power devices

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Abstract
This is a review article on the current status and future prospects of the research and development on gallium oxide (Ga$_2$O$_3$) power devices. Ga$_2$O$_3$ possesses excellent material properties, in particular for power device applications. It is also attractive from an industrial viewpoint since large-size, high-quality wafers can be manufactured from a single-crystal bulk synthesized by melt-growth methods. These two features have drawn much attention to Ga$_2$O$_3$ as a new wide bandgap semiconductor following SiC and GaN. In this review, we describe the recent progress in the research and development on fundamental technologies of Ga$_2$O$_3$ devices, covering single-crystal bulk and wafer production, homoepitaxial thin film growth by molecular beam epitaxy and halide vapor phase epitaxy, as well as device processing and characterization of metal–semiconductor field-effect transistors, metal–oxide–semiconductor field-effect transistors and Schottky barrier diodes.

Keywords: gallium oxide, Ga$_2$O$_3$, power devices, edge-defined film-fed growth, halide vapor phase epitaxy, molecular beam epitaxy

(Some figures may appear in colour only in the online journal)

1. Introduction

SiC and GaN power devices have attracted much attention as key components of the high-efficiency power conversion required for energy saving in the near future. Their device performance can far exceed that of the Si-based devices mainly used in current power electronics. However, SiC and GaN do not have to be the only candidates for next-generation power devices in the near future, because the materials and devices with the best performance and cost advantage should be chosen for society. Against this background, we have been proposing a new oxide compound semiconductor, gallium oxide (Ga$_2$O$_3$), as another promising candidate because of its excellent material properties and suitability for mass production.

The bandgap ($E_g$) and the expected Baliga’s figure of merit (FOM) of Ga$_2$O$_3$ are much larger than those of SiC and GaN. These outstanding material properties will in principle enable Ga$_2$O$_3$ power devices with even higher breakdown voltage ($V_{bd}$) and efficiency than their SiC and GaN counterparts.

SiC wafers are produced from bulk ingots typically grown using a sublimation method at extremely high temperatures above 2000°C. Various growth methods are being used for GaN bulk and/or wafer production, such as the high nitrogen pressure method, the ammonothermal technique and hydride vapor phase epitaxy; however, it is an open question which technique will dominate the market. As mentioned above, SiC and GaN wafers are produced from bulks synthesized by growth methods other than melt growth, because no atmospheric melt growth methods, which are standard for the production of semiconductor single-crystal bulks to date, are applicable for both SiC and GaN. However, in the case of Ga$_2$O$_3$, a single-crystal bulk can be synthesized using several standard melt growth methods; therefore, this is a strong advantage for Ga$_2$O$_3$ over SiC and GaN, in particular for mass production.

This review article mainly summarizes the recent progress in research and development (R&D) activities on this
emerging semiconductor Ga$_2$O$_3$ power device technology. Details about the above two attractive features of Ga$_2$O$_3$ will be introduced in the following sections. At present, the device technology is still at a primitive stage; however, the developed transistors and diodes with simple structures have verified its great potential for power devices.

2. Crystal structures of Ga$_2$O$_3$

The Ga$_2$O$_3$ single crystal is known to show five polymorphs, labeled α, β, γ, δ and ε [1]. Among the crystal structures, Ga$_2$O$_3$ mainly crystallizes in the monoclinic β-gallia structure with lattice constants of $a = 12.2$ Å, $b = 3.0$ Å and $c = 5.8$ Å as shown in figure 1. The β phase is the most stable structure, and the other phases are meta-stable ones. Note that the β-Ga$_2$O$_3$ is the only crystal structure that can be grown from the melt. Most of the reported scientific studies have been on the crystal growth and material properties of β-Ga$_2$O$_3$. The second meta-stable polymorph is α-Ga$_2$O$_3$ with a corundum structure, which is often stabilized by low-temperature heteroepitaxial growth on sapphire substrates [2, 3]. The heteroepitaxial growth of γ-Ga$_2$O$_3$ thin films, which has a defective-spinel structure, has also been reported [4, 5]. Formation of the meta-stable crystalline phases is strongly dependent on the substrate lattice and growth temperature. Typically, high growth temperatures lead to the formation of β-Ga$_2$O$_3$ even in the case of heteroepitaxial growth on foreign substrates. In this review, we focus on β-Ga$_2$O$_3$.

3. Material properties of β-Ga$_2$O$_3$

Some of the basic material parameters of β-Ga$_2$O$_3$ have not been fully studied and understood. There is great variability in the reported $E_g$ values, between 4.5 and 4.9 eV [6–9]. The n-type doping technology is relatively easy and mostly established. Sn and Si atoms are known to be shallow donors with small activation energies in Ga$_2$O$_3$. Electron densities (n) can be controlled in the wide range of $10^{15}$–$10^{19}$ cm$^{-3}$ [7, 8, 10, 11]. In contrast, there has been no report on effective hole conduction in Ga$_2$O$_3$. We consider that it is difficult to find acceptor atoms with a small activation energy since Ga$_2$O$_3$ is a wide bandgap oxide semiconductor. Furthermore, a very low hole mobility ($\mu$) prohibiting effective p-type conductivity in Ga$_2$O$_3$ was expected from the first-principles calculation of the Ga$_2$O$_3$ band structure [12–14]. Even in the worst case, tight localization of holes at specific sites in a Ga$_2$O$_3$ bulk was also predicted [15]. The thermal conductivity of Ga$_2$O$_3$ strongly depends on the crystal orientation due to its asymmetric crystal structure as shown in figure 1. The highest thermal conductivity of 0.27 W (cm K)$^{-1}$ can be obtained in the [010] direction, which is more than twice as large as that in the [100] direction [16]. However, even the [010] thermal conductivity of Ga$_2$O$_3$ is still much smaller than those of other semiconductors.

4. Advantages of Ga$_2$O$_3$ power devices from the material point of view

Here, we discuss why there is a real possibility that Ga$_2$O$_3$-based transistors and diodes can have excellent power device characteristics such as high $V_{br}$, high power, and low loss due to its material properties. Table 1 summarizes the physical properties of β-Ga$_2$O$_3$ and other major semiconductors for power devices. The Ga$_2$O$_3$ bulk electron $\mu$ of 300 cm$^2$ V$^{-1}$ S$^{-1}$ was estimated on the basis of the experimental data for the typical $n$ range of $10^{15}$–$10^{16}$ cm$^{-3}$ for the drift layers of vertical power devices [11, 17]. From the interpolation of the relationships among the $E_g$ and breakdown electric fields ($E_{br}$) of the other semiconductors, the $E_{br}$ of Ga$_2$O$_3$ is expected to have a very large value of about 8 MV cm$^{-1}$ [17]. The high $E_{br}$ is the most attractive property of Ga$_2$O$_3$, because the Baliga’s FOM, which is the basic parameter to show how suitable a material is for power devices, is proportional to the cube of $E_{br}$, but is only linearly proportional to $\mu$. The fundamental limits of on-resistances ($R_{on}$) as a function of $V_{br}$ for Ga$_2$O$_3$ and representative semiconductors are plotted in figure 2. It suggests that the conduction loss of Ga$_2$O$_3$ devices can be one order of magnitude lower than those of SiC and GaN devices at the same $V_{br}$. Therefore, we consider that Ga$_2$O$_3$ will best show its potential in unipolar devices.

5. Single-crystal Ga$_2$O$_3$ bulks and wafers

In general, large-diameter single-crystal wafers are required to mass produce vertical devices that are favorable for high-voltage and high-current power devices. Single-crystal Ga$_2$O$_3$ bulks have been synthesized by several melt growth methods such as the Czochralski [18, 19], the floating-zone (FZ)
and the edge-defined film-fed growth (EFG) [22] methods. In contrast, SiC and GaN bulk crystals are grown using methods such as sublimation, vapor phase epitaxy and high-pressure synthesis other than melt growth methods [23–25]. We propose that EFG has an advantage against the other melt growth methods regarding the bulk size, which is a key factor for high-volume production of large-size single-crystal Ga2O3 wafers. Figure 3 shows a photograph of a 4 inch diameter single-crystal Ga2O3 wafer produced from an EFG-grown Ga2O3 bulk. The crystal quality of Ga2O3 wafers prepared from EFG bulks has already been very good, with a full-width at half-maximum of the x-ray diffraction rocking curve (XRC) as narrow as 17 arcsec and a dislocation density on the order of 10^3–10^4 cm^−2 as characterized by surface etch pits. The wafer surface was atomically flat and smooth after chemical–mechanical polishing (CMP) with a small root-mean-square (rms) surface roughness of 0.11 nm. The good material workability of Ga2O3 is another important feature. Undoped Ga2O3 bulks show n-type conductivity due to unintentional Si incorporation from the Ga2O3 powder source. Thus, at present, compensation doping with deep acceptors such as Mg and Fe is required for the production of semi-insulating bulk crystals and wafers.

6. Epitaxial growth of Ga2O3 thin films

For the epitaxial growth of Ga2O3 thin films, there have been many reports on molecular beam epitaxy (MBE) [26–31], halide vapor phase epitaxy (HVPE) [32–35], metal–organic chemical vapor deposition [36–39] and mist chemical vapor deposition [2, 40]. In this section, the current status of our MBE and HVPE technologies for Ga2O3 thin film growth will be introduced.

6.1. MBE

At the time of writing this article, scientific studies on MBE growth have been the most advanced among the epitaxial growth techniques of Ga2O3 thin films. In general, normal gas-source MBE machines equipped with a turbo molecular pump are used for Ga2O3 growth. There are two types of oxygen sources used for the MBE growth of oxide semiconductors; one is oxygen radicals, generated by an radio-frequency (RF)-plasma cell [26–29], and the other is ozone [30, 31]. Our work on the ozone MBE growth of undoped and Sn-doped Ga2O3 films on native Ga2O3 (010) substrates will be described in the following [31].

<table>
<thead>
<tr>
<th>Material properties of major semiconductors and β-Ga2O3.</th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
<th>β-Ga2O3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$ (eV)</td>
<td>1.1</td>
<td>1.4</td>
<td>3.3</td>
<td>3.4</td>
<td>5.5</td>
<td>4.5–4.9</td>
</tr>
<tr>
<td>Electron mobility $\mu$ (cm^2 V s^−1)</td>
<td>1,400</td>
<td>8,000</td>
<td>1,000</td>
<td>1,200</td>
<td>2,000</td>
<td>300</td>
</tr>
<tr>
<td>Breakdown field $E_{br}$ (MV cm^−1)</td>
<td>0.3</td>
<td>0.4</td>
<td>2.5</td>
<td>3.3</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>Relative dielectric constant $\varepsilon$</td>
<td>11.8</td>
<td>12.9</td>
<td>9.7</td>
<td>9.0</td>
<td>5.5</td>
<td>10</td>
</tr>
<tr>
<td>Baliga’s FOM $\varepsilon \mu E_{br}^3$</td>
<td>1</td>
<td>15</td>
<td>340</td>
<td>870</td>
<td>24,664</td>
<td>3,444</td>
</tr>
<tr>
<td>Thermal conductivity (W cm K^−1)</td>
<td>1.5</td>
<td>0.55</td>
<td>2.7</td>
<td>2.1</td>
<td>10</td>
<td>0.27 [010] 0.11 [100]</td>
</tr>
</tbody>
</table>

Figure 2. Theoretical unipolar performance limits of $R_{on}$ as a function of $V_{br}$ for β-Ga2O3 and other major semiconductors power devices. Reproduced with permission from [17]. Copyright 2012, AIP Publishing LLC.

Figure 3. Photograph of 4 inch diameter single-crystal Ga2O3 wafer.
The specification of our ozone MBE machine used for Ga$_2$O$_3$ thin film growth is as follows. Ga and Sn (n-type dopant) are, respectively, supplied from Ga metal with six nines purity and four nines SnO$_2$ powder heated in conventional Knudsen cells. The oxygen source is an ozone (5%)–oxygen (95%) gas mixture generated by an ozone generator. One of the noteworthy advantages of ozone over RF-plasma is its high growth rate, reaching a few $\mu$m h$^{-1}$.

Figure 4(a) shows the surface morphologies of Ga$_2$O$_3$ epitaxial films grown at various temperatures by ozone MBE. The rms surface roughnesses of the Ga$_2$O$_3$ epitaxial films are plotted as a function of growth temperature ($T_g$) in figure 4(b). As shown in figure 4(a), step bunching along the [100] direction is observed for $T_g$ of higher than 700°C, and the surface becomes more rough with increasing $T_g$. A different type of
rough surface due to three-dimensional growth is shown for $T_e = 500^\circ C$. These experimental data indicate that 550–650$^\circ$C is the optimum window of $T_e$ for obtaining a smooth surface.

Next, the electrical properties of the ozone–MBE Ga$_2$O$_3$ films were characterized. The dependence of effective carrier concentration ($N_d$–$N_a$) on $T_e$ was characterized by using electrochemical capacitance–voltage ($C$–$V$) measurements. Figure 5 plots the $N_d$–$N_a$ depth profiles in three Sn-doped Ga$_2$O$_3$ epitaxial films grown at $T_e =$ 540, 570 and 600$^\circ$C. Uniform distributions of the doped Sn atoms along the growth direction were observed for the samples grown at $T_e =$ 540$^\circ$C and 570$^\circ$C. On the other hand, a delay in the Sn doping at the initial stage was confirmed for the sample grown at $T_e =$ 600$^\circ$C, which was likely to be due to Sn segregation. Therefore, the optimum $T_e$ for Sn-doped n-Ga$_2$O$_3$ films was determined to be 550–570$^\circ$C from the overlap of the growth conditions for the best structural and electrical properties.

6.2. HVPE

MBE is a very useful tool for scientific research, because we can obtain high-quality, high-purity epitaxial films by omitting the possibility of the incorporation of unintentional impurities. However, the productivity of MBE, which requires an ultra-high-vacuum atmosphere, is open to question. We chose HVPE from the several epitaxial growth methods as the first candidate for Ga$_2$O$_3$ thin film growth for future mass production of Ga$_2$O$_3$ epitaxial wafers. Ga$_2$O$_3$ HVPE R&D is still at a primitive stage; however, we have already established several important technologies [33, 34].

An atmospheric-pressure horizontal hot-wall HVPE system as schematically shown in figure 6 is used for Ga$_2$O$_3$ growth [33]. Currently, we use EFG-grown Ga$_2$O$_3$ (001) substrates for the HVPE growth. Based on thermodynamic analysis, GaCl and O$_2$ were determined to be appropriate precursors for Ga$_2$O$_3$ growth [33]. In the HVPE system, GaCl is generated by the reaction between high-purity Ga metal and Cl$_2$ gas at 850$^\circ$C in an upstream region of the reactor. The GaCl and O$_2$ are separately introduced into a growth zone using N$_2$ as a carrier gas, and the Ga$_2$O$_3$ substrate is placed on a quartz glass susceptor. The SiCl$_4$ dopant gas is simultaneously supplied in case of n-type Ga$_2$O$_3$ growth. The growth rate has been controlled up to as high as about 20 $\mu$m h$^{-1}$ without degradation of the material quality of the Ga$_2$O$_3$ epitaxial film [33]. Unintentionally doped (UID) Ga$_2$O$_3$ thin films grown by HVPE possess excellent structural and electrical properties, evidenced by an XRC peak as narrow as the one from the EFG bulk single crystal and an extremely low residual carrier concentration of less than $1 \times 10^{13}$ cm$^{-3}$ [34]. The n-type conductivity of Ga$_2$O$_3$ films can be controlled by the Si doping density in the wide range on the order of $10^{15}$ $\sim$ $10^{18}$ cm$^{-3}$. Details of the material and electrical properties of HVPE-grown n-Ga$_2$O$_3$ thin films will be reported elsewhere.

7. Ga$_2$O$_3$ transistors

7.1. Ga$_2$O$_3$ MESFETs

Transistor action for single-crystal Ga$_2$O$_3$ devices was first demonstrated using simple metal–semiconductor field-effect transistor (MESFET) structures [17]. By ozone MBE, a Sn-doped n-type Ga$_2$O$_3$ layer with a thickness of 300 nm was grown on a Mg-doped semi-insulating Ga$_2$O$_3$ (010) substrate. The Sn doping concentration was set at $7 \times 10^{17}$ cm$^{-3}$. The activation energy of Sn in Ga$_2$O$_3$ was estimated to be about 60–80 meV; therefore, about half of the Sn dopants were activated in the MBE-grown Ga$_2$O$_3$ layer at room temperature (RT). Figure 7(a) shows a cross-sectional schematic of the n-Ga$_2$O$_3$ MESFET. We employed a circular FET pattern as...
shown in figure 7(b). In the first process of ohmic contact formation, a reactive ion etching (RIE) treatment was performed using a gas mixture of BCl₃ and Ar followed by evaporation of Ti(20 nm)/Au(230 nm) and lift off. We found that the RIE process is effective in improving the ohmic contacts. Finally, Schottky gates were fabricated by Pt (15 nm)/Ti(5 nm)/Au(250 nm) deposition and lift off. Surface dielectric passivation was not performed for the device. The gate length, source–drain spacing and diameter of the inner circular drain electrode were 4, 20 and 200 μm, respectively.

Figures 8(a) and (b) show the dc output and transfer characteristics of the Ga₂O₃ MESFET, respectively. The drain current density (I_d) was effectively modulated by a gate voltage (V_g), and the device exhibited a perfect pinch off. The maximum I_d was 26 mA mm⁻¹ at a drain voltage (V_d) of 40 V and a V_g of +2 V. The three-terminal destructive breakdown in the off-state, which resulted in permanent degradation of the gate electrode, happened at a V_d of over 250 V. The maximum transconductance (g_m) was 2.3 mS mm⁻¹ for V_d = 40 V. The off-state drain leakage current was as small as 5 μA mm⁻¹, and the on/off I_d ratio reached about four orders of magnitude.

The Ga₂O₃ MESFET showed excellent device characteristics as the first FET demonstration. However, the devices also exhibited two clear issues. The most serious problem in the device characteristics was the high contact resistance of source/drain (S/D) electrodes. In addition, the I_d on–off ratio was limited by the small leakage current through the unpassivated Ga₂O₃ surface.

7.2. Depletion-mode Ga₂O₃ MOSFET version 1: MBE-grown Sn-doped Ga₂O₃ channel

To overcome the drawbacks of the MESFETs, we next fabricated depletion-mode Ga₂O₃ MOSFETs [41]. Figure 9 shows a schematic cross section of the Ga₂O₃ MOSFET. The Sn-doped Ga₂O₃ layer with a thickness of 300 nm was grown at 560°C on an Fe-doped semi-insulating Ga₂O₃ (010) substrate by ozone MBE. The device process started with multiple Si-ion (Si⁺) implantations to the regions under the S/D electrodes to form a 150 nm deep box profile with Si = 5 × 10¹⁹ cm⁻³, followed by activation annealing at 925°C for 30 min in an N₂ gas atmosphere. Then, a Ti/Au metal stack was deposited on the implanted regions and annealed again at 470°C for 1 min in an N₂ gas atmosphere. This metal annealing process is effective to further decrease contact resistance, probably due to the reaction between the metal and Ga₂O₃ at the interface. We obtained a specific contact resistance as low as 8.1 × 10⁻⁶ Ω cm² for the annealed contacts. Further details of the Si⁺ implantation doping in Ga₂O₃ and its application to the fabrication of low-resistance ohmic contacts are reported elsewhere [42]. A 20 nm thick Al₂O₃ gate dielectric and passivation film was formed on the Ga₂O₃ layer at 250°C by plasma atomic layer deposition. Note that the conduction band offset at the Al₂O₃–Ga₂O₃ interface was estimated to be about 1.5 eV [43]. The gate metal was formed with a Pt–Ti–Au stack on top of the Al₂O₃ film. The gate length and width were 2 μm and 500 μm, respectively. The spacing between the S/D Si⁺-implanted regions was 20 μm.

Figure 10(a) shows the dc output characteristics of the Ga₂O₃ MOSFET at RT. As in the case of the MESFET, the I_d was effectively modulated by V_g with good saturation and sharp pinch-off characteristics. Device self-heating caused by the poor thermal conductivity of Ga₂O₃ gave rise to the negative output conductance with increasing V_d. The maximum I_d was 39 mA mm⁻¹ at V_g = +4 V. The three-terminal off-state V₁r was as high as 370 V at V_g = -20 V. The I_d–V_g characteristic of the MOSFET at V_d = 25 V is shown in figure 10(b). The I_d on–off ratio was extremely high, exceeding ten orders of magnitude with the measured off-state leakage reaching the lower limit of the measurement.
instrument. These device characteristics were much superior to those of the Ga2O3 MESFETs.

We also investigated the performance of the Ga2O3 MOSFET at high-temperature operation. The device characteristics evolved smoothly with increasing device operating temperature. No kink or abrupt change that might be indicative of breakdown events and/or permanent degradation was observed, suggesting stable device operation in the whole temperature range from 25 to 250°C. The MOSFET maintained a high $I_d$ on–off ratio of about four orders of magnitude even at 250°C. Furthermore, the device characteristics were almost entirely recovered after operation at 250°C and cool down to RT.

7.3. Depletion-mode Ga2O3 MOSFET version 2: Si$^{+}$-implanted Ga2O3 channel

The Ga2O3 MOSFETs with a Sn-doped n-Ga2O3 channel suffered from reproducibility of the doping profile, because the suppression of the delay of Sn incorporation into the Ga2O3 at the initial stage of the MBE growth requires the precise control of $T_g$ in the narrow temperature window of 550–570°C. This issue led to both poor channel thickness control and non-uniform in-plane n. We addressed the problem in [44] by applying Si$^{+}$-implantation doping to not only the S/D electrodes but also the channel layer for reliable doping.

The device structure of the Ga2O3 MOSFET presented in this subsection was mostly the same as that of the Sn-doped-channel MOSFET shown in figure 9, except that the channel was formed by Si$^{+}$ implantation doping to a UID Ga2O3 layer grown by MBE. The thickness of the MBE-grown UID Ga2O3 layer was 300 nm, which was the same as the Sn-doped channel. The implanted Si atom densities in the channel layer and the S/D regions were $3 \times 10^{17}$ and $5 \times 10^{19}$ cm$^{-3}$, respectively. Multiple implantations were performed to obtain box profiles with depths of 300 nm for the channel and 150 nm for the S/D regions. Implant activation annealing was performed once at 925°C for 30 min in N$_2$ atmosphere for both the channel and S/D regions. After the implantation and activation process, all fabrication procedures were identical to those employed for the Sn-doped-channel Ga2O3 MOSFETs.

All the device characteristics of the Si$^{+}$-implanted-channel MOSFETs were almost the same as or slightly improved over those of the Sn-doped-channel Ga2O3 MOSFETs. Figures 11(a) and (b) show the dc output and breakdown characteristics of the Ga2O3 MOSFET with a gate length of 4 μm at RT. The maximum $I_d$ was 65 mA mm$^{-1}$ at
$V_g = +6\text{ V}$. The three-terminal off-state $V_{br}$ was as high as 415 V at $V_g = -30\text{ V}$. The off-state $I_d$ remained below the detection limit prior to device breakdown. At $V_d = 30\text{ V}$, a high $I_d$ on–off ratio of about ten orders of magnitude was achieved, and the maximum $g_m$ was 3.6 mS mm$^{-1}$. Figure 12 plots the temperature dependence of the transfer characteristics at $V_d = 30\text{ V}$ of the MOSFET. The presented devices with the Si$^{+}$-implanted channel also revealed stable operation up to 250°C as did the devices with the MBE-grown Sn-doped channel. The MOSFETs maintained a low drain leakage current of less than 5 $\mu$A mm$^{-1}$ and a high $I_{on}$ on–off ratio of about four orders of magnitude at 250°C.

8. Ga$_2$O$_3$ Schottky barrier diodes (SBDs)

8.1. Ga$_2$O$_3$ SBDs fabricated on UID Ga$_2$O$_3$ native substrates

For the purpose of evaluating the basic device performance of Ga$_2$O$_3$ SBDs, we first fabricated simple SBD structures on a...
UID Ga2O3 (010) substrate with a thickness of 600 μm, which were produced from an FZ-grown bulk crystal [45]. The substrates showed n-type conductivity due to the unintentionally incorporated Si in the Ga2O3 powder source. The 100 μm diameter circular Schottky anode electrodes were fabricated on the front side of the substrate with a Pt–Ti–Au stack. Next, BCl3/Ar RIE treatment was performed on the whole back area of the substrate, and the cathode electrode of Ti/Au was evaporated onto it. These were the same procedures employed for the MESFET to fabricate S/D ohmic contacts [17].

Note that n was uniform along the thickness of the substrate but showed in-plane variation from $3 \times 10^{16}$–$1 \times 10^{17}$ cm$^{-3}$ as evaluated by C–V measurements. The in-plane distribution of n was caused by a non-uniform Si atom density, which was attributed to the characteristic of the Ga2O3 FZ growth. Here, we introduce device characteristics of the two selected SBDs having different n of $3 \times 10^{16}$ cm$^{-3}$ and $5 \times 10^{16}$ cm$^{-3}$, which were fabricated at different locations on the same substrate. The forward current density–voltage (J–V) characteristics of the SBDs are shown in figures 13(a) and (b). The near-unity ideality factors of 1.04–1.06 were estimated for both devices, indicating the high crystal quality of the FZ Ga2O3 substrate and good Schottky interface property. A Schottky barrier height of 1.3–1.5 eV was extracted for the Pt–Ga2O3 interface from the semi-logarithmic-plotted J–V and $1/C^2$–V characteristics. The $R_{an}$ of the Ga2O3 SBDs, which were determined from the slopes of the linear regions in figure 13(a), were relatively high at 7.85 and 4.30 mΩ⋅cm$^2$ because of the low conductivity of the bulk substrate. Figure 13(b) shows the reverse J–V characteristics of the Ga2O3 SBDs. The reverse $V_{br}$ values were 150 and 115 V for $n = 3 \times 10^{16}$ and $5 \times 10^{16}$ cm$^{-3}$, respectively, which were reasonably high for the n and the simple device structure.

8.2. Ga2O3 SBDs fabricated on HVPE-grown n–Ga2O3 drift layers

Recently, we started development on full-scale Ga2O3 SBDs with the advancement of the HVPE technology [33, 34]. The Ga2O3 SBDs were fabricated on epitaxial wafers with HVPE-
grown Si-doped \( n^-\)-Ga\(_2\)O\(_3\) drift layers on \( n^+\)-Ga\(_2\)O\(_3\) (001) substrates. SiCl\(_4\) was simultaneously supplied during the growth as an \( n^-\)-type dopant gas. The growth rate of the Ga\(_2\)O\(_3\) epitaxial layers was set at 10 \( \mu \text{m} \text{h}^{-1}\). After the HVPE growth, the surfaces of the epitaxial layers were rough with many pits; therefore, the CMP process was performed to flatten the surfaces. The thickness of the post-CMP drift layer was about 7 \( \mu \text{m}\).

A schematic cross section of the SBD structure is shown in figure 14. The depth profiles of \( N_d-N_a \) extracted by the \( d(1/C^2)/dV \) method in two \( n^-\)-Ga\(_2\)O\(_3\) epitaxial layers grown with different SiCl\(_4\) flow rates were almost constant at 1.4 \( \times 10^{16} \) cm\(^{-3}\) and 2.0 \( \times 10^{16} \) cm\(^{-3}\), respectively. Figure 15(a) shows the forward \( J-V \) characteristics of the SBDs. From linear fits to the slopes within the range of \( J = 100-200 \) A cm\(^{-2}\), the specific \( R_{on} \) were estimated to be 3.0 m\( \Omega \cdot \text{cm}^2\) for the device with \( N_d-N_a = 1.4 \times 10^{16} \) cm\(^{-3}\) in the drift layer and 2.4 m\( \Omega \cdot \text{cm}^2\) for the one with \( N_d-N_a = 2.0 \times 10^{16} \) cm\(^{-3}\). Note that the \( R_{on} \) values included a substrate resistance as large as 1.0 m\( \Omega \cdot \text{cm}^2\). The ideality factors of the SBDs were 1.03–1.07, indicating that the Pt/HVPE-grown Ga\(_2\)O\(_3\) interface followed the ideal thermionic emission theory. The reverse \( J-V \) characteristics shown in figure 15(b) reveal a high \( V_{br} \) of around –500 V for both SBDs. Note that hard breakdown events happened with catastrophic damage in both devices due to electric-field concentration at the edge of the anode electrodes. Therefore, implementation of edge termination designs such as a field plate and/or a guard ring to the presented device structure should lead to further improvement in \( V_{br} \).

9. Conclusion

This paper has attempted to give a review of the present status of R&D on new wide bandgap semiconductor Ga\(_2\)O\(_3\) power devices. Ga\(_2\)O\(_3\) bulk single crystals can be synthesized by several melt growth methods, and large-size, high-quality Ga\(_2\)O\(_3\) wafers produced from the EFG bulk have already been available up to the 4 inch diameter size. Among several
epitaxial growth techniques, MBE and HVPE succeeded in producing device-quality Ga$_2$O$_3$ epitaxial wafers. Significant progress has been made in the development of Ga$_2$O$_3$ transistors and diodes in the last few years, and the device characteristics demonstrated the great potential of Ga$_2$O$_3$ power devices for future high-power and high-voltage applications. We consider that vertical transistors and diodes operating at the voltage range of higher than 3 kV will be the main target for Ga$_2$O$_3$ power devices in future R&D. However, Ga$_2$O$_3$ devices are not limited to the power device applications and thus should also be developed for several different application fields such as high-frequency and extreme environment electronics. Further efforts and progress in R&D on Ga$_2$O$_3$ devices should pave the way for next-generation semiconductor electronics.

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**References**


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