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Reduced microwave attenuation in coplanar waveguides using deep level impurity compensated Czochralski-silicon substrates

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Abstract

We show that deep level doping of Czochralski-grown silicon wafers is capable of providing high resistivity handle wafers suitable for radio frequency integrated circuits. Starting from n-type Czochralski silicon wafers having a nominal resistivity of 50 $\Omega \cdot \text{cm}$, we use ion implantation and subsequent annealing to increase the resistivity of the wafers to over 10 k$\Omega \cdot \text{cm}$ at room temperature. Coplanar waveguides fabricated on implanted wafers show strongly reduced attenuation down to 0.3 dB mm$^{-1}$ from 0.8 dB mm$^{-1}$ for un-implanted wafers in the 1–40 GHz range, providing clear evidence that the technique is effective in improving performance of passive devices at GHz range frequencies.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The need for high resistivity silicon substrates for making passive devices and analog and mixed signal radio frequency integrated circuits (RFIC) working at GHz range frequencies has been underlined in the International Technology Roadmap for Semiconductors (ITRS) [1]. The key issue is to minimize the background free carrier concentration, which is directly proportional to the conductivity of the substrate to improve the RF performance of the devices fabricated on them. Float zone (FZ)-technique-grown silicon is a straightforward solution for resistivities up to about 10 k$\Omega \cdot \text{cm}$ [2], but costly as its diameter is limited to 8” [3]. An alternative approach has been to use insulating substrates, which showed some success. The major problems in this case were device failure [4] due to unequal thermal expansion between the handle and the active wafers at internal device operating temperatures of 85 °C and above, and complications in device design for using materials such as sapphire [5, 6], or even air [7] as the handle material.

Our approach is to make high resistivity Czochralski (Cz) technique grown Si through deep level compensation [8] for use as a handle wafer which will remove the difficulties mentioned above. We have already shown that it is possible to achieve very high resistivities starting from low resistivity Cz-Si wafers using gold [9, 10] and manganese [11] doping. A recent technological review [12] recognized the novelty of our approach and commented that compatibility with Si very large scale integration (VLSI) processes was awaited. In order to address this issue, in this work we use ion implantation and in-diffusion of Au for compensation of shallow background donors in Cz-Si to show a large reduction in microwave attenuation in the 1–40 GHz range using coplanar waveguides (CPWs) fabricated on the implanted wafers. This is the first direct evidence that the method of deep level doping in Cz-Si...
2. Calculations

A typical CPW structure as shown in figure 1 was used to calculate analytically the RF signal attenuation. There are three main loss mechanisms: resistive conductor losses in the metal tracks \( \alpha_c \), losses due to absorption in the substrate \( \alpha_d \), and losses caused by charge carriers at the dielectric–substrate interface \( \alpha_i \) resulting in a total attenuation \( \alpha \), expressed in dB per unit length as

\[
\alpha = \alpha_c + \alpha_d + \alpha_i. \tag{1}
\]

The frequency-dependent conductor losses, \( \alpha_c \), are mainly due to resistive losses in the metal tracks. For our ratio of track width, \( w = 50 \, \mu\text{m} \), signal to ground spacing, \( s = 34 \, \mu\text{m} \), and Al track thickness, \( t_m = 500 \, \text{nm} \), the resistive losses [13] in dB per unit length as

\[
\alpha_c = \frac{8.68 [\phi(w) + \psi(w + 2s)]}{240\pi K(k)K'(k)(1 - k^2)} R_S \sqrt{\varepsilon_{eff}} = 1.04 R_S \sqrt{\varepsilon_{eff}} \tag{2}
\]

where the numerator and the denominator are solely determined by geometrical design, and the factor \( R_S = (\mu_0 \pi f \rho)^2 \), where \( \mu_0 \) is the permeability of free space, \( \rho \) is the metal resistivity and \( f \) is the frequency. The dielectric losses of the semiconductor have a small intrinsic component, which is negligible even for high resistivity substrates, and a free carrier component. For substrates much thicker than the CPW dimensions, the substrate losses, \( \alpha_d \), can be expressed as [13]

\[
\alpha_d = \frac{2.17}{\rho_s} \sqrt{\frac{\mu_0}{\epsilon_0 \varepsilon_{eff}}} \tag{3}
\]

where \( \rho_s \) is the resistivity of the substrate material.

In order to determine the attenuation experimentally, two-port S-parameters were measured, and the attenuation constant was determined using the relation

\[
\alpha_{\text{expt}} = -\frac{10}{l} \log_{10} \left( \frac{|S_{21}|^2}{1 - |S_{11}|^2} \right) \tag{4}
\]

where \( l \) is the length of the CPW in mm.

3. Experimental results and discussions

We chose 6" diameter, 675 \( \mu\text{m} \) thick, phosphorous (P) doped n-type (100) Cz-Si wafers from MEMC with a nominal resistivity of 50–60 \( \Omega \text{cm} \) as the starting material. A 20 nm sacrificial oxide was grown using dry oxidation at 950 \( ^\circ\text{C} \) for 28 min in a Tempres furnace to provide protection against implantation damage. Gold was implanted at 100 keV through the oxide layer into either the polished or the backside of the wafer with doses of 1, 2, and 4 \( \times 10^{13} \text{cm}^{-2} \). Subsequently, wafers were annealed for 1 h at 950 \( ^\circ\text{C} \) in Ar, followed by oxide layer removal by wet etching in buffered HF until hydrophobic.

Resistivities of the wafers were then measured at 20 \( ^\circ\text{C} \) by the four-point probe (FPP) technique. Samples of 1 \( \text{cm}^2 \) dimension were cleaved from the wafers for spreading resistance profiling (SRP), and secondary ion mass spectroscopy (SIMS). CPWs were fabricated using evaporation to deposit a 500 nm thick aluminum layer, followed by photo-lithographic patterning using a contact aligner to give a signal width line of 50 \( \mu\text{m} \) and a ground-signal spacing of 34 \( \mu\text{m} \). The pattern was subsequently etched using an Al etchant at 40 \( ^\circ\text{C} \) for 2 min.

Sets of CPWs of four different lengths, 0.8, 1.6, 3.2 and 6.4 mm, were fabricated. A Cascade Microtech Summit 12 000 probe station, with infinity ground-signal-ground probes, and an Agilent E8631A vector network analyzer, calibrated using an impedance standard substrate (ISS), were used for microwave measurements. The ISS contained Au CPWs of dimensions identical to our waveguides on an alumina substrate having a resistivity of 1 \( \times 10^{14} \Omega\text{cm} \).

Diffusion of Au in Si is dominated by the kick-out mechanism [14] and leads to a U-shaped Au profile [9]. This is clearly evident in the Au SIMS profiles taken both at the front and the backside of the wafer as shown in figure 2. The SIMS detection limit for Au is a few times 1 \( \times 10^{11} \text{cm}^{-3} \).

The integrated doses of the as-implanted (not shown) profiles agree with the nominal doses to within 1%.
Figure 3. Spreading resistance profiles of Au-implanted and 950 °C annealed Si samples with different implantation doses as given in the legend. SRP was done from the front and backsides of the samples.

Table 1. Measured FPP resistivities at 20 °C of the front and backsides of Cz-Si wafers implanted with different doses of Au and annealed at 950 °C for 1 h in Ar ambient.

<table>
<thead>
<tr>
<th>Side of wafers measured</th>
<th>Resistivity (kΩ cm) for various gold implantation doses (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 x 10¹³</td>
</tr>
<tr>
<td>Implanted</td>
<td>4.2</td>
</tr>
<tr>
<td>Un-implanted</td>
<td>4.0</td>
</tr>
</tbody>
</table>

which proves the quantitative nature of the SIMS calibration. For the lowest dose SIMS profiles, the implanted (front) side and the un-implanted (back) side of the wafers are practically identical whereas for the higher doses large concentrations of un-diffused or immobile Au are seen at a depth of around 0.3 μm below the front sides of the wafers, reminiscent of the as-implanted profile. The immobile Au might either be related to damage-induced defects or to the solubility limit of Au being reached at the annealing temperature of 950 °C, which was chosen as the lowest temperature at which all Au might dissolve.

The FPP resistivity values of the as-implanted (un-annealed) samples were identical to those before implantation. The post-anneal resistivities increased considerably and are given in table 1. The highest resistivity obtained was 18 kΩ cm for an implantation dose of 4 x 10¹³ cm⁻². Even though the front and backside resistivities are roughly similar, it is seen that the backsides show slightly higher values, demonstrating that the immobile Au is not active and even hampering resistivity enhancement.

Resistivity profiles of the samples measured by the SRP technique are shown in figure 3. It is found that Au-doped Si has steeply varying symmetric U-shaped resistivity profiles as predicted. Compared to the FPP resistivities, the peak values obtained from SRP are somewhat lower, but in view of the complicated scaling methods [15] applied to obtain SRP resistivity from measured values of resistances, the discrepancy is not serious. Both the techniques show that the resistivity increases with increase in the Au implantation dose. The U-shaped profile of the diffused Au allows implantation of Au from the backside of SOI wafers to increase the resistivity directly under the buried oxide and the active layer as long as the oxide provides a good barrier against diffusion.

The S-parameters of the CPWs were measured using both an un-implanted Si starting wafer and the deep level impurity-doped wafers with resistivity up to 15 kΩ cm. The results are plotted in figure 4 as a function of the lengths of the CPWs at 1, 10, and 40 GHz. For both the low and high resistivity wafers, the attenuation is proportional to the length of the waveguide, as is expected from well-designed waveguides. The frequency dependence of the measured attenuation is shown in figure 5 where the result of measurements of a CPW on an impedance standard substrate (ISS) is included for comparison. It is clearly seen that the Au deep level doping reduces the attenuation, and at 40 GHz it is lowered from about 0.8 to 0.3 dB mm⁻¹, a decrease of more than 60%. The CPW of the ISS shows an even lower attenuation of about 0.15 dB mm⁻¹. As discussed earlier, the conductor loss scales inversely with the skin depth of the metal track and so inversely
4. Conclusions

High resistivity Cz-Si substrates were made from standard, low resistivity, n-type Si through deep level Au doping using ion implantation and in-diffusion anneal. SIMS profiles, SRP and FPP measurements are in good agreement with one another indicating resistivities in excess of 10 kΩ cm at room temperature. The typical U-shaped Au doping profile resulting from the kick-out diffusion mechanism demonstrates that back implantation is effective for introducing Au into the handle wafer. Microwave measurements on CPWs show that the increased resistivity levels lead to a more than 60% decrease in attenuation in CPWs. The fact that the processes used in our work are Si VLSI-compatible takes the principle of deep level dopant compensation in Si closer to a technologically viable highly demanded [1, 12] novel material.

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