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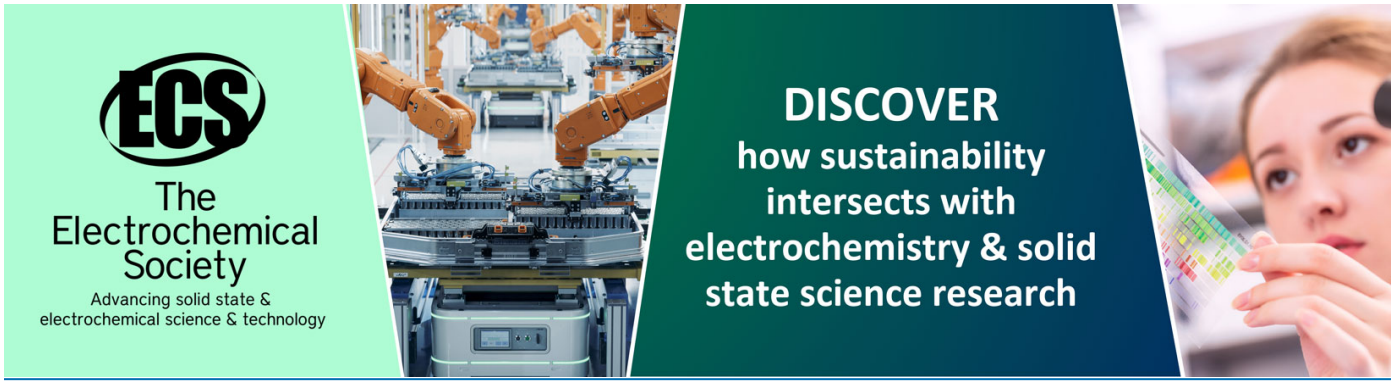

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Fast and precise algorithms for calculating offset correction in single photon counting ASICs built in deep sub-micron technologies

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ABSTRACT: An important trend in the design of readout electronics working in the single photon counting mode for hybrid pixel detectors is to minimize the single pixel area without sacrificing its functionality. This is the reason why many digital and analog blocks are made with the smallest, or next to smallest, transistors possible. This causes a problem with matching among the whole pixel matrix which is acceptable by designers and, of course, it should be corrected with the use of dedicated circuitry, which, by the same rule of minimizing devices, suffers from the mismatch. Therefore, the output of such a correction circuit, controlled by an ultra-small area DAC, is not only a non-linear function, but it is also often non-monotonic. As long as it can be used for proper correction of the DC operation points inside each pixel, it is acceptable, but the time required for correction plays an important role for both chip verification and the design of a big, multi-chip system. Therefore, we present two algorithms: a precise one and a fast one. The first algorithm is based on the noise hits profiles obtained during so called threshold scan procedures. The fast correction procedure is based on the trim DACs scan and it takes less than a minute in a SPC detector systems consisting of several thousands of pixels.

KEYWORDS: Pattern recognition, cluster finding, calibration and fitting methods; Simulation methods and programs; Large detector-systems performance

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1 Introduction

New designs of hybrid pixel detectors, working in the single photon counting (SPC) mode, are going in the direction of increasing the single pixel functionality while decreasing its size. One of the disadvantages of this approach is that matching of smaller blocks decreases even if we go to smaller technologies, what usually helps making the same device less spread in the chip. However, designers would rather increase the functionality further than increase the area just for better matching. Therefore, the offset spread of DC operating points between channels exists, and designers challenge this problem proposing adequate compensation circuits in specific points of the signal processing path [1, 2]. Considering the binary readout circuit containing the discriminator, different correction circuits are used for minimization of the mismatch effect usually at the discriminator input, which is the critical point for a globally set threshold voltage. An example of a prototype circuit designed in CMOS 180 nm is presented together with the correction procedure results.

Taking into account the pixel size minimization, the correction DACs quality is often degraded. Ultra-low area correction DACs are not only nonlinear but they are often non-monotonic [3, 4]. The large multi-thousand channel systems require proper calculation of the correction DACs values in order to make the whole system uniform and to apply common threshold to all pixels. Non-monotonic DACs characterization is a time consuming process and therefore effective and fast correction algorithms are required. We have developed fast correction algorithms, which are able to calculate proper values of correction DACs in systems containing several thousands of pixels in less than a minute. The details of elaborated methods are presented together with examples of measuring result.

2 The offset spread in multichannel system

The key feature of multichannel sensor systems is that all the channels should be as uniform as possible while taking into account the technology imperfections. In the case of hybrid pixel detectors working in SPC mode with energy windowing, the spread of the DC offset, which can be distinguished at the discriminators input together with the spread of the gain in the analog processing path, are critical. Increasing the single pixel functionality together with decreasing its size requires reducing the area of analog blocks. Using smaller technology node generally increases matching of devices of the same dimensions, however, at some point, the spread cannot be minimized further, as the variation of device parameters seems to stabilize at certain points. For example the variation of a threshold voltage of a NMOS transistor can be written as

$$\sigma^2(V_T) \approx (A_{VT})^2/WL$$

where the V_T is a threshold voltage of an NMOS transistor, A_{VT} is a variation proportionality constant of threshold voltage, W and L are the width and length of the transistor in certain technology nodes. The figure 1 shows the A_{VT} in different technologies, and as it can be seen, the value stabilizes at around 3 mVμm making perfect matching impossible [2]. In nanotechnologies there are several new effects, which must be taken into account: poly-silicon gate morphology, litho spread, pockets or helo implants, hot carrier effects, etc. [2, 5, 6].

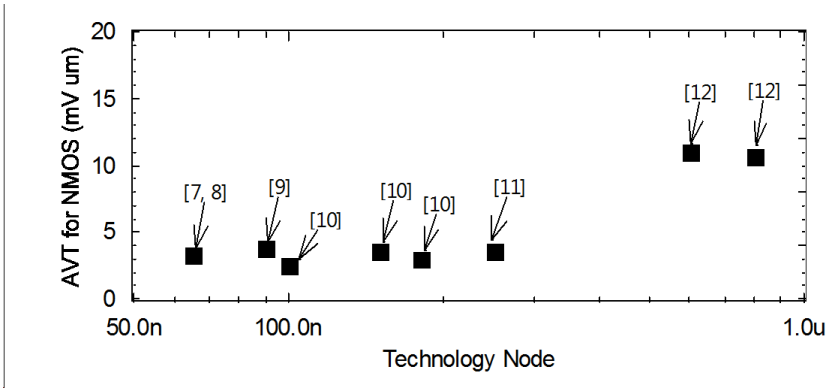

Figure 1. The threshold voltage variation proportionality constant of NMOS transistor in different technology nodes.

3 Trim DACs characteristics

As a mismatch of the devices always exists, the designers tools, which can help make an array of uniform sensors, are digital correction circuits able to compensate the mismatch. There is a small margin for optimization between the device size and acceptable offset spread, which can be corrected by the trimming circuits. An example here could be a prototype circuit, which is a hybrid pixel detectors readout ASIC working in SPC mode and built-in CMOS 180 nm. As the pixel size is small ($100\times100\,\mu$m^2) and increased functionality (energy window, continuous readout, etc.) is an important factor, the correction circuit should be as small as possible but has to allow for

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correction of the DC offset in a certain range. The necessary resolution and range of the correction DACs is taken from the Monte Carlo (MC) simulations during the design stage or it is based on earlier measurement results [13, 14]. The discriminator threshold applied is common for all discriminators, but the difference in gain, discriminator offset and DC level in each pixel causes a significant spread of the effective threshold voltage in the whole pixel matrix. To reduce this spread of the effective threshold voltage there is an additional 7-bit correction block at the input of DC coupled AMP stage (figure 2a). The trim block uses two source followers with a coupled control of their bias currents. The trim DAC current I_{trim} is subtracted from the first branch (source follower M1) and is added to the second one (source follower M2). As a result the DC differential voltage at the discriminator input should be a "more linear" function of the trim DAC current. The figure 2 shows simulated characteristics of VA (figure 2b) and VB voltages (figure 2c) and a subtraction of those voltages as an effective correction characteristic (figure 2d).

However, due to imperfections of the technology, the mismatch of transistors, used in the current sources, is significant, and the DC level at discriminator input is not only a non-linear function of the trim DAC current, but it is also non-monotonic. An example of a trim DACs characteristics (DC level at the discriminator input as a function of trim DAC value) are shown in figure 3. The area of a 7-bit trim DAC (7 binary weighted current sources and switches) is only $20\,\mu\text{m}\times 5.2\,\mu\text{m}$.

Despite of the imperfections of the presented characteristics, the important question is if these DACs can be used for effective correction of DC offsets. From figure 3 one can see that the range is adequate (nearly all trim DACs characteristics cross the horizontal line at about 200 mV). The quality of correction depends on the real resolution and an algorithm used for calculations.

4 Correction algorithms

The design of a trim DAC is only the first step in the hardware offset correction. The second important step is implementation of a fast and effective algorithm to find the proper values of trim DACs, which results in minimum offset spread from pixel to pixel. Few methods can be distinguished, two of which (one basing on trim DACs characteristic and the second basing on trim DACs scan) are described below.

4.1 Precise correction algorithm

The trim DACs characteristics give the full information about the behavior of the correction circuit in each pixel and allow for immediate calculation to minimize any offset spread. However, the characterization of trim DACs is a time consuming process. During this procedure the threshold voltage is changed within a certain range, which allows noise hits counting in each pixel for each value of trim DAC (figure 4b). Then the noise counts profiles are fit to a Gaussian distribution and the peak position (max of noise counts) is calculated. The peak position for each pixel versus trim DAC value defines the trim DAC characteristic (figure 4c). The trim DAC characterization requires steps presented on the diagram (figure 4a). Having the characteristics makes it easy to set the value of the trim DAC in each pixel, which moves the peak positions (maximum of noise counts) to the same value of threshold even for non-monotonic characteristics.

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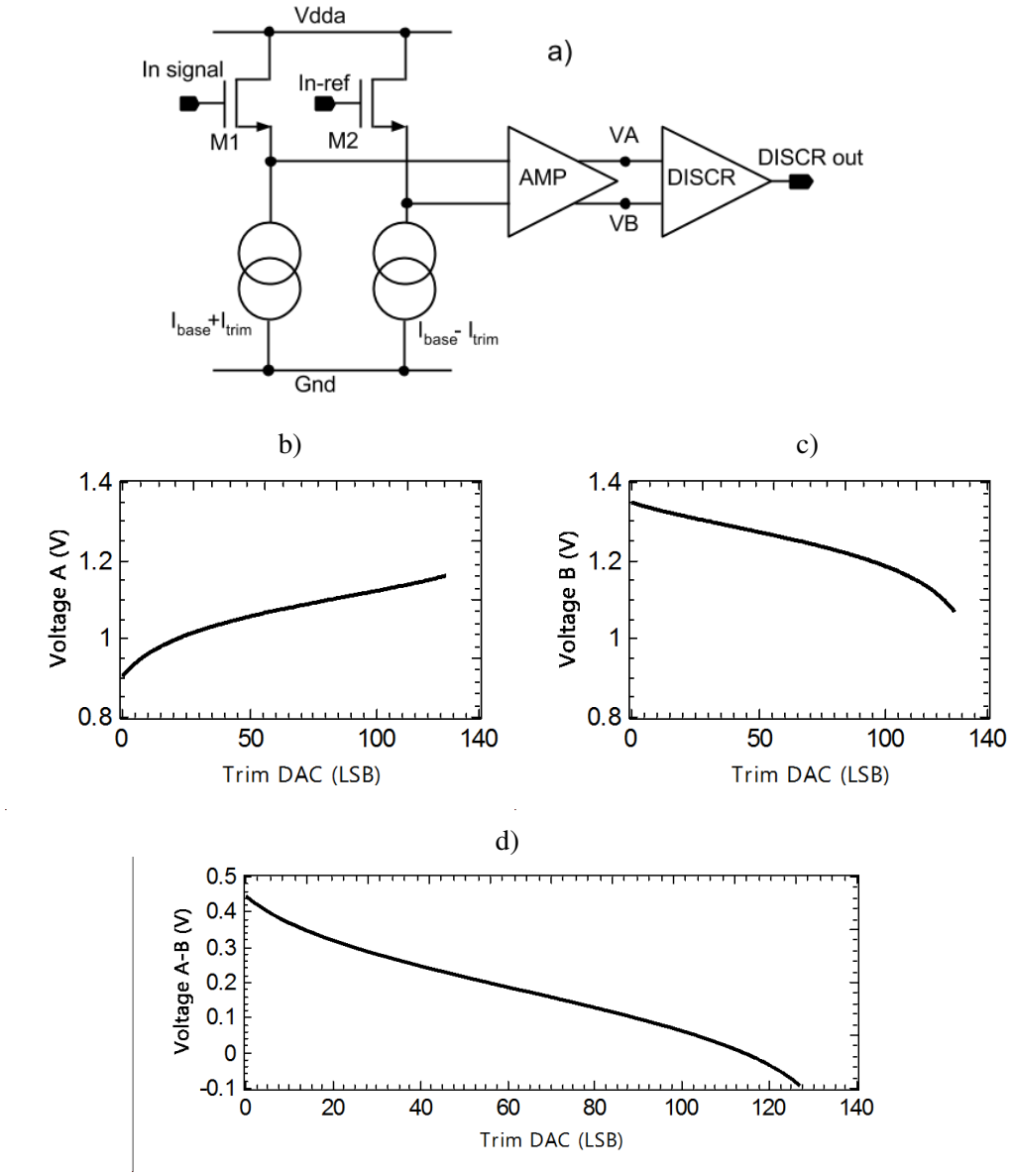

Figure 2. a) The simplified scheme of the trim block used in the example prototype IC, b) simulated voltage VA, c) simulated voltage VB, d) simulated trim DACs characteristic.

The whole procedure requires precise measurement of noise counts so that measured profiles can be fitted to a Gaussian distribution. Assuming the measurement of the trim DACs characteristics in the whole range, for each step within the trim DAC the threshold scan measurement is done with a resolution of 1mV in the wide range of 0.5 V. This gives 500 steps, which is done for each value of trim DACs (128 times). Each threshold scan requires an additional fitting of 18432 channels to the Gaussian distribution, what results in more than 2,350,000 fittings together with 64,000 measuring steps. Assuming 100 ms per step, the measuring time equals 100 minutes, however the fitting time must be added and it varies due to the algorithm used, processor speed, etc. In our case the total time for trim DAC characteristics measurements is about 2 hours.

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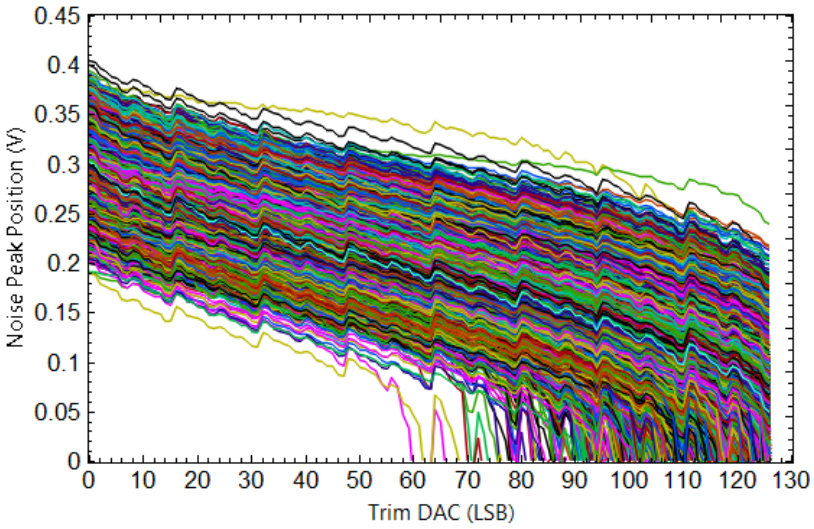

Figure 3. The trim DACs characteristics for 18432 channels of a prototype ASIC.

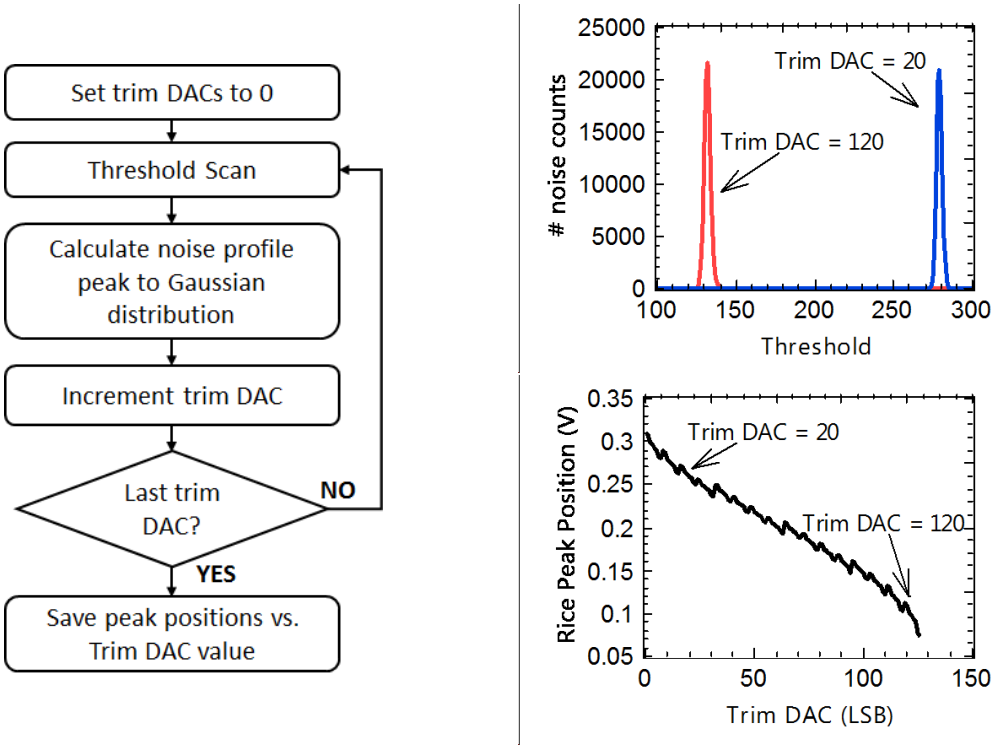

Figure 4. The algorithm for trim DACs characteristic measurement: (a) the algorithm, (b) single pixel noise counts for two different settings of trim DAC (c) trim DAC characteristic for one pixel.

4.2 Fast correction

It is possbile to ommit the trim DACs characteristic measurements and just do a so-called trim DACs scan (figure 5a). This procedure was used in the Pilatus trimming procedure [15], however it requires a monochromatic X-ray beam of certain energy and assumes linear characteristics of

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trim DACs. If the trim DACs are linear, the scan of noise hits should give similar results of noise counts distribution as in the case of threshold scans. The same will apply for the energy peak position — during trim DACs scan the profile could be fit to s-curve. However, due to nonlinear trim DAC characteristics, the obtained distribution of noise counts cannot be fitted to a Gaussian function. More importantly, if the characteristic is non-monotonic, like in the described case, the plots obtained have several local maximums (following points are not "in right sequence" — see figure 5b), and it is very hard to recover it properly as the large number of channels make large number of exceptional cases for different algorithms. Therefore, one way for the fast correction calculation is to find the peak with the maximum number of noise counts (which is very close to the peak position in the precise correction algorithm, but without fitting to a Gaussian distribution).

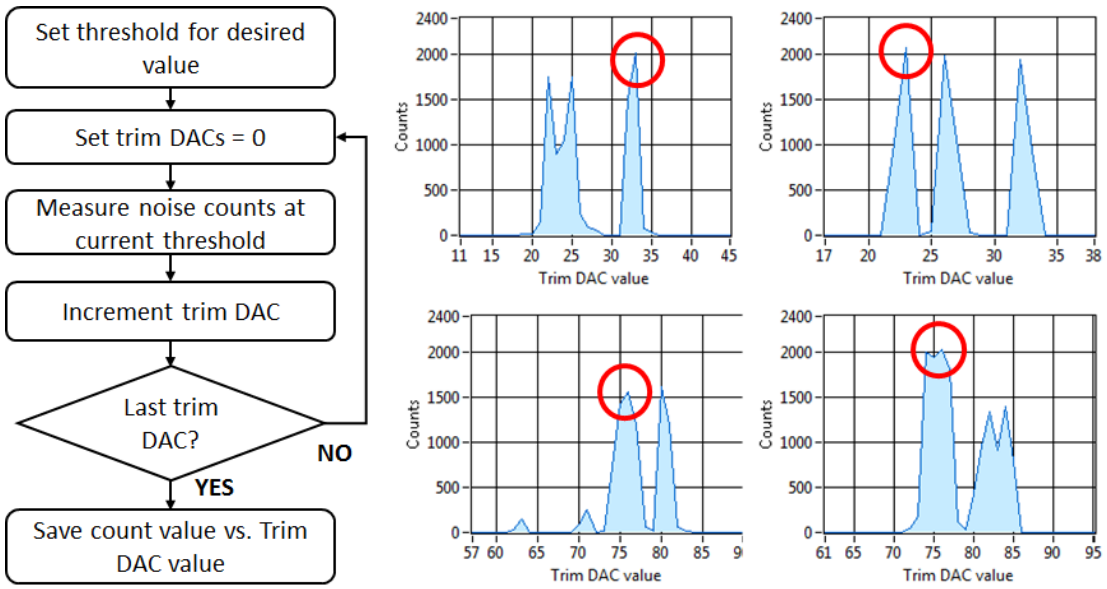

Figure 5. Fast correction algorithm: (a) the algorithm, (b) trim DACs scans for different pixels with the maximum value marked.

5 Measurements

Both methods for precise and fast correction were implemented in LabVIEW^{TM} and are used for automatic operation. Both were measured for performance with several prototype chips. A example result of noise peak position before and after correction procedure for 18432 pixels with the use of 7-bit trim DAC is presented on figure 6. The precise correction procedure for the presented results took about 2 hours and resulting spread is reduced from $\sigma = 29.54$ mV rms down to $\sigma = 1.91$ mV for all pixels. The fast correction was able to reduce the initial spread down to $\sigma = 2.70$ mV in 40 seconds (only 128 measuring steps with 100 ms per step). This time will scale linearly with the trim DACs length, e.g. 5-bit DAC can be corrected in 10 sec. Of course in the case of fast correction the resulting spread is a bit higher than in the case of trim DACs characteristics, but the time was reduced down to 40 seconds making the picture uniform enough for final application.

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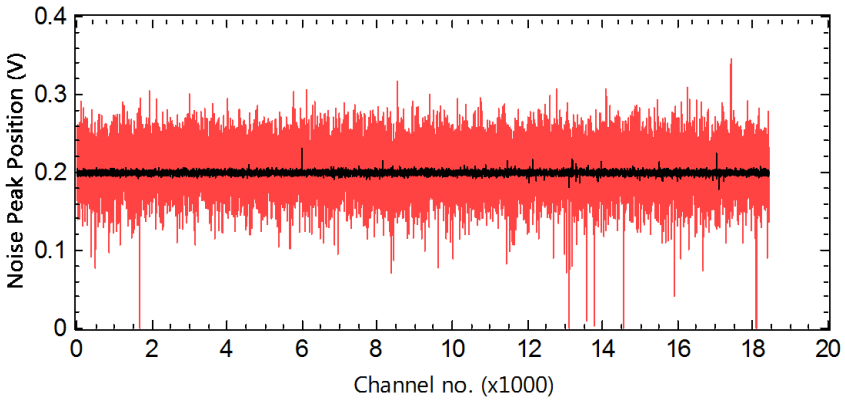

Figure 6. The noise peak position before correction (red plot) and after correction with the use of 7-bit correction DACs (black plot) for 18432 pixels.

6 Summary

The paper discusses a uniformity limitations of a large area multi-channel ASIC for hybrid pixel X-Ray detector binary readout. The source of those limitations is the technology itself and therefore dedicated in-pixel correction circuits for trimming the offsets are required. A multi-thousand channel prototype circuit was presented, for which two dedicated algorithms for calculating proper trimming DACs values are used. The precise one uses the trim-DACs characterization procedure, which takes a long time, but can be used further for re-calculating settings for different criteria. The fast one however, uses the noise counts for effective trimming of each pixel and, as presented, it takes less than a minute to perform the entire procedure. Measurements prove the usability of the fast correction algorithm for practical application.

Acknowledgments

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