OPEN ACCESS

Analysis of packaging effects on wire bonder made microtransformer chips

To cite this article: A Moazenzadeh et al 2013 J. Phys.: Conf. Ser. 476 012110

View the article online for updates and enhancements.

You may also like

- <u>Transfer printing of nanomaterials and</u> <u>microstructures using a wire bonder</u> Xiaojing Wang, Stephan Schröder, Alessandro Enrico et al.
- <u>Development and Optimization of Thin-Film Technology Based Micro Inductors</u> and <u>Transformers</u> Sebastian Beringer, Dragan Dinulovic, Martin Haug et al.
- <u>Fully Integrated Spiral-type</u> <u>Microtransformers on a Silicon Substrate</u> Jae Y. Park and Jong U. Bu





DISCOVER how sustainability intersects with electrochemistry & solid state science research



This content was downloaded from IP address 3.147.73.12 on 03/05/2024 at 20:49

Analysis of packaging effects on wire bonder made microtransformer chips

A Moazenzadeh¹, S H Moosavi², N Spengler¹, R Zeiser² and U Wallrabe¹

¹ Laboratory for Microactuators, Department of Microsystems Engineering (IMTEK), University of Freiburg, Georges-Koehler-Allee 102, 79110 Freiburg, Germany. ² Laboratory for Assembly and Packaging Technology, Department of Microsystems Engineering (IMTEK), University of Freiburg, Georges-Koehler-Allee 103, 79110 Freiburg, Germany.

wallrabe@imtek.uni-freiburg.de

Abstract. We present the fabrication and characterization of microtransformer chips, based on wire bonded microcoils which are encapsulated in a Polydimethylsiloxane (PDMS) package. Our investigations focused on the degradation in electrical performance due to the higher dielectric constant of PDMS compared to air. We further studied the thermo-mechanical induced strain on the system due to thermal expansion of the package at temperatures up to 250° C. According to the measurements, encapsulating the chips decreased the resonance frequency and the quality factor near the resonance. However, both the maximum quality factor and the power efficiency were not affected by the encapsulation. Furthermore, induced thermo-mechanical strains due to the mismatched coefficients of thermal expansion of the chip and the packaging materials did not decrease the mechanical integrity of the SU-8 post and the coil itself.

1. Introduction

The trend towards further miniaturization of electronic devices makes the integration and miniaturization of reliable power convertors indispensable. Hence much effort has been spent to increase the performance of the on chip inductors and transformers. The effects of using low-k polymers for the encapsulation of the radio frequency (RF) inductors have been investigated before in several publications [1,2]. However, increase in the capacitance of the inductor chip as a result of the packaging could compromise the performance in very high frequency regime (VHF) (30-300 MHz) as well and needs further investigation.

The fabrication of wire bonder made microcoils [3] and microtransformers [4–6] has been reported before. Apart from the increase in processing speed and the additional flexibility, manufactured devices are among the best microinductors due to the high performance in terms of inductance density, coupling factor and power efficiency [5]. In this paper, we report a method for the encapsulation of the wire bonder made microtransformer chips in PDMS for protection of the delicate wires and bonds. Meanwhile we investigate two important aspects related to the added packaging to the chips: the influence on the electrical performance and also the reliability of the chips at high temperatures.

The encapsulation of microtransformer chips provides a practical solution in order to protect them from external mechanical shocks. It also makes the chip handling easier, especially for further processes like the assembly into the target circuit. However, replacing air (ε_r =1) with a dielectric material (ε_r >1)

Content from this work may be used under the terms of the Creative Commons Attribution 3.0 licence. Any further distribution $(\mathbf{\hat{H}})$ (cc` of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI. Published under licence by IOP Publishing Ltd 1

in an inductor-based system, results in an increase of the capacitance and therefore parasitic losses of the chip. Also, induced strain due to the differences in coefficients of thermal expansion (CTE) of the chip and the packaging materials results in additional thermo-mechanical stress on the chip. Therefore, further investigations of the reliability at increased temperatures are needed.

2. Fabrication

For the fabrication, a 4 inch borosilicate wafer was gold-metallized via electroplating to implement 12 µm thick supply tracks and bond pads (figure 1a). Using a thick SU-8 process defined an array of 650 µm high cylindrical posts as well as a frame around the chip (figure 1b). After a short O₂-plasma cleaning step a modified, automated ball-wedge wire bonder (WB 3100plus, ESEC, Switzerland) was employed to wind two solenoids, each with 20 windings, in a helical trajectory around the posts (figure 1c). The coils themselves were stable, however, in order to provide a physical protection for the coils and their bond connections, Sylgard[®] 184 PDMS (Dow Corning Corp., USA) was used as the packaging material. Besides the low volume shrinkage, its dielectric constant of 2.65 is lower than of most epoxies and other silicone materials [7]. The PDMS was statically dispensed into the SU-8 frame at a temperature of 80 °C, and subsequently cured at 70 °C for 2 hours in an oven to form the package (figure 1d). Details for the fabrication have been reported in [5].





3. Measurement and discussion

3.1. Packaging effects on the electrical performance

To investigate the effect of the encapsulation on the electrical performance, seven identical chips were electrically characterized before and after the encapsulation. The high frequency characterization of the transformers was performed using a 2-port on-wafer measurement method.

Encapsulating the chips led to an increase in capacitance (*C*), while the inductance (*L*) of the chip stayed constant. As a result, based on the formula (1) the resonance frequency (f_{\circ}) decreased (fig. 2).

$$f_{\circ} = \frac{1}{2\pi\sqrt{LC}} \qquad (1)$$

The quality factor also decreased near the resonance (fig. 3) as a result of the increased internal capacitance of the inductors, respectively. However, below 100 MHz, the quality factor was not influenced, and it's maximum of approx. 64% appeared at a constant frequency of f=85 MHz. Finally, the power efficiency was hardly affected by the encapsulation (fig. 3). Details of the measured values for the seven identical chips, before and after the packaging are summarized in the table 1.



Figure 2. Measured inductance of the primary solenoid of seven identical transformer chips before and after the encapsulation. The resonance frequency was decreased by 21% after the encapsulation.



Figure 3. Measured Q-factor (left) and power efficiency (right) of the primary solenoid of seven identical transformer chips before and after the encapsulation.

Table 1. Average values for the measurements of the chips, before and after the PDMS encapsulation.

	L(nH)	Q_{\max}	$\eta_{max}(\%)$	Resonance
Before packaging	404±4	23.40±0.5	63.59±2.39	-
@ <i>f</i> (MHz)	1	85	61	312±3
After packaging	406±5	23.33±1.21	64.03±2.31	-
@ <i>f</i> (MHz)	1	84	60	258±2

3.2. Verification of the thermo-mechanical induced strain

To check the thermo-mechanical reliability of the package, the induced strain was measured at different temperature stages, using the Digital Image Correlation technique (DIC) where the 3D expansion of the

chip was recorded and analyzed. Absolute behavior in each thermal stage can be achieved with precision of $1 \,\mu$ m.

During the measurement procedure, the sample was kept in a vacuum oven with a transparent lid, where the temperature was increased from room temperature up to 250°C in steps of 25°C. The final results revealed that the expansion of the PDMS package did not decrease the mechanical integrity of the SU-8 post and the coil (figures 4 and 5). Figure 4 (a-c) show that the package expanded around 40 μ m in the Z direction, whereas it was around zero for the SU-8 post on which the solenoids were wire bonded. Fig. 4 (d-f) show the strain in X, and fig. 4 (g-i) in Y direction. They represent a compression between the two points on the SU-8 post and on the package in each temperature stage.

Figure 5 reveals, that the induced shear strain in the XY plane mainly appeared at the package frame, instead of the solenoids or the bonds at 250°C.



Figure 4. The package behaviour at temperature ramps. (a-b) the displacement of the chip at 250°C with respect to the room temperature. (c) The displacement of two points on the SU-8 post and on the package going through different temperature stages. (d), (e), (g) and (h): The strain imposed on the chip in the X and Y direction at 250°C. (f-i): The strain exposed on the two points on the SU-8 post and on the package going through different temperature stages in the X and Y direction respectively



Figure 5. Shear strain measurement at 250°C

4. Conclusion

We present a successful packaging approach for the wire bonded miniaturized microtransformer chip by using PDMS as an encapsulation material. According to the measurements, encapsulating the chips decreased the resonance frequency and also the quality factor near the resonance. However, both the maximum quality factor and the power efficiency were not affected by the encapsulation. Studying the induced thermo-mechanical strain due to the thermal expansion of the PDMS up to 250°C showed that the package expanded around 40 μ m in the Z direction. This value was around zero for the SU-8 post on which solenoids were wire bonded. Furthermore, induced thermo-mechanical strains due to mismatched coefficients of thermal expansion of the chip and the packaging materials did neither affect the mechanical integrity of the SU-8 posts, nor electrical connectivity of the wire bonds.

Acknowledgments

This work was supported by DFG graduate school *Embedded Microsystems* under grant Number 1103.

References

- [1] Choi Y, Yoon E and Yoon J 2003 Encapsulation of the micromachined air-suspended inductors *Microwave Symposium Digest* pp 1637–40
- [2] Carchon G, Raedt W and Beyne E 2004 Wafer-level packaging technology for high-Q on-chip inductors and transmission lines *Microw. Theory Tech.* **52** 1244–51
- [3] Kratt K, Badilita V, Burger T, Korvink J G and Wallrabe U 2010 A fully MEMS-compatible process for 3D high aspect ratio micro coils obtained with an automatic wire bonder *J. Micromechanics Microengineering* **20** 015021
- [4] Moazenzadeh A, Spengler N and Wallrabe U 2013 High-performance, 3D-microtransformers on multilayered magnetic cores *Micro Electro Mechanical Systems (MEMS)*, 2013 IEEE 26th International Conference on (Taipei) pp 287–90
- [5] Moazenzadeh A, Spengler N, Lausecker R, Rezvani A, Mayer M and Korvink J G 2013 Wire bonded 3D coils render air core microtransformers competitive J. Micromechanics Microengineering 23
- [6] Raimann M, Peter A, Mager D, Wallrabe U and Korvink J G 2012 Microtransformer-Based Isolated Signal and Power Transmission *IEEE Trans. Power Electron.* **27** 3996–4004
- [7] Schneider F, Fellner T, Wilde J and Wallrabe U 2008 Mechanical properties of silicones for MEMS *J. Micromechanics Microengineering* **18** 065008