Peak current failure levels in ESD sensitive semiconductor devices and their application in evaluation of materials used in ESD protection. Part 2: Experimental verification

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Peak current failure levels in ESD sensitive semiconductor devices and their application in evaluation of materials used in ESD protection. Part 2: Experimental verification

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Abstract. This paper gives experimental demonstration that the method described in Part 1 of the paper, using data from Human Body Model test on devices, can be used to estimate an ESD pulse current threshold for damage to ESD energy susceptible semiconductor devices. The technique is intended for laboratory evaluation of ESD threats from equipment, materials and other ESD sources in the electronics assembly factory environment. The predicted ESD current damage threshold is demonstrated to give a useful boundary to a "safe" area of ESD current and duration.

1. Introduction

The evolution of electronics and semiconductor technology has led to devices with ever smaller dimensions in order to achieve greater circuit density, greater performance and higher frequencies. With reduction in internal dimensions, the devices have become more sensitive to electrostatic discharge (ESD) events since the late 1990s. The current trend, which is expected to continue, is for circuit performance at the expense of on-chip ESD protection level [1]. This is pushing more emphasis on reducing ESD exposure on the manufacturing floor to allow safe handling of ESD sensitive devices during manufacturing. Cost effective reduction of ESD exposure in electronics manufacturing from the basic level set up in international standards for the ESD control [2,3] requires quite detailed understanding of mechanisms that cause device damage. The device technology is today at the nanoscale frontier and, accordingly, modern device physics is, from the ESD control standpoint [4], far from the macroscopic ESD control in the electronics assembly environment [2,3]. That sets the goal for this paper, which is to bridge the gap in understanding between device physics and assessment of ESD risks at electronics manufacturing.

The paper consists of two parts. In Part 1 of the paper [5] we showed that theoretical analysis of the thermal model of damage to ESD energy susceptible devices, combined with the data from standard Human Body Model (HBM) [6] tests on devices, can be used to estimate an ESD pulse current threshold for damage to ESD energy susceptible semiconductor devices. Part 2 gives an experimental verification of the validity of this approach. The current threshold concept we proposed in Part 1 has been evaluated by investigating damage to example devices using range of ESD waveforms derived

from Resistor-Capacitor (RC) and Transmission Line Pulse (TLP) generators. The standard HBM pulse is a particular implementation of the RC generator with values C=100 pF, R=1500 Ω.

The technique presented in the paper is intended for laboratory evaluation of ESD threats from equipment, materials and other ESD sources in the electronics assembly factory environments. Examples are given in Section 4 that how the ESD current damage threshold is used to assess ESD threat from charged garments and ESD threats related to automated handling equipment in device assembly process.

2. Experimental arrangements

A device under test (DUT) was placed in the output circuit of a simple ESD generator, Fig. 1, which consisted of a pulse forming network (PFN) and high voltage source. The PFN was charged to a preset voltage. An ESD pulse was initiated by closing the mercury wetted relay switch causing current to flow in the load circuit consisting of the series resistance R, the DUT and current measurement equipment. The latter consisted of a 50 Ω transmission line connected to a matched 50 Ω input of a digital storage oscilloscope.

Two types of PFN were used. When exponential decay RC waveforms were required, the PFN was a capacitor and a series resistor R was connected in the load circuit. The duration of the pulse was controlled by the RC time constant. An ESD current pulse with desired peak value and duration was obtained by varying the capacitor value C, PFN charging voltage V and resistor R. Several capacitors and resistor values were available to obtain desired ESD pulse characteristics, including approximately the standard HBM values.

When rectangular TLP waveforms were required, an appropriate length of coaxial cable formed the PFN. An additional shunt resistor was tied to ground in parallel with a series resistor R to prevent mismatch and departure from the desired rectangular waveform. The duration of the pulse was controlled by the length of the cable used, and the peak current controlled by the charging voltage.

For RC pulse durations were measured from 50 % of the rising edge to 37 % of the falling edge of the peak current corresponding to the theoretical time constant RC. Peak value was estimated by extrapolation of the falling edge of the waveform ignoring any overshoot. For TLP pulses we measured the peak current as the average of the plateau, and the duration as the time between 50 % of peak current for rising and falling edges. RC pulse durations of 13, 35, 52, 70, 98, 135, 190, 320, 560 or 1060 ns and TLP pulse durations of 4, 6, 12, 21, 32, 51 or 102 ns were measured without the device test fixture in the circuit. The presence of devices did not have significant effect on ESD waveforms, except in one case (HVC134). Rise times for HBM and TLP pulses were similar, in the range 0.5-2 ns, and depended to some extent on the device under test.

The ESD current through the DUT was conducted through a 50 Ω coaxial cable and recorded by an oscilloscope for the measurement of peak discharge current and ESD duration. The operation of the DUT was tested after each ESD event.

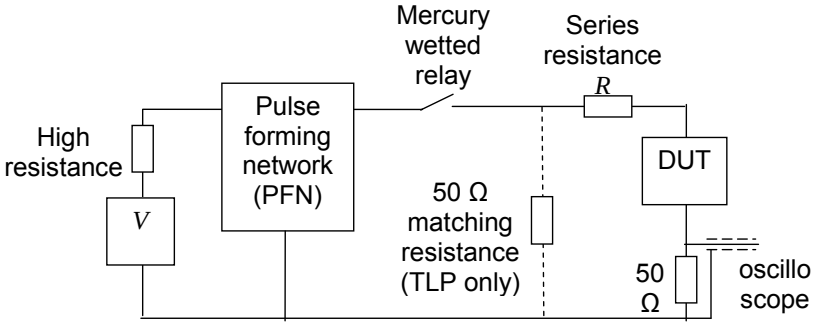

Figure 1 Circuit of the ESD generator. The PFN components, series resistance R and the charging voltage V were varied to obtain the ESD current with desired peak value and duration.

The device testing procedure followed to that described in the HBM standard [6], with the exception that only positive pulses were applied into the DUT. Three new devices were tested for each ESD duration to avoid any step stress hardening effects of the devices.

Five devices were selected for testing (Table 1). All devices were surface mount packaged devices except a Schottky diode 5082-2835. Device failure was judged by measuring the reverse leakage current of the stressed junction with a Keithley 6517A electrometer. Failure criteria were chosen according to maximum leakage currents specified on data sheets. In most cases the devices failed with leakage current increasing abruptly by several orders of magnitude. Further experiments showed that devices did not recover after such failure.

Table 1. Devices selected for trials

Device	**Datasheet ESD information (if available)**	**Failure criteria**
Agilent 5082-2835 Schottky diode		Max. reverse leakage current I_r = 100 nA @ V_r = 1 V
Philips BFT-25 NPN RF transistor		Abrupt change in leakage current I_{eb} @ V_{eb} = 2 V
Agilent ATF-34143 PHEMT	Class 1 (<2000V) HBM EIA/JESD22-A114-A	Max leakage current I_{gss} = 300 μA
Hitachi HVC 134 PIN diode	200 V (C=100 pF, R = 1.5 kΩ) Both forward and reverse direction	I_r > 0.1 μA at V_r = 60 V
Agilent HSMS-2820 Schottky diode		Max. reverse leakage current I_r = 100 nA @ V_r = 1 V

3. Experimental results

3.1. Measurement of device failure characteristics

HBM withstand voltages were measured for each type of device using the RC arrangement (C=115 pF, *R*=1484 Ω) approximating the HBM standard values (Table 2). This combination in practice produced a measured 190 ns duration pulse.

The HBM withstand voltages (V_{HBM}) and corresponding current withstand thresholds (I_{fHBM}) calculated according to formula $I_{fHBM} = V_{HBM}/1500\Omega$ [5] are listed in Table 2. Measured current withstand thresholds are also presented. Because there was significant peaking in some waveforms, the overshoot was visually eliminated by extrapolation from the measured maximum current values. This, in addition to extra impedance due device and oscilloscope, reduces measured I_{fHBM} compared to the calculated value.

Table 2. HBM withstand voltages and currents for selected devices

Device	**V_{HBM} (V)**	**Calculated I_{fHBM} (mA)**	**Measured I_{fHBM} (mA)**
5082-2835	400	267	220
BFT-25	700	467	420
ATF-34143	350	233	200
HVC-134	400	267	50
HSMS-2820	900	600	510

The measured current at the withstand value I_{fHBM} is in most cases a little below the calculated value. In the case of the HVC 134 it was significantly less than calculated. This indicates that the device resistance can sometimes have significant effect. On failure, at V_{HBM} = 500, the current through the HVC 134 device increased to 300 mA which is comparable with the expected 330 mA peak current at that voltage level.

3.2. RC and TLP current damage thresholds

The results of RC and TLP ESD tests on the five selected device types are shown in Figure 2. First the I_{fHBM} point was plotted. Then $t^{-0.5}$ and $t^{-0.25}$ current damage threshold curves were added as described in Part 1 of our paper [5]. Finally the test results were plotted. Each data point indicates the result of one test.

The current damage thresholds can be seen to give most cases a reasonable estimate of the onset of device damage for RC waveforms. In every case, an assumption that these lines give the boundary of safe ESD current and duration would be expected to provide protection of the devices. In general, given the likelihood of statistical differences between devices of each type, we believe the results show remarkably good agreement with the theory.

For TLP pulses, the current threshold for failure is also depending on the failure mode of device and is given either by I_f=0.7I_{fRC} or by I_f=I_{fRC}, where I_{fRC} is the current threshold according to Eq. (1) for a RC pulse duration, t_{ESD}, equal to the duration of the TLP pulse [5]. From Figure 2 we can see that TLP damage occurred below these limits in the cases of the 5082-2835, BFT 25, ATF34143 and HSMS 2820 devices. In most cases TLP damage occurred above or on the predicted 0.7 I_f lines. An exception was the HVC134 device where the TLP damage occurred slightly above the I_f=I_{fRC} line and follwed the $t^{-0.5}$ dependence at ESD durations shorter than t_{HBM}. In general, we believe again that the results show remarkably good agreement with theory.

For the HVC134 device, at longer RC durations below the destruction level, the peak current through the device was much less than expected, being of the order tens rather than hundreds of mA. This shows that the device resistance was high and limited the current up until the point at which destruction occurred.

In no case was there any evidence of a t^{-1} dependent region emerging at low pulse durations [5]. This confirms that the non-adiabatic regime for these sensitive devices extended to the lowest pulse durations (4 ns) we used.

4. Application of the current threshold in ESD control

We propose that in assessing ESD threats from a material, process or automated handling line, the HBM ESD withstand peak current is a primary specification. The material or equipment should not be able to source an ESD peak discharge current exceeding this threshold. As an example, if the most sensitive device to be handled has a 100 V HBM withstand, the peak ESD current from any ESD source must not exceed 0.067 mA at 150 ns duration, appropriately derated for other ESD durations.

As an example, a survey of such discharges may be made as a part of the material or equipment laboratory qualification procedure. Use of the current threshold gives a possibility also to assess risks associated with direct ESD from charged insulators in the cases where the presence of insulators near or in contact with ESDS cannot be avoided, for example, at special process stages in automated handling equipment, etc [7] (assessment of risks due to electrostatic fields from charged insulators at large is a more complex issue which required different treatment). The ESD current can be measured using a proper discharge probe connected either directly or through a current transformer to a high bandwidth oscilloscope. We have used this technique to evaluate the likelihood of ESD damage occurring due to discharges from charged ESD garments used in electronics manufacture [8] as well as from different materials commonly used in automated assembly lines [9,10] (see the references for more details and example ESD waveforms).

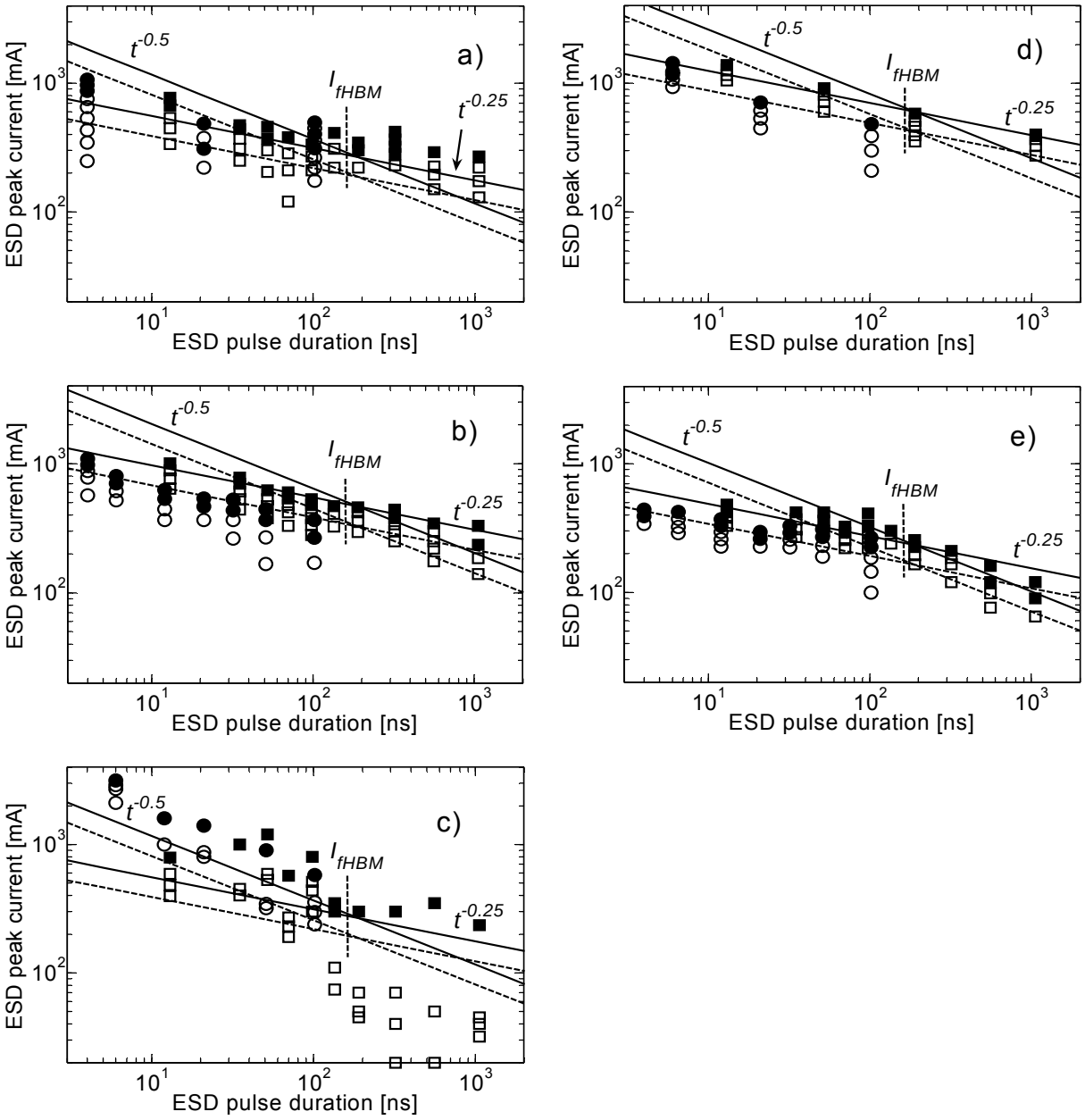

Figure 2 ESD test results for a) 5082-2835 Schottky diode, b) BFT-25 RF transistor, c) ATF-34143 PHEMT transistor, d) HSMS -2820 Schottky diode and e) HVC134 PIN diode: (○) TLP no damage, (●) TLP damage, (□) RC pulse no damage, (■) RC pulse damage, (- - -) 0.7 I_f.

5. Conclusions

The results show that for the five devices tested the predicted ESD current damage thresholds derived from HBM ESD data gave good indication of the onset of damage in real devices. The predicted $t^{-0.25}$ and $t^{-0.5}$ dependences of the ESD pulse current damage threshold with pulse duration corresponded well with our experimental results. The damage current threshold variation with duration was best described by the $t^{-0.25}$ curve for the Schotky diodes and RF transistor, and by the $t^{-0.5}$ curve for the PIN diode. The PHEMT damage threshold appeared to be described by the lower of the $t^{-0.5}$ and $t^{-0.25}$

curves. In general TLP rectangular pulse damage occurred at lower peak ESD current levels than RC pulse damage, as predicted by our model.

These results confirm that to define an "ESD safe" area bounded by $t^{-0.5}$ and $t^{-0.25}$ curves calculated from HBM withstand data would be a useful general guide for all the components tested. When evaluating ESD risk from practical sources it is unnecessary for many purposes to account for an adiabatic region in evaluating ESD risk. Instead it is safe to use the $t^{-0.25}$ current limit at low ESD durations as this current limit is lower than the expected damage threshold current in the adiabatic regime.

While the RC current threshold I_f gave a reasonable boundary for ESD damage from the RC sources used in this work, a margin of safety would be achieved by using a lower current threshold of 0.7 I_f to account for the possibility of more severe waveforms.

The current damage threshold cannot be considered to be a reliable rule that is applicable in every case, but should instead be considered a useful guide that may be valuable in a range of ESD risk situations that are otherwise difficult to assess. It is of the nature of tools for research and expert assessment rather than simple factory test methods. Nevertheless we believe it will provide a rational means of assessment of ESD risks to energy susceptible devices in a wide range of situations, processes and materials.

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