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2007 Sci. Technol. Adv. Mater. 8 231

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SCIENCE AND TECHNOLOGY OF ADVANCED MATERIALS

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# Porous silicon and aluminum co-gettering experiment in p-type multicrystalline silicon substrate

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Received 8 August 2006; received in revised form 17 January 2007; accepted 1 February 2007
Available online 10 May 2007

**Abstract**

The lifetimes of non-equilibrium minority carriers, which bound with the diffusion length, are considered as two important parameters of the low-quality multicrystalline silicon (mc-Si) substrate. Its value defines the quality of the initial substrate. It is also subjected to change as a result of many high-temperature operations during the device fabrication. Therefore, it is necessary to incorporate certain processing steps that either improve or preserve the electronic quality of the mc-Si substrate. In this study, a novel porous silicon and aluminum co-gettering experiment has been applied as a beneficial approach to improve the electronic quality of the low-resistivity mc-Si substrates. Porous silicon layers were prepared by anodization of the $n^+$ silicon region by a simple electrochemical etching process using an aqueous HF-based electrolyte, which leads to the creation of porous silicon microcavities. Besides making porous silicon and aluminum co-gettered samples, both phosphorous and aluminum alloy-gettered samples and reference samples were made. The gettering-induced lifetime enhancement in the test samples was monitored by measuring the lifetime/diffusion length of the test samples using two independent methods such as photoconductivity decay (PCD) measurement and the photocurrent generation method (PCM), respectively. The result in both the measurements has shown a reasonably good agreement with each other. Therefore, it is inferred that the applied co-gettering experiment has a synergetic effect to improve the lifetime of the mc-Si substrate.
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*Keywords:* Multicrystalline silicon; Lifetime; Porous silicon; Gettering process

## 1. Introduction

The basic advantage of low-resistivity multicrystalline silicon (mc-Si) substrate in comparison with the single-crystalline silicon is its cheaper cost. This material has a localized region of high dislocation density and large impurity precipitate concentration, which in turn acts as carrier recombination sites. The presence of defects and impurities in the mc-Si substrate leads to the formation of energy levels in the forbidden zone, which essentially have some influence on the electrical (including the recombination) parameters of the material. This in turn results in a reduced minority carrier diffusion length ($L_n$) in the bulk region of the substrates [1–3]. Therefore, the processing step like gettering is the most suitable, which either removes or blocks the impurities and defects away from the device-active regions that have to be incorporated in the device-processing step to improve the electronic quality of the mc-Si substrate [4,5]. The gettering mechanisms such as intrinsic gettering (IG) process induced by oxygen precipitation have been applied as an integral part in the fabrication of integrated circuits [6]. The extrinsic gettering (EG) mechanisms such as phosphorous diffusion gettering (PDG) [7], aluminum alloy gettering (AAG) [4,7] or a combination of phosphorous and aluminum gettering have shown beneficial effects to improve or restore the bulk quality of silicon substrate [7–9]. Due to the slow dissolution of precipitate in the dislocation regions, these regions cannot be improved by the conventional PDG or AAG process step [3,8,9].

It was shown that porous silicon is an interesting material that has found application in various fields of microelectronics because of its unusual electrical and optical properties [10]. These nanostructured layers are usually prepared by the anodization of the silicon wafer in

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doi:10.1016/j.stam.2007.02.002

an aqueous HF solution, which leads to the formation of a porous silicon layer containing a large number of small pores [11,12]. The pore diameter typically varies between 40 and 200 Å. It shows that a significant amount of increase in the surface area-to-volume ratio ($\approx 200\,cm^2/m^3$) is achieved due to the presence of microstructure of the porous silicon network [13]. It is found that this material may be an attractive option for the silicon surface micromachining processing that is chemically stable in the HF-based electrolyte but is tolerant to the high-temperature processing step [14]. It also finds application in the area of opto-electronic devices [15], photovoltaic cells [16] and even as a sacrificial layer formation of the silicon-on-insulator (SOI) structure in the manufacturing of the integrated circuits [17].

In the present work, we describe the feasibility of the process implementation of a novel porous silicon and aluminum co-gettering experiment, which is applied as an alternative method to improve the minority carrier lifetime ($\tau_n$) or diffusion length of the low-resistivity mc-Si substrates. It is shown that high-temperature annealing of the chemically etched porous silicon surface in a high-flux solar furnace has enhanced the impurity diffusion into the porous silicon network, thereby acting as an efficient external gettering site [18–20]. This very reactive porous material can be oxidized far more rapidly ($\approx$10–20 times) than the oxidation process of a single-crystalline silicon surface [15,21]. The porous silicon gettering consists of oxidizing the porous silicon layers in wet oxygen ambient condition followed by the removal of the oxide in a dilute HF solution. Because of the lattice mismatch with the silicon surface, it can act as an external gettering center for the impurities that otherwise remain in the wafer and form a nucleation site for the oxidation-induced stacking faults (OISF). The impurities and defects can be accommodated inside the cavities of the porous silicon network. This condition is referred to as 'pre-oxidation gettering stage' [19,21]. There are several methods available to measure the diffusion length of minority carriers in the bulk of the semiconductor substrate. These methods are based on the measurement of some device properties such as the current or the voltage in which the measured parameter is a function of the diffusion length. In study, two independent methods such as the photoconductive decay measurements and photocurrent generation method have been applied to estimate the gettering-induced improvement in the diffusion length of the minority carriers in the low-resistivity mc-Si substrates.

## 2. Experimental

The starting material was a $\langle 100 \rangle$-oriented, 1 Ω-cm resistivity, boron-doped multicrystalline silicon substrate. These wafers were then chemically polished using a cold solution of $HF{:}HNO_3{:}CH_3COOH$ in a 4:1:1 by volume ratio. This had approximately removed 10–15 μm of silicon from both sides. The experiments were divided into (a) porous silicon/aluminum alloy co-gettering (porous silicon/Al co-gettering) and (b) simultaneous phosphorous/aluminum alloy gettering (P/Al gettering), respectively. These processes are intended to improve the electronic quality of the mc-Si wafer and guarding them against any more contamination during further thermal processing. In the first case, porous silicon/aluminum co-gettering experiments were performed at 850–950 °C. Here, porous silicon layers of approximately 150–200 nm thickness was electrochemically grown in a specially designed anodization cell in which silicon substrate was used as the positive electrode and platinum wire mesh acted as the cathode. The electrolyte consists of 48% aqueous HF solution mixed with ethanol and water (in 1:1:5 by volume ratio of $HF{:}CH_3–CH_2–OH{:}H_2O$) and the current density was 50–100 $mA/cm^2$ for an etching time of 5 min [22]. Then, wafers were rinsed in 18 MΩ de-ionized water and dried. Thereafter, a thick film of high-quality aluminum layer of 2 μm was deposited by the vacuum evaporation technique on the other side of the silicon wafer. Immediately, wafers were vertically stacked in the diffusion boat with Al-deposited sides facing each other and inserted into an open-tube furnace. Prior to the starting of the pre-oxidation step at 950 °C, the silicon wafers were annealed at 850 °C in the nitrogen gas ambient for 30 min. Then, ambient gas changed to nitrogen/oxygen ($N_2/O_2$) gas and the temperature slowly raised to 950 °C at a ramping rate of 4 °C/min till the furnace reached a steady temperature at 950 °C. The wet oxidation of the porous silicon was performed at 950 °C for 60 min duration in wet oxygen ambient in which the oxygen is bubbled through water heated at 95–100 °C. This helps to carry the steam from the bubbler into the furnace maintained at 950 °C. After the oxidation step, the furnace is cooled down to about 450 °C with a cooling rate of 4 °C/min and thereafter wafers were pulled out. The remaining Al–Si eutectic formed during the annealing stage is removed by applying an ultrasonic treatment in dilute HCl followed by a rinse in de-ionized water. The oxide formed during the wet oxidation can be removed by a short dip in dilute HF solution followed by a thorough rinse in de-ionized water. In the second case, simultaneous phosphorous diffusion and aluminum gettering experiments were carried out at 850–950 °C for 30–60 min with approximately 2 μm thick high-quality aluminum layer vacuum evaporated on the rear surface of the silicon substrate. The presence of aluminum layer on the rear surface of the wafer will act as a mask that avoids the diffusion of phosphorous on the rear side and forms an effective gettering site for impurities and defects at temperatures above 800 °C. Similarly, reference test samples without any porous silicon/aluminum treatments or phosphorous and aluminum alloy treatments, but with a phosphorous diffusion process performed at 850 °C for 20 min, were carried out. The gettering-induced improvement in the processed wafers was monitored by photoconductivity decay (PCD) measurements [23] and the photocurrent generation method (PCM), respectively. We

first measured the lifetime of the test samples after cleaning them with a dilute solution of HF followed by immersion in a passivating solution of iodine/methanol [24], because for a systematic lifetime measurement, it is important to have a reliable surface passivation that does not affect the properties of the bulk lifetime. The front surface of the porous silicon/aluminum co-gettered and phosphorous–aluminum co-diffusion gettered samples was chemically polished in acid solution and the p–p$^+$ junction at the rear contact was retained. The test sample is illuminated with a pulse of light from a stroboscope, which will generate carriers in the silicon sample. After several transient times of illumination were elapsed, the excess carrier concentration ($n'$) has a nearly uniform distribution throughout the wafer. The apparatus monitors decay of the excess bulk minority carrier density ($n'$) induced when the strobe light is immediately switched off [23]

$$\frac{dn'}{dt} = -\frac{n'}{\tau_b} - \frac{2J}{qW}. \quad (1)$$

Here, $\tau_{bulk}$ is the bulk recombination lifetime, the factor 2 accounts for the recombination current $J$ from both the front and back surfaces and $W$ is the sample thickness. The change in carrier conductivity is measured in terms of the effective lifetime ($\tau_{eff}$), which is directly proportional to the bulk carrier concentration ($n_b$). The interfacial recombination velocity ($S$) may be defined as

$$J = qSn' \quad (2)$$

in such case, Eq. (1) becomes [22]

$$-\frac{1}{n'}\frac{dn'}{dt} = \left(\frac{1}{\tau_{bulk}} + \frac{2S}{W}\right), \quad (3)$$

where $W$ is the sample thickness. In the low injection level, if $S \ll D_n/W$, value of the diffusion coefficient ($D_n$) of the minority carriers in the p-type mc-Si is $D_n = 28\,cm^2/s$ [24]. Therefore, by rearranging the above Eqs. (1)–(3), effective lifetime ($\tau_{eff}$) is expressed in terms of the bulk lifetime ($\tau_{bulk}$) and surface recombination velocity ($S$)

$$\frac{1}{\tau_{eff}} = \left(\frac{1}{\tau_{bulk}} + \frac{2S}{W}\right). \quad (4)$$

When several samples with identical doping but with different thicknesses are measured, a plot of reciprocal lifetime ($1/\tau_{eff}$) versus $2/W$ can be generated, which gives a straight line. The bulk lifetime ($\tau_{bulk}$) at each injection levels is then obtained from the intercept of the straight line in the reciprocal lifetime ($1/\tau_{eff}$) axis and the slope of the graph gives the value of $S$ . Then, the electron diffusion length is calculated by using the expression $L = \sqrt{D_n\tau}$ [22]. Secondly, we applied the photocurrent generation method [26,27] to measure the minority carrier properties. It is based on creating an accumulation (induced p$^+$) layer on one side, and an inversion (induced n$^+$) layer on the other side of the wafer by depositing thin and semi-transparent layers of high- and low-work function metals such as Pd or Al, respectively. The desired n$^+$–p–p$^+$ structure was realized on the substrate by growing a good-quality thin thermal oxide on the front surface at 500 °C for 15 min and then deposition of a vacuum-evaporated thin Al layer took place. This Al layer is thin and semi-transparent enough to transmit light. The thermally grown $SiO_2$ layer under the top metal layer on the silicon surface provides a metal-oxide-semiconductor (MOS) structure for carrier generation. It forms an inversion layer (n$^+$) on the front surface of the sample due to the diffusion of the holes and electrons to the surface barrier and charge separation in the space charge region [25]. The structure is able to generate a photocurrent when illuminated with monochromatic radiation in the near-bandgap region, i.e., $\lambda > 850$ nm [26,27]. The incident photon flux ($N_{ph}$) and intensity of the incident radiation ($P_{in}$) are related [25]

$$N_{ph} = P_{in}\frac{\lambda}{hc}, \quad (5)$$

where $h$ ( $= 6.64 \times 10^{-34}$ J/s) is the Planck's constant, $c$ is the velocity of the light and $\lambda$ is the wavelength of the incident light. Following the arguments in Refs. [26,27], we find that $w \gg d_p$ where $d_p$ is the accumulation layer (p$^+$) thickness and $L_n \gg \alpha_\lambda{}^{-1} \gg d_p$. Then, the photo-generated current density ($J_{sc}$) is related with the intensity of incident light radiation of wavelength $\lambda$ (i.e., $\lambda > 850$ nm) [26],

$$J_{sc} = \frac{q\lambda[1 - R_\lambda]L_n\alpha_\lambda^{-1}}{hc[L_n^2 - (\alpha_\lambda^{-1})^2]\cos h(w/L_n)}P_{in}, \quad (6)$$

where $q$ is the electronic charge, $R_\lambda$ is the reflectivity at $\lambda$, $\alpha_\lambda$ is the absorption coefficient at $\lambda$ and $L_n$ is the bulk diffusion length of the minority carriers. The spectral response (SR) of the device is determined from the ratio of the measured short-circuit current density at each wavelength to the light power incident on the top surface of the device as

$$SR(\lambda) = \frac{J_{sc}}{P_{in}}. \quad (7)$$

The internal quantum efficiency ($Q_{in}$) of the device is expressed as [28]

$$Q_{in} = \frac{J_{sc}}{qN_{ph}}\frac{1}{1 - R_\lambda}, \quad (8)$$

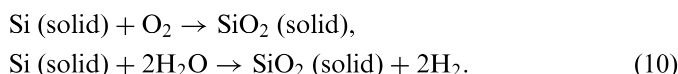
where $J_{sc}$ and $P_{in}$ are the current density and power intensity corresponding to the radiation of photon energy $hv > E_g$. Using Eqs. (6–8), $Q_{in}$ can be expressed in terms of SR($\lambda$) as

$$Q_{in} = \left[\frac{hc}{q\lambda}\frac{1}{1 - R_\lambda}\right]SR(\lambda). \quad (9)$$

## 3. Results and discussion

The porous silicon layers grown on the silicon surface by a simple and reproducible method exhibits good surface texture with uniform thickness and low porosity [10]. The

surface morphology of the porous silicon layers measured by AFM is shown in Fig. 1. It shows that the resulting etched surface of the porous silicon consists of irregular and randomly distributed nanocrystalline upright structures. The refractive index of the porous silicon layer was measured to be about 1.9, which agrees with the value previously reported for porous silicon layers [10,16]. It shows that this material can be oxidized much rapidly than the single-crystalline silicon because the lattice constant of the porous silicon network is slightly higher than the crystalline silicon [17]. Moreover, the porous silicon oxidation rate is large enough ($\approx$10–20 times) due to the high reactivity of the mesoporous structure of the porous silicon network, which helps to oxidize this material without wafer warpage [21,22,29]. Heat treatment of the porous silicon is carried out at 950 °C in a wet oxidizing atmosphere in which oxygen is passed through the water heated at 90–100 °C [17]. The chemical reaction describing the wet thermal oxidation of the silicon surface is given by [30]



$$\text{Si (solid)} + O_2 \rightarrow SiO_2 \text{ (solid)},$$
$$\text{Si (solid)} + 2H_2O \rightarrow SiO_2 \text{ (solid)} + 2H_2. \quad (10)$$

The oxidation proceeds by the diffusion of the oxidizing species through the oxide to the $Si/SiO_2$ interface where the oxidation process occurs [30]. Therefore, diffusion is most rapid in wet oxidation. Thermally grown $SiO_2$ layer is usually amorphous in nature and has a density of $\sim$2.2 gm/cm$^3$. The oxidation occurs throughout the porous silicon volume and this in term corresponds to the growth of several nanometers of regular silicon dioxide. The thickness and refractive index of the wet oxidized silicon surface were $<$1000 nm and 1.45, respectively. The linear activation energy depends on the reaction rate at the $SiO_2$/Si interface. The diffusion-limited parabolic and linear activation energy corresponding to the wet oxidation was calculated and is found to be 0.71 and 1.96 eV, respectively.

Fig. 2 shows the $Q_{in}$ response to the test samples in the long wavelength range 850 nm $< \lambda <$ 1050 nm range. It is noticed that $Q_{in}$ response of the porous silicon/aluminum co-gettered sample (-■-) is significantly higher than the corresponding value measured for the phosphorous and aluminum co-gettered sample (-●-) or the ungettered reference sample (-▲-). It may be resulted from the enhanced current collection in the long wavelength region for the gettered samples. From the figure, it is observed that there is a gradual decrease of the measured photocurrent in the long wavelength range ($\lambda >$ 850 nm) for all

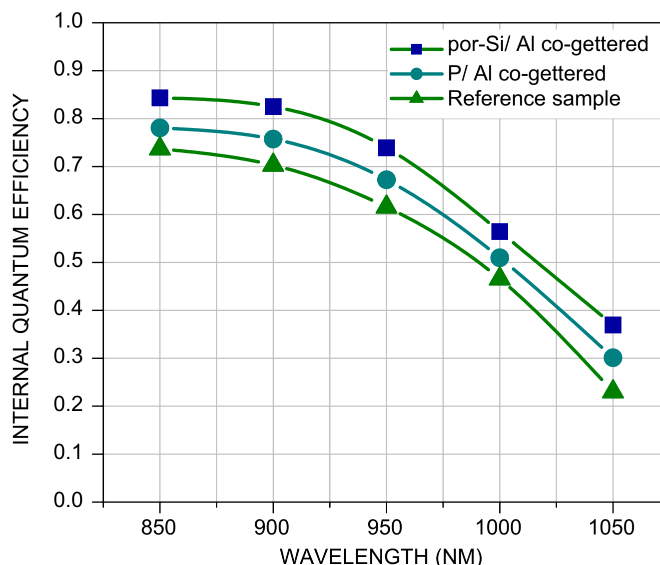



Fig. 2. Internal quantum efficiency plot for the porous silicon/aluminum co-gettered, phosphorous/aluminum alloy gettered and reference multi-crystalline silicon samples in the wavelength range 850–1050 nm.

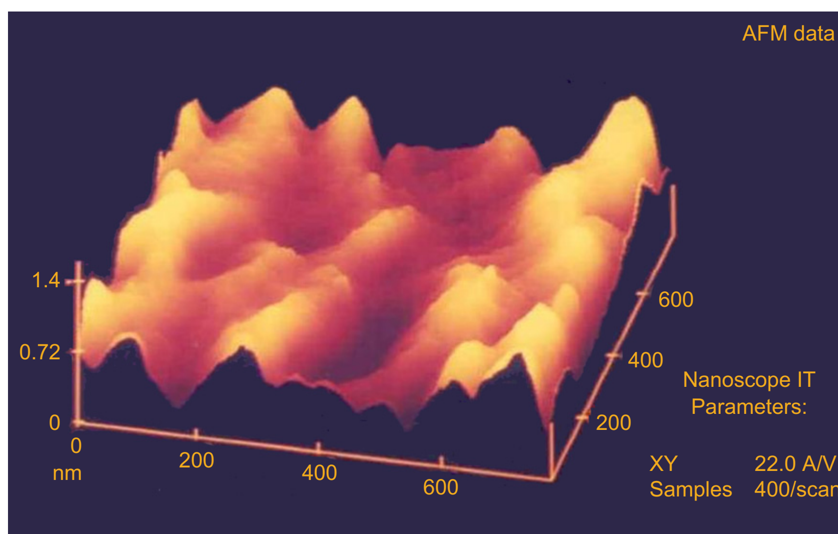



Fig. 1. Surface morphology measurement of the porous silicon surface by AFM shows the irregular and randomly distributed microcavities on the etched silicon surface.

the three types of test devices. It may be understood from the fact that absorption coefficient is lower at longer wavelengths; thereby resulting in a reduction in current collection efficiency in the long wavelength range. This trend in carrier photocurrent with the absorption coefficient ($\alpha_\lambda^{-1}$) due to the weaker absorption can be used to estimate the diffusion length in the near-bandgap radiation (850 nm $<\lambda<$ 1050 nm) by following the relationship between the $Q_{in}^{-1}$ and $\alpha_\lambda^{-1}$ accordingly [22,31]

$$\frac{Q_{in}^{1}}{f_0}-\frac{\alpha_\lambda^{1}}{L_n}=1, \quad (11)$$

where $L_n$ is the bulk diffusion length and $\alpha_\lambda$ is the absorption coefficient of the silicon corresponding to the wavelength $\lambda$ and $f_0$ corresponds to the correction factor for non-uniform illumination of light [22,31]. The conventional interpretation of the $Q_{in}$ data is obtained from a plot of $Q_{in}^{-1}$ versus $\propto_\lambda^{-1}$, where the absorption coefficient $\propto_\lambda^{-1}$ is a known function of the wavelength [27]. Eq. (11) represents a linear relation between the $Q_{in}^{-1}$ and $\propto_\lambda^{-1}$ for small absorption length $\propto_\lambda^{-1}$ with a slope solely determined by the diffusion length for $\propto_\lambda^{-1}\ll W$. The intercept of the straight line on the absorption length axis gives the value of the minority carrier diffusion length ($L_n$). Fig. 3 describes the extrapolation of the value of diffusion length for the three types of test samples by a least-square fit of $Q_{in}^{-1}$ versus $\alpha_\lambda^{-1}$ plot in the 850 nm $<\lambda<$ 1050 nm wavelength range. The value of the minority carrier diffusion length extracted for all the three samples in the near-bandgap wavelength region and the PCD measurements are given in Fig. 4. It shows that the results of the diffusion length calculated from the long wavelength limit were agreeing reasonably well with the corresponding lifetime data obtained from the PCD measurements. This enhancement in the minority carrier diffusion length is brought out by the improvement of the electronic quality of the bulk substrate due to the porous silicon/aluminum co-gettering effect. During the heat treatment, it shows that the porous silicon layer grown on one side and Al layers deposited on the other surface undergo an oxidation or/annealing step under the $N_2/O_2$-controlled atmosphere, which allows the impurities to diffuse throughout the porous silicon layer and the aluminum layer, respectively. This may help to getter impurities towards the porous silicon layer on one side and the aluminum/silicon melt on the other side. The porous silicon has a hydrogen-rich surface, which makes the possibility of a bulk passivation effect during the high-temperature oxidation step and may also help to suppress the electrically active defects in the bulk region of the mc-Si substrate [18,19]. The grain boundary and dislocation passivation by Al indiffusion or indiffusion of atomic hydrogen generated at the Al–Si may also contribute to enhance SR in the longer wavelength range and hence to an apparent improvement of the minority carrier diffusion length in the porous silicon/aluminum co-gettered samples [3,8,18,20].

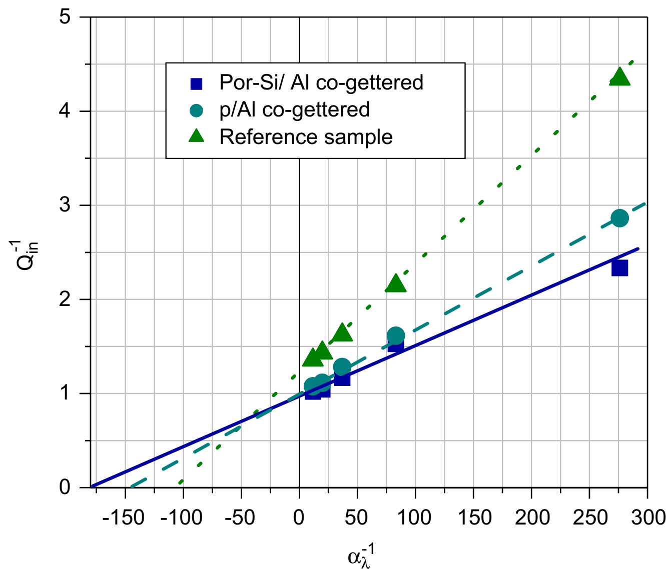



Fig. 3. The minority carrier diffusion length deduced from the plot of inverse internal quantum efficiency versus absorption coefficient in the wavelength 850–1050 nm.

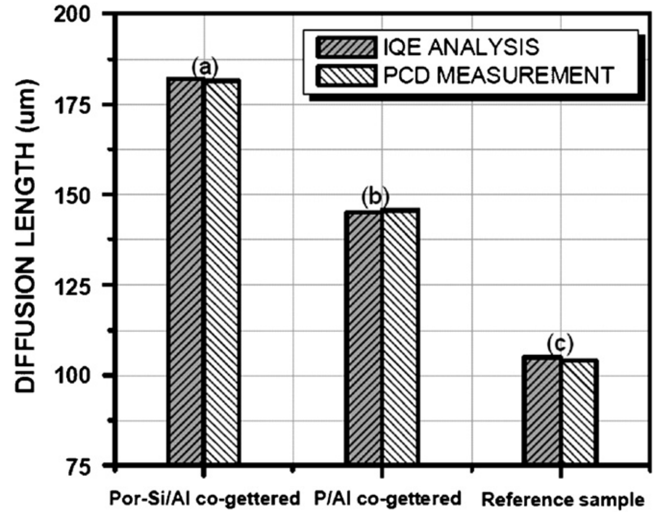



Fig. 4. The minority carrier diffusion length measured in the test samples by the analysis of the internal quantum efficiency measurement and photoconductive measurements for the three different processing schemes considered in the studies: (a) porous silicon/aluminum co-gettered, (b) phosphorous/aluminum alloy gettered and (c) reference mc-Si sample, respectively.

## 4. Conclusion

It is shown that the process of implementation of the porous silicon and aluminum co-gettering experiment has a positive trend of improvement in the electronic quality of the mc-Si substrates. These processes are intended to improving the electronic quality of the mc-Si wafer and guarding them against any more contamination during further thermal processing. We have applied both photoconductive decay and a photocurrent generation method to

estimate the gettering-induced improvement in the lifetime /or diffusion length of the minority carriers in the gettered mc-Si substrates. The results of both these measurements are in good agreement with each other.

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