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Quantum dots in Si/SiGe 2DEGs with Schottky top-gated leads

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Abstract. We report on the fabrication and characterization of quantum-dot devices in a Schottky-gated silicon/silicon–germanium modulation-doped two-dimensional electron gas (2DEG). The dots are confined laterally inside an etch-defined channel, while their potential is modulated by an etch-defined 2DEG gate in the plane of the dot. For the first time in this material, Schottky top gates are used to define and tune the tunnel barriers of the dot. The leakage current from the gates is reduced by minimizing their active area. Further suppression of the leakage is achieved by increasing the etch depth of the channel. The top gates are used to put the dot into the Coulomb-blockade regime, and conductance oscillations are observed as the voltage on the side gate is varied.

A new generation of high quality, high mobility silicon/silicon–germanium quantum-well devices has recently emerged to meet the needs of nascent technologies like quantum computing and spintronics. In the near future, it is possible that silicon will form the basis for many of the same nano-scale devices previously constructed from III–V materials. Indeed, silicon has some advantages over other materials in the context of quantum information processing due to long spin lifetimes associated with zero nuclear spin ²⁸Si, the most prevalent isotope, and low spin–orbit coupling [1]–[6]. Silicon quantum wells also display interesting physics associated with valley splitting [7]–[11]. Quantum dot quantum computing architectures have been

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proposed, requiring not only the unprecedented control of individual few-electron quantum dots, but also the fine-tuning of couplings to neighbouring dots [12]–[16].

To meet these needs, an expanding fabrication toolbox has been developed for silicon/silicon–germanium quantum well devices. Etch-defined quantum dots have been fabricated in Si/SiGe quantum wells [17]–[19] and bulk SiGe [20, 21] using lateral side gates in the plane of the dot [18, 20, 21] or a single metal-on-oxide gate over the entirety of the dot [17, 19]. These gates can successfully modulate the potential of the dot. However, the etching procedure induces a depletion zone around the etch boundary which limits the control of the tunnel barriers [22] due to the weak capacitive coupling of the gates. Metal side gates can be used to reduce the distance between the dot and the gates [23], thereby improving the coupling. Nevertheless, the shape of the dot and the tunnel barriers in the leads are ultimately bounded by the dimensions defined by the etch. Since exquisite control of the tunnel barriers between dots and leads (or additional dots) is a prerequisite for quantum computing, the ability to manipulate the dot shape and dot-lead tunnel couplings with top gates will be advantageous.

In gallium arsenide quantum dots, a level of control consistent with quantum computing has been achieved using Schottky top gates [24]. In this technique, metal gates are patterned directly above the quantum-well heterostructure, providing a strong and proximal capacitive coupling. Current flow between the top gates and the underlying two-dimensional electron gas (2DEG) is prevented by the Schottky barrier, which depletes carriers in the vicinity of the electrodes. Similar schemes have been explored in the context of silicon heterostructures, culminating in the demonstration of quantum point contacts [25]–[28]. However, silicon Schottky barriers have proven leaky [29], with current paths possibly following lattice dislocations, arising from state-of-the-art strain relaxation techniques in Si/SiGe heterostructures. The leakage problem, which forms the greatest obstacle for silicon quantum devices, is still poorly understood. In short, Schottky top-gated quantum dots have not been attained in modulation-doped silicon/silicon–germanium 2DEGs. Their demonstration forms an important milestone.

Here, we demonstrate two hybrid quantum dot devices that employ both etching and top-gate fabrication techniques. In particular, we show that tunnel junctions can be formed and tuned using Schottky top gates. An additional degree of control is provided by a back gate, which enables the density of the 2DEG to be varied. Leakage is minimized in this geometry due to the small size of the top gates, whose active area is less than $0.2 \mu\text{m}^2$. Additional suppression of leakage is observed in devices with deeper channel etches. We hypothesize that ultra small gates reduce the overlap of electrodes with localized leakage paths.

The devices are patterned in a Si/SiGe heterostructure grown by ultrahigh vacuum chemical vapour deposition. The 2DEG sits at the top of a 80 \AA strained silicon layer capped with 140 \AA of $\text{Si}_{0.7}\text{Ge}_{0.3}$, 140 \AA of P-doped $\text{Si}_{0.7}\text{Ge}_{0.3}$ and 35 \AA of Si. The strained silicon is grown on a relaxed $\text{Si}_{0.7}\text{Ge}_{0.3}$ virtual substrate obtained by grading from 0 to 30% Ge over several microns [30]. Strained silicon is necessary to achieve the correct band offsets for quantum confinement relative to the surrounding (relaxed) SiGe [31]. The electron density of the 2DEG is $4 \times 10^{11} \text{ cm}^{-2}$ with a mobility of $40\,000 \text{ cm}^2 \text{ Vs}^{-1}$ as determined from magnetoresistance measurements of an etch-defined Hall bar at 2 K. Ohmic contacts are made to the 2DEG by Au/Sb evaporation and subsequent 400°C annealing. Gold is sputtered onto the entire back of the sample to form a back gate.

A $4 \mu\text{m}$ long, 800 nm wide channel is defined in the heterostructure by e-beam lithography and CF_4 reactive ion etch such that a two-terminal device is created (figure 1). The etch depths are 55 and 85 nm for Devices A and B respectively, as confirmed by atomic force microscopy.

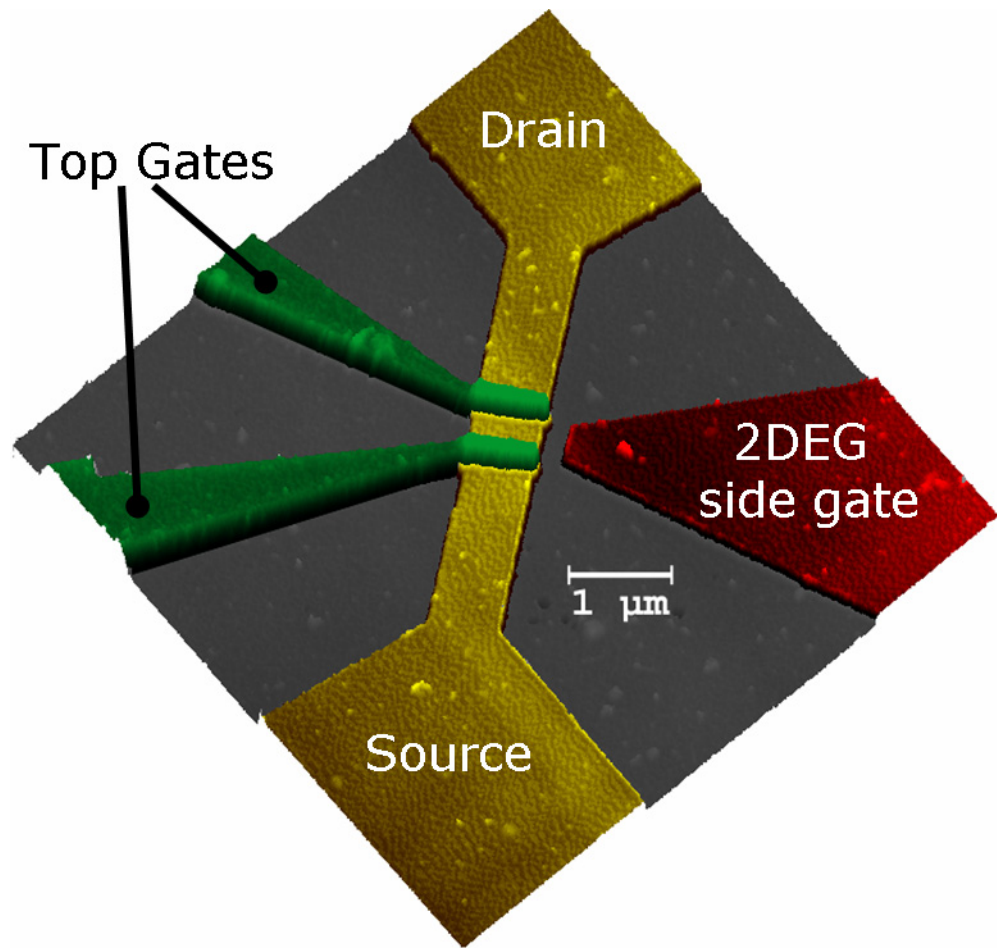


Figure 1. False colour atomic force micrograph of a quantum dot consisting of an 800 nm wide etched-defined 2DEG channel, a 2DEG side gate in the same plane as the channel, and 100 nm wide metal Schottky gates extending from the etched region up and across the channel. The separation between the metal top gates is about 400 nm. A negative voltage is applied to the top gates to locally deplete the 2DEG and form a quantum dot between the gates. The potential of the dot can be modulated by the side gate.

A single side gate about 300 nm from the channel is patterned into the heterostructure in the same lithographic and etching step. The 2DEG in this lateral gate is electrically isolated from the 2DEG in the channel, and its capacitive coupling can be used to modulate the potential of the electrons in the quantum dot.

Metal top gates are formed by a second e-beam lithography step followed by evaporation of 80 nm of Pd and lift-off. The gates are patterned with an active top-gate area of 100 nm \times 800 nm and are carefully aligned to within 20 nm such that the gate just extends across the top of the channel. Contact pads and wires are also formed in this step in the etched regions and extend up the side of the channel to the gates. All measurements of conductance through the device are low-frequency lock-in measurements.

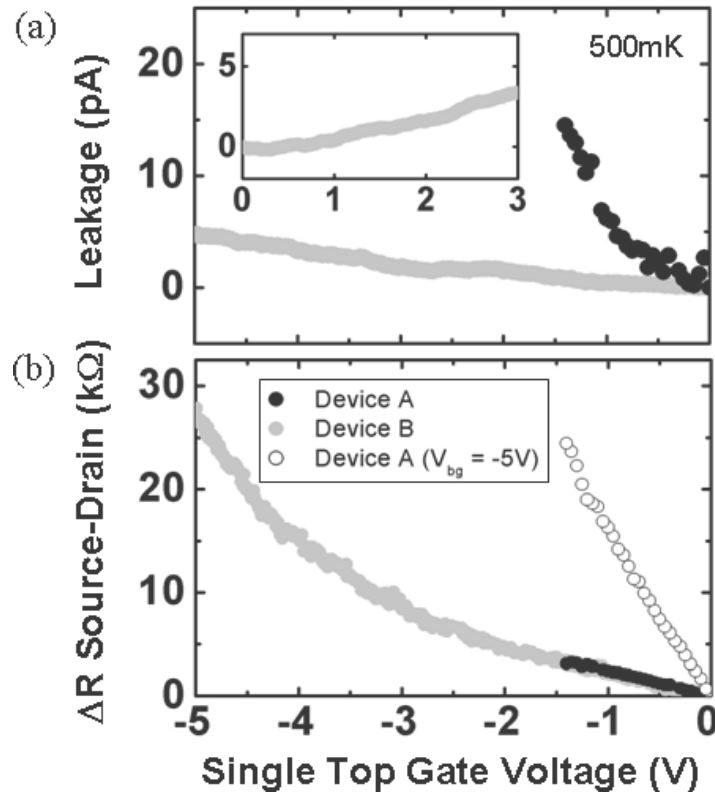


Figure 2. (a) As the voltage is decreased on a single top gate, the leakage current is minimal out to -1.4 V for Device A and -5 V for the deeper etched Device B. Inset: the leakage is suppressed in Device B even for positive voltages up to 3 V (units on axes same as the main figure). (b) The change in resistance through the channel from $V_{tg} = 0$ V within this low-leakage working range. For Device A, an increase in resistance greater than the h/e^2 necessary for quantum confinement is achieved only after a backgate is used to lower the carrier concentration in the channel.

The Schottky gates are characterized by measuring the change in resistance through the channel of each device (figure 2(b)) along with the leakage current from the gate as the voltage (V_{tg}) on a single top gate is varied (figure 2(a)). The leakage current of Device A is small (< 15 pA) down to an applied voltage of -1.4 V. In this working range, the resistance through the channel increases by 6 k Ω from the two-point resistance measured across the whole device of 36 k Ω at $V_{tg} = 0$ V. However, the resistance through each lead should be greater than $h/e^2 = 26$ k Ω when used to define the quantum dot.

Device B exhibits a much greater working range, with minimal leakage current (< 10 pA) out to -5 V—more than three times greater than Device A—such that a tunnelling resistance increase of 28 k Ω is achieved between the two sides of the channel. (The two-point resistance is 73 k Ω with the top gates grounded.) The only difference in the fabrication of the two devices is the deeper etch depth for Device B. Previous work suggests that side-wall depletion increases with etch depth in similarly etched Si/SiGe 2DEG wires [32]—a trend we have observed as well. This wider depletion zone associated with the deeper etch may provide better insulation of

the metal electrodes from the active 2DEG of the channel. The large available working range is further demonstrated by forward biasing the top gate of this device; the leakage is suppressed up to +3 V as shown in the inset of figure 2(a).

In the case when the leakage current is still a limiting factor (as in Device A), the back gate can be employed to tune the carrier density in the device such that the necessary resistance through the leads is achieved within the working range of the top gates. The carrier density decreases with a negative voltage applied to the back gate (V_{bg}) and the resistance of the whole device—including the leads—is increased. Since we do not know the lead resistance separate from the rest of the device, we again measure the increase in resistance induced by a top gate. Because the resistance is inversely proportional to the density, the resistance increases more rapidly given a lower carrier density in the channel as the voltage on the top gate is varied. With -5 V applied to the back gate to partially deplete the carriers, the resistance across the whole of Device A is increased to 43 k Ω . The third data set in figure 2(b) shows that an increase in resistance of 25 k Ω is then observed as the top-gate voltage is varied from 0 to -1.4 V, further depleting the carriers local to the top gate. Voltages on the back gate down to -7 V are applied to achieve changes in resistance due to the top gate as high as 80 k Ω .

The confining characteristics of the top gates are further demonstrated by putting both leads of a device into the tunnelling regime. A quantum dot is formed in the undepleted region between the gates, with side-wall confinement provided by the surface depletion from the etching. For Device B with each of the top gates at -5 V, conductance through the channel is blockaded for source–drain biases (V_{ds}) in the range -1 mV $< V_{ds} < 0.6$ mV as shown in figure 3(a). Assuming a disc geometry, this gives a dot diameter of 470 nm with about 700 electrons in the dot with the back gate grounded.

The etch-defined lateral gate can be used to modulate the potential in the dot. If the voltage on the side gate (V_{sg}) is varied when the top gates are grounded, the carrier density in the channel is altered, corresponding to a monotonic change in the conductance with no oscillations. In contrast, when the negative voltages necessary for blockade are applied to the top gates as before, conductance oscillations are observed as the voltage on the side gate is increased, with the number of electrons in the dot increasing by one with each oscillation (figure 3(b)). The large separation between the dot and the side gate produces a non-proximal capacitive coupling, which also affects the tunnel barriers. For $V_{sg} > 0.3$ V, the side-gate voltage decreases the resistance in the leads such that finite background conductance is observed. Conductance oscillations continue to be observed, however, indicating that electrons are still bound in the dot between the leads. The conductance between the leads no longer goes to zero even with the background removed, suggesting that the tunnel coupling of the dot to the source and drain leads has increased [33]. The peak spacing with V_{sg} is about 280 mV, giving a capacitive coupling of 0.57 aF. As expected, this is similar to the coupling observed for lateral 2DEG gates used to modulate purely etch-defined dots [18]. As shown for Device A in figure 3(c), these oscillations are observable up to about 10 K or 830 μ eV, consistent with the charging energy calculated from the Coulomb blockade. A random peak shift is also observed as the temperature is increased, most likely due to background charge fluctuations which occur as discreet switching events.

In conclusion, we have shown that low-leakage Schottky top gates can be implemented in Si/SiGe heterostructures over a large working range in voltage, producing tunnel barriers and quantum dots in the underlying 2DEG. In one device, an additional back gate was needed to achieve tunnelling behaviour within the working range of the top gates. We anticipate that such back gates will become common features of silicon quantum devices, in analogy with III–V

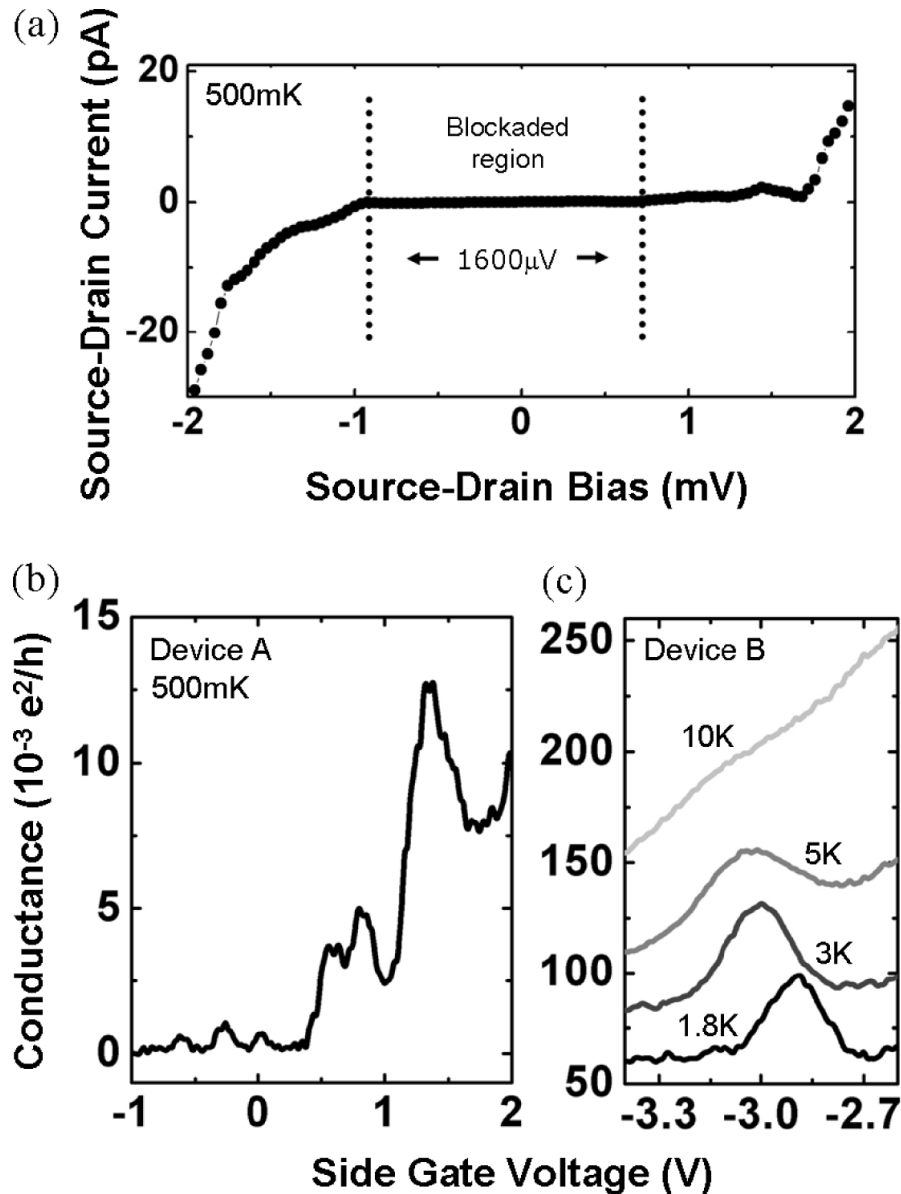


Figure 3. (a) Current through the dot as the drain–source bias across the dot is varied. The width of the zero-conductance plateau about $V_{ds} = 0$ corresponds to a charging energy of $800 \mu\text{V}$. (b) Conductance measurement through the dot as the voltage on the lateral 2DEG gate is varied. Oscillations are observed indicating that the charge on the dot has changed by one electron between minima. Two regimes of the dot are shown: (i) at $V_{sg} < 0.3 \text{ V}$, the electrons in the dot are well isolated from the leads such that the conductance goes to zero between peaks. (ii) For $V_{sg} > 0.3 \text{ V}$, the side gate has opened up the leads such that the dot is better coupled to the leads; the peaks are broadened and the conduction does not go to zero between peaks even when the background is removed. (c) A single conductance peak as the temperature is varied. The peak is indistinguishable from the background at 10 K, in good agreement with the measured charging energy of the dot.

devices. In a second device with deeper etching, a much larger working range was observed, increasing the resistance into the tunnelling regime even without a back gate. In future work, we believe that optimization of etch depths together with side-wall passivation or gate oxides could achieve better isolation results than either process alone. Quantum dots were achieved in both our devices, with tunable Schottky barriers. In addition to Schottky gates, the dots also utilize 2DEG side gates, demonstrating the compatibility of the two techniques. For proximal control of individual dots, we expect that Schottky plunger gates will replace side gates, allowing for much smaller dots as well as multiple coupled dots.

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