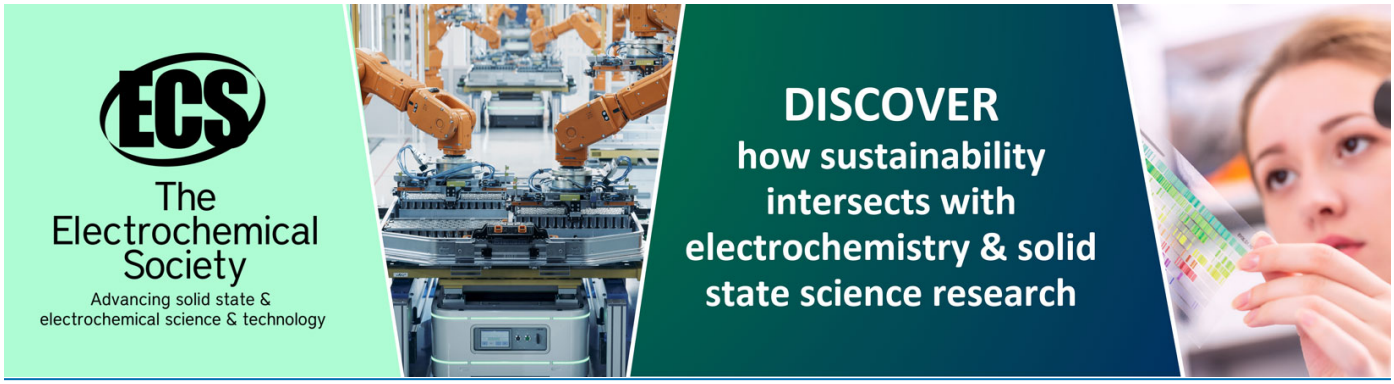
On-chip thermal management of hotspots using a perspiration nanopatch



J. Micromech. Microeng. **20** (2010) 075010 (10pp) doi:10.1088/0960-1317/20/7/075010

On-chip thermal management of hotspots using a perspiration nanopatch

Shankar Narayanan, Andrei G Fedorov[1] and Yogendra K Joshi

George W Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0405, USA

E-mail: andrei.fedorov@me.gatech.edu

Received 18 January 2010, in final form 22 April 2010
Published 21 May 2010
Online at stacks.iop.org/JMM/20/075010

Abstract

A cooling mechanism based on evaporation from thin liquid films is utilized for thermal management of hotspots combining efficient heat and mass transfer techniques. Dissipation of large heat fluxes from small form-factor areas is made possible by minimizing the thermal resistance across the evaporating liquid film. This is achieved by maintaining a very thin film ($\sim$15 μm) of coolant by capillary confinement using a nano-porous membrane ($\sim$10 μm). At the same time, evaporation is promoted by using jet impingement of dry air on the membrane. Based on these underlying ideas, a MEMS device called a 'perspiration nanopatch' is presented. The design and fabrication process of this micro-fluidic device is described along with experimental performance characterization under different operating conditions. Dissipation of heat fluxes in excess of 600 W cm^{-2} is demonstrated with heat transfer coefficients approaching 0.1 MW m^{-2} K^{-1} for surface temperatures well below the saturation temperature of the working fluid.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

In order to sustain a remarkable reduction of electronic product cost per function ($\sim$30% every year), the semiconductor industry pursues enhancement in equipment productivity, manufacturing yield, and most importantly, functionality (i.e. the number of bits, logic gates, transistors, etc incorporated into a die). Consequently, an increase of merely 12% in chip area accommodates 40–60% more functionality per annum. At the same time, a continuous reduction of about 30% in feature sizes is observed every year [1]. While an overall increase in functionality has resulted in higher power dissipation, thermal management is further exacerbated by large leakage currents due to shrinking feature sizes. In addition, clustering of functional units on the microprocessor to enhance computational performance creates hotspots, requiring efficient heat dissipation from these confined areas. A failure to address hotspot thermal management can cause localized heating resulting in substantial temperature gradients detrimental to chip performance and reliability [2]. Hence, a comprehensive chip-level thermal management solution requires an effective cooling mechanism to dissipate large heat fluxes from hotspots that can be seamlessly integrated with a suitable background cooling system.

Unlike air cooling, traditionally used for thermal management of microprocessors, which has a fundamental limit on the maximum heat flux that can be dissipated, liquid coolants have the advantage of utilizing the latent heat of vaporization by undergoing a change in phase, in addition to very efficient convective cooling, resulting in much greater power dissipation while maintaining a lower and uniform surface temperature. For instance, at chip (junction) temperatures close to 85 °C, pool boiling of dielectric fluorocarbon FC72 can dissipate heat fluxes of the order of 50 W cm^{-2} while air-cooled heat sinks of an equivalent size can support only 0.1 W cm^{-2} [3]. Though phase change has an appealing potential for heat transfer enhancement, limitations do exist to implement it for applications with higher heat load. The highest heat flux achievable by boiling or evaporation depends on the thermo-physical properties of the coolant and hydrodynamics of two-phase flow. While boiling or phase change in the bulk of liquid in the direct vicinity of the heat source is a feasible option for hotspot thermal management,

[1] Author to whom any correspondence should be addressed.

Table 1. Literature summary of the maximum heat flux dissipated by different cooling mechanisms.

Cooling mechanism	Heat flux
Single-phase flow in microchannels (Pijnenberg *et al* [6])	450 W cm^{-2} (at $T = 85$ °C with DI water and silicon microchannels)
Single-phase flow in porous media (Hetsroni *et al* [7])	416 W cm^{-2} (at $T = 85$ °C with stainless-steel sintered particles)
Single-phase, multi-jet impingement cooling (Overholt *et al* [8])	471 W cm^{-2} (at $T = 85$ °C with DI water)
Two-phase flow in microchannels with sub-cooling (Faulkner *et al* [9])	275 W cm^{-2} (at $T = 125$ °C with water in horizontal, rectangular microchannels with an inlet temperature of 10 °C)
Two-phase flow in microchannels with sub-cooling (Kosar *et al* [10])	250 W cm^{-2} (at $T = 160$ °C with water in horizontal, rectangular microchannels with an inlet temperature of 20 °C)
Two-phase flow in porous media (Chen *et al* [11])	80 W cm^{-2} (water, copper sintered particles)

it requires the surface to exceed saturation temperature and is bounded by the critical heat flux (CHF). At atmospheric pressure, the CHF for saturated pool boiling is in the range of 15–25 W cm^{-2} for FC72 and 100–120 W cm^{-2} for water [4], which can be further enhanced by incorporating micro-textured surfaces (e.g., yielding 105 W cm^{-2} for pool boiling of saturated FC72 [3]). A comparison of different cooling mechanisms currently in development for high heat dissipation is summarized by Agostini *et al* [5]. This study also lists the maximum heat flux corresponding to a junction temperature of 85 °C using jet impingement, single and two-phase flow in microchannel and porous media. Table 1 is a brief comparison of the highest performing cooling methods on the basis of the heat flux dissipated for a particular junction temperature.

Evaporation or phase change at the free surface of any liquid film is limited by the thermal resistance across the film (affecting heat conduction/convection) and the mass transfer resistance at the free surface of the film (affecting the rate of evaporation). The thermal resistance of liquid film can be minimized if its thickness is reduced to a monolayer, while the rate of evaporation from the liquid–vapor interface can be maximized if a dry sweeping gas is utilized at the free surface of the evaporating layer. The concept of gas assisted thin-film evaporation was first demonstrated by Bar-Cohen *et al* [12] using high velocity flow of liquid–gas (FC72-Helium) mixture in a narrow gap between substrates. In their experiments, heat fluxes approaching 20 W cm^{-2} with volumetric heat dissipations close to 18 W cm^{-3} were demonstrated. Since the underlying idea relies on formation of a thin liquid film as a result of two-phase annular flow, the formation of dryout regions in the channels was a concern for sustained operation. Based on the understanding of rate-limiting factors, a micro-fluidic cooling device, termed 'perspiration nanopatch' [13], was proposed for dissipation of large heat fluxes from confined areas like on-chip hotspots. The design and operating principles of this device, along with theoretical analysis and macroscopic proof-of-principle experiments, were discussed in [14].

Building on the ideas outlined in the above-referenced work, this paper describes a process of fabricating a chip-mountable MEMS 'perspiration nanopatch' (figure 1) cooling device, with demonstrated capability for thermal management of hotspots. The heterogeneous fabrication process integrates the micro- and nano-scale components produced on different material substrates, which serve distinct functions, yielding a composite cooling device along with a microfabricated test structure in a single package. The experiments are carried out using prototype devices, and results demonstrate dissipation of very large heat fluxes while maintaining low surface temperatures.

2. Device fabrication

The cooling device and the test structure consist of three distinct layers (figure 1), which are fabricated in a cleanroom environment. An array of resistance micro-sensors and heaters are fabricated on a Pyrex substrate for temperature sensing and simulation of microprocessor hotspots. A second device layer facilitates fluid delivery to the hotspot with microchannels fabricated on a silicon substrate, including the inlet and outlet ports. This device layer also integrates a membrane made of porous anodic alumina (PAA), which confines a thin film of coolant within a cavity by capillary action and provides a passage only for vapor phase. A third device layer adhesively bonds the Pyrex and silicon substrates. This layer also provides the spacing between the silicon and Pyrex substrates, essentially defining the coolant film thickness between the membrane and the hotspot.

2.1. Fabrication of the sensors and hotspots on the Pyrex substrate

Fabrication of sensors on the Pyrex substrate is carried out by deposition of multiple layers of metal (using electron beam evaporation, E-beam) followed by the photo-resist lift-off process. The fabrication process starts with a polished 4 inch Pyrex wafer, which is first cleaned in Piranha. This is followed by spinning a negative photo-resist (NR9-8000, Futurrex) at 3000 RPM for 1 min resulting in a resist thickness of 8 μm. After pre-exposure bake in a convective oven at 150 °C, the resist is UV-exposed providing 168 mJ cm^{-2} dosage at a wavelength of 365 nm. It is then baked at 70 °C and developed using a resist developer (RD6, Futurrex) at room temperature for approximately 1 min. Thin layer deposition of titanium (500 °A) and platinum (3000 °A) is carried out using E-beam, where titanium serves as an adhesion layer. Using a resist remover (RR41, Futurrex) at 115 °C, the lift-off process is performed to result in a patterned composite metal layer on Pyrex. Given the use of a negative resist on a non-conductive substrate, resist baking in an oven instead of a hotplate

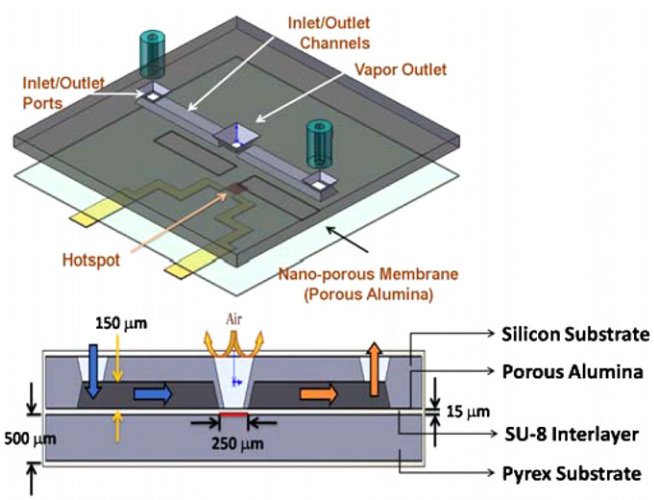


Figure 1. A schematic of the cooling device, test structure layers and assembly.

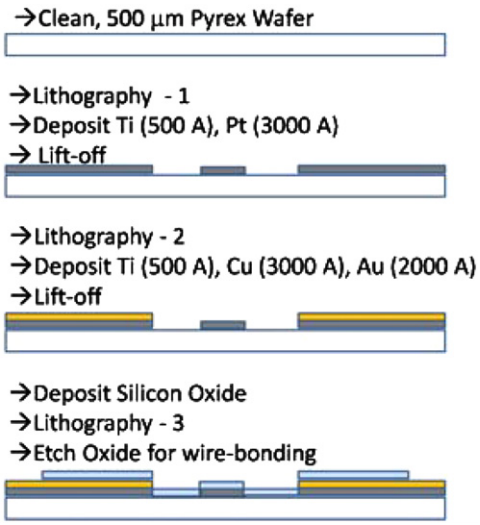


Figure 2. Fabrication process for hotspot and sensors on the Pyrex substrate.

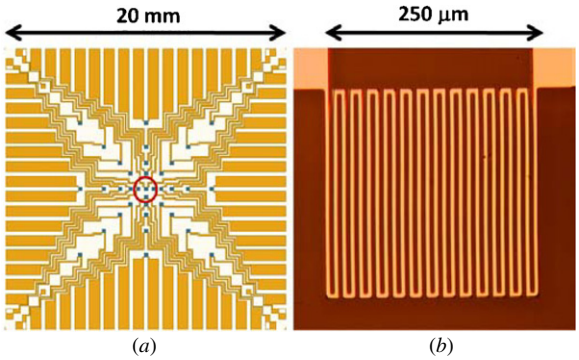


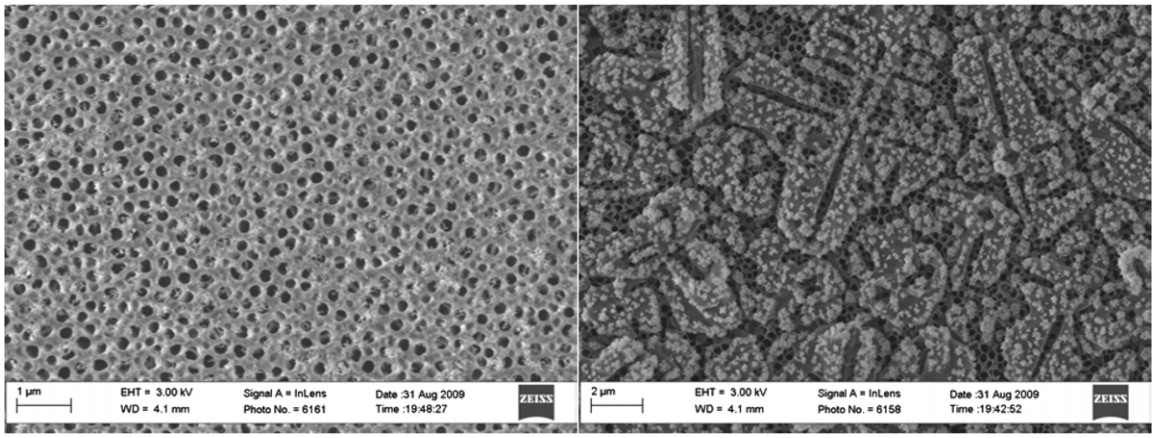
Figure 3. (*a*) Device layout on the sensor substrate, illustrating a centrally located square hotspot (250 μm) surrounded with 35 RTDs. (*b*) Magnified view illustrating the detailed design of a square 250 μm hotspot resistor.

yields more repeatable results. In order to avoid charring the underlying photo-resist, the metal deposition by E-beam is carried out at slower rates (1.5–2.5 °A s^{-1}) and in intervals, allowing the substrate to cool down. Subsequent lithography and metal deposition steps are performed following parameters mentioned above with the exception of the baking times. A smaller baking time in the oven is found to be more suitable due to the preexisting metal layer on the substrate. After successfully patterning the resist, E-beam deposition of titanium (500 °A), copper (3000 °A) and gold (2000 °A) is carried out followed by a lift-off process. A composite layer is formed by the metal lines connecting the sensor and hotspot to the device periphery. Use of a composite layer allows minimizing the electrical resistance of the metal lines, thus ensuring localized heating and temperature sensing. A thin layer of dielectric (silicon oxide) is thermally deposited using plasma enhanced chemical vapor deposition (PECVD) to avoid direct contact of the metal layer with the coolant during device testing. Square windows (600 μm × 600 μm) are etched peripherally in the deposited silicon oxide to expose the underneath metal for wire-bonding the device layer to a printed circuit board (PCB) for interfacing with data acquisition and experimental control hardware. The fabrication process of the sensors and hotspot on the Pyrex substrate is described pictorially in figure 2.

With overall dimensions of 20 mm × 20 mm, the sensor substrate consists of a central heater (a hotspot) surrounded with 35 temperature sensors, as shown in figure 3(*a*). The hotspots are fabricated as squares of different dimensions ranging from 250 to 750 μm sides, while all the surrounding sensors (thin-film platinum resistance thermal detectors or RTDs) are squares of 250 μm sides. The design layout shown in figure 3(*a*) illustrates a 250 μm hotspot surrounded by RTDs. The RTDs are densely spaced near the center (hotspot) to record the maximum change in temperature and are spread more sparsely toward the periphery where the thermal gradients are modest. Figure 3(*b*) shows a magnified view illustrating the detailed design of a square 250 μm hotspot resistor. The long and thin (10 μm) serpentine lines of hotspot and RTDs provide relatively high resistance (∼600 Ω), as compared to connecting metal lines (∼5 Ω), within a very confined space of the heating/sensing domain. The Pyrex substrate is used as a sensing/heating layer for the following reasons: (1) being transparent, it provides optical access to monitor the fluid channel where evaporation is taking place, and (2) its low thermal conductivity (∼1 W mK^{-1}) minimizes the heat spreading into the substrate, while the hotspot is activated.

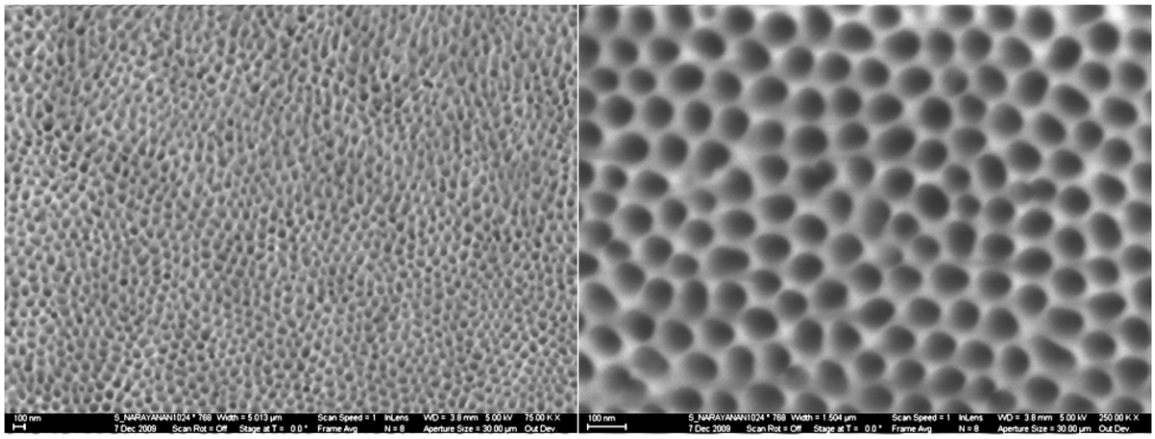
2.2. Fabrication of the nonporous alumina membrane on the silicon substrate

The membrane and fluidic channels are fabricated on a 4 inch, N-type, both sides polished, silicon substrate (of 100 crystallographic orientation). Silicon nitride (1 μm) is deposited on both sides of the wafer using the PECVD process. This is followed by lithography on both sides of the wafer. A positive tone photo-resist (SC1827, Shipley) is spun at 3000 RPM for 45 s resulting in a resist thickness close to 3 μm. It is then baked at 115 °C on a hotplate for



(*a*) (*b*)

Figure 4. SEM images comparing commercially obtained porous alumina, before (*a*) and after (*b*) immersion into the BOE solution.



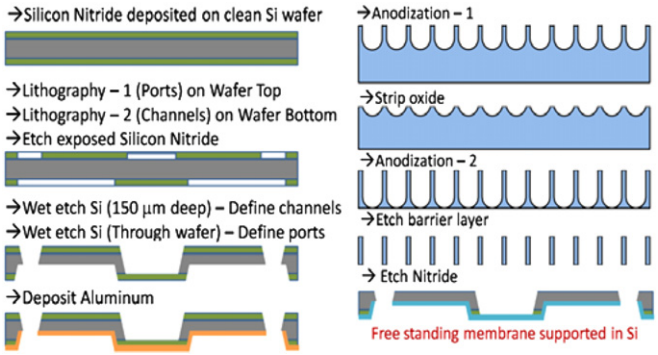
(*a*) (*b*)

Figure 5. Low (*a*) and high (*b*) magnification SEM images of the PAA membrane showing uniform distribution of cylindrical nanopores with a nominal diameter of 60 nm.

1 min, UV-exposed and developed (using MF319, Shipley) at room temperature for 1 min. The exposed silicon nitride underneath the patterned resist is etched using deep reactive ion etching (DRIE). This provides a patterned nitride layer to etch the exposed silicon to define inlet/outlet channels and ports. Silicon was anisotropically wet-etched in a potassium hydroxide (KOH) bath (stirred and maintained at 85 °C), to yield channels and ports as illustrated in figure 1. The etch rates of silicon as a function of the temperature and concentration of KOH can be found in [15, 16].

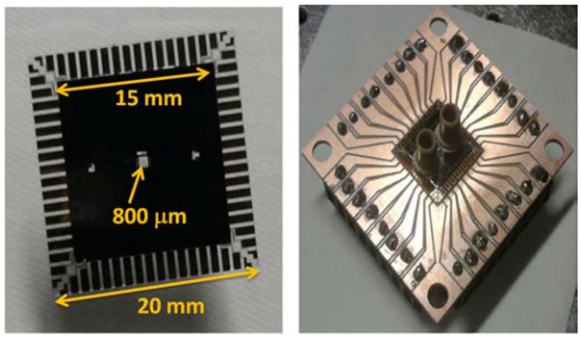
Co-fabrication of a nanoporous membrane (porous anodic alumina, PAA) on the silicon substrate utilizes a two-step PAA fabrication process [17–24]. With channels and ports already fabricated, a uniform layer of pure aluminum (99.99% or higher, 10 μm thick) is deposited using E-beam on the silicon substrate. The wafer is then diced into samples with overall dimensions of 15 mm × 15 mm. The PAA fabrication is initiated with anodization of the E-beam deposited aluminum in 0.3 M oxalic acid, stirred and maintained at 0 °C. An anodization voltage of 40 V is applied using a dc power supply (Agilent 6035 A). The samples are then immersed in a solution of chromic (1.5 wt%) and phosphoric acid (6 wt%) stirred at 60 °C [25] to etch away the layer of aluminum oxide formed by the first anodization step. This leaves behind a nano-structured surface with indentations that act as pore-initiation sites for a second anodization step. The second anodization step is carried out with similar parameters as the first step, for a prolonged duration (exceeding 24 h) to ensure anodization through the entire thickness of aluminum. The appearance of a transparent layer of dielectric (alumina) marks the end of the second anodization step. The samples are then dipped in the buffered oxide etchant (BOE) at room temperature to etch away the nitride layer supporting the alumina membrane layer from the back. While a photo-resist can be used to protect alumina during BOE etch of silicon nitride, exposed alumina is not found to be severely attacked. This is illustrated in figures 4(*a*) and (*b*), comparing SEM images of PAA samples before and after immersion in BOE.

Followed by removal of the nitride using BOE, the barrier layer in porous alumina is etched away by immersion of samples in H_3PO_4 for 45 min at room temperature (∼20 °C). The pore opening and widening process can also be monitored and controlled as described in [26–28]. This results in open pores with a nominal diameter of 60 nm (figures 5(*a*) and (*b*)).



(*a*) (*b*)

Figure 6. Fabrication process for (*a*) micro-fluidic channels, and (*b*) porous anodic alumina.



(*a*) (*b*)

Figure 7. Top views of (*a*) the device after SU-8 bonding and making fluidic connections and (*b*) a wire-bonded device connected to the PCB with board-to-wire connectors.

The fabrication of channels/ports on the silicon substrate along with porous alumina is described pictorially in figure 6.

2.3. Adhesive bonding of Pyrex and silicon substrates

Adhesive bonding allows joining non-planar substrates and is carried out at much lower temperatures compared to anodic or fusion bonding. It is often used for the dual purpose of fabricating interlayer features as well as bonding [29–37]. Bonding of sensor and membrane substrates is carried out using an SU-8 interlayer. SU-8 is first spun onto the sensor substrate at 3500 RPM, followed by two-step pre-exposure bake at 65 °C (3 min) and 95 °C (7 min) on a hotplate. The substrate is then patterned under UV followed by a post-exposure bake at 95 °C (5 min). This is followed by developing the exposed substrate. Using a bonding jig, built in-house, the two substrates are aligned for bonding such that the porous membrane is positioned centrally over the hotspot on the sensor substrate. The aligned substrates are then placed in an oven at 180 °C with application of pressure creating an adhesive bond. Since no leaks are observed, the resulting bond strength is found sufficient to withstand typical pressure drops (∼15 kPa) associated with fluid flow in microchannels of this device. Figure 7(*a*) shows a complete MEMS device after adhesive bonding and fluidic connections (Nanoports, Upchurch Scientific) are made to the inlet/outlet ports. In order to interface with external hardware for data acquisition and experiment control, the device is wire-bonded to a PCB with board-to-wire connectors, as shown in figure 7(*b*).

3. Experimental characterization

The RTD calibration process determines each sensor's electrical resistance as a function of temperature. The process of calibration is carried out in a temperature controlled, forced convection oven (built in-house). While the temperature at different locations inside the oven is monitored using calibrated T-type thermocouples (±0.1 °C resolution), the electrical resistance of each RTD is recorded. A typical linear response between resistance and temperature of a 500 μm square hotspot heater (also serving as the hotspot temperature sensor) and neighboring RTDs is shown in figure 8(*a*). A linear regression model is used to relate temperature with electrical resistance for each sensor. (The coefficient of determination of linear models for all RTDs is found to be 1, suggesting a reliable linear fit between the two variables.)

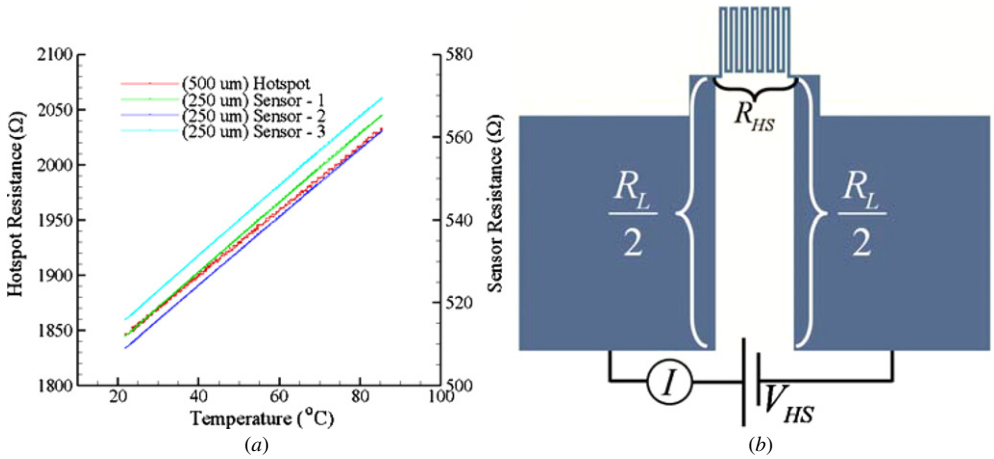
Figure 8(*b*) illustrates the circuitry for an RTD (e.g., hotspot heater/sensor) consisting of the electrical resistances of heater/sensor itself (R_{HS}) and metal lines (R_L) connecting the sensor to the power source. The heater/sensors are designed such that $R_{HS} \gg R_L$ ($R_{HS} \sim 600\ \Omega$ in comparison to $R_L \sim 5\ \Omega$) to ensure localized heating (at hotspot) and temperature measurements (at different sensor locations). Experiments are carried out by applying a bias of V_{HS} across the hotspot using a dc power supply (Agilent E3640A), while the current, I and RTD resistances are recorded using a data acquisition system (Agilent 34970A). At the hotspot, Joule heating is caused by activating the power supply, while the temperature and the heat flux dissipated are determined by measuring the resistance (V_{HS}/I) and the total power input ($V_{HS} \times I$), respectively. It is to be noted that the total power generated at the hotspot ($V_{HS} \times I$) is dissipated either by active cooling from the top, or by heat spreading through the substrate,

$$\dot{q} = \dot{q}_c + \dot{q}_{sp}, \tag{1}$$

where $\dot{q}_c$ and $\dot{q}_{sp}$ denote the power dissipated by the active cooling and heat spreading, respectively. The extent of heat dissipation to the substrate due to spreading can be evaluated as

$$\dot{q}_{sp} \approx \frac{(T_{hs} - T_\infty)}{R_{sp} + R_{1D} + R_{conv}}, \tag{2}$$

where T_{hs} and T_∞ represent the hotspot and ambient temperature, respectively; R_{sp} represents the thermal resistance to heat spreading into the substrate from an infinitesimally thin, square-shaped heat source emanating a constant heat flux into a semi-infinite domain; and R_{1D} and R_{conv} represent thermal resistances corresponding to one-dimensional heat conduction through the substrate and free convection, respectively. These resistances are estimated as $R_{1D} = \frac{\delta_{sub}}{k_{sub} A_{sub}}$ and $R_{conv} = \frac{1}{h_\infty A_{sub}}$, where δ_{sub}, k_{sub} A_{sub} denote the substrate thickness, thermal conductivity and area, respectively, and h_∞ is the heat transfer coefficient (HTC)



(*a*) (*b*)

Figure 8. (*a*) A typical (linear) resistance versus temperature calibration curve obtained for the central hotspot and three surrounding RTDs; (*b*) an illustration of the electrical circuit consisting of resistances of hotspot and metal line in series with a dc power supply.

corresponding to free convection. The spreading resistance can be related to the substrate thermal conductivity and the heat source characteristic length using the following semi-empirical equation [38, 39]:

$$R_{\text{sp}} = \frac{0.4732}{k_{\text{sub}}\ell_{hs}} \tag{3}$$

with $k_{\text{sub}} = 1.1$ W mK^{-1}, $\ell_{hs} = 2.5 \times 10^{-4}$ m, $\delta_{\text{sub}} = 5.0 \times 10^{-4}$ m, $A_{\text{sub}} = 4.0 \times 10^{-4}$ m^2 and $h_\infty = 10$ W m^{-2} K^{-1}; the total thermal resistance is given by $R_{\text{total}} = R_{\text{sp}} + R_{1\text{D}} + R_{\text{conv}} = 1972$ K W^{-1}. The heat flux dissipated by active cooling is then calculated as

$$\dot{q}''_c = \frac{\dot{q} - \dot{q}_{\text{sp}}}{A_{hs}}, \tag{4}$$

and the overall HTC of the active cooling mechanism is defined as

$$h_c = \frac{\dot{q}''_c}{(T_{hs} - T_\infty)}, \tag{5}$$

where $\dot{q}''_c$ is the heat flux dissipated corresponding to a hotspot temperature of $T_{hs} = 85\,^\circ$C. Note that T_∞ represents the ambient room temperature ($=21.1 \pm 0.05\,^\circ$C) recorded during the experimental characterization of the device. Further details on data analysis are available in [40].

To promote evaporation, air jet impingement from a nozzle (1 mm diameter) is implemented using a miniature diaphragm pump (Hargraves, BTC-Miniature Diaphragm Pump). The nozzle is held in place using a positioning tool that can control the angle of impingement and the nozzle-to-membrane separation (as shown in figure 9). An air flow meter (GFM371S, Aalborg) and a pressure transducer (Omega) are used in series with the air pump to measure the volumetric air flow rate (AFR) and supply line pressure, respectively. These measurements are used to calculate the velocity of air exiting the nozzle. All experiments requiring jet impingement of air are carried out at normal incidence to the surface. The liquid coolant (de-ionized, (DI) water) is delivered at extremely low coolant flow rates (CFR) ($\sim 10^{-10}$ to 10^{-8} m^3 s^{-1}) using a syringe pump (SPI).

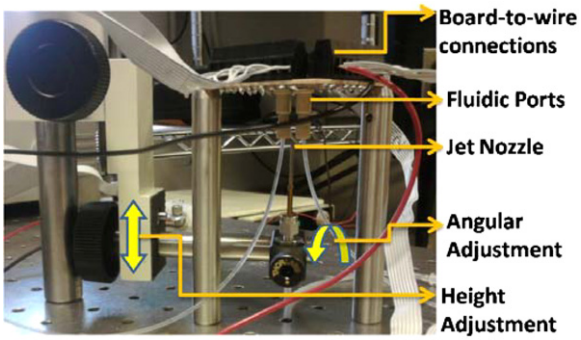


Figure 9. The device test rig complete with the fluidic and electrical connections and an air jet nozzle. The PCB is also shown, which is inverse-mounted for a clear view of the sensor substrate from the top. This allows for visual/optical monitoring the coolant flow in the channel during operation.

All experiments are performed on devices with hotspot dimensions of 250 × 250 μm. From our earlier theoretical analysis [14], the two operating parameters that can significantly affect the thermal and mass transfer resistances and therefore the rate of thin film evaporation are the CFR and the AFR, respectively. Therefore, performance characterization of the cooling device is carried out to assess its response to different combinations of the CFR and AFR. In order to estimate the extent of improvement achievable using this cooling mechanism, the following two relevant baseline tests are initially conducted to form a basis for comparison: (1) purely jet impingement of air (i.e. no liquid coolant) for varying the AFR and the nozzle-to-hotspot separation, and (2) single-phase micro-channel liquid cooling (i.e. no evaporation due to blocked membrane) for varying the CFR.

4. Results and discussion

4.1. Air jet impingement cooling (baseline test 1)

Forced convection using air jet impingement is carried out by exposing the hotspot heater/sensor on the Pyrex substrate

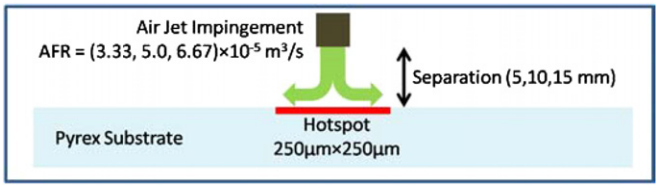


Figure 10. Schematic diagram showing the experimental arrangement of the baseline experiments of jet impingement air cooling. The AFRs and nozzle-to-hotspot separations are varied to analyze their effect on the HTC for the normal incidence.

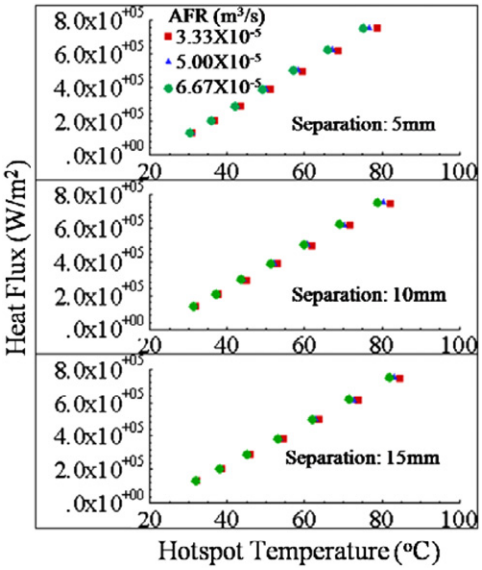


Figure 11. Heat flux dissipated by air jet impingement for different AFRs and nozzle-to-hotspot separations.

to the air jet with normal incidence. Moreover, to eliminate any additional thermal resistance due to the presence of a membrane and an intermediate SU-8 layer, the silicon substrate is not bonded with Pyrex, as illustrated in figure 10.

The experiments are carried out to analyze two important parameters that affect overall cooling: the mean jet velocity and the nozzle-to-hotspot separation. The AFR is varied between 3.33×10^{-5} m^3 s^{-1} and 6.67×10^{-5} m^3 s^{-1}, which correspond to impingement velocities of 37–74 m s^{-1}, while the nozzle-to-hotspot separation is varied from 5.0×10^{-3} to 1.5×10^{-3} m. Under these operating conditions, heat from the hotspot is dissipated by turbulent forced convection of air flow within the stagnation zone of the jet. These experiments are conducted inside an enclosure to avoid interaction of stray air currents with the air jet and repeated to ensure consistency of measurements.

Figure 11 shows the linear variation of the dissipated heat flux with the hotspot temperature at steady state. The average HTC defined by equation (5) for each set of operating conditions is summarized in table 2. As expected, the HTC is found to increase with an increase in the mean jet velocity and with a decrease in nozzle-to-hotspot separation. The HTC values of just over 5.5 kW m^{-2} K^{-1} are demonstrated corresponding to the smallest nozzle separation (5 mm) and the highest mean velocity (74 m s^{-1}).

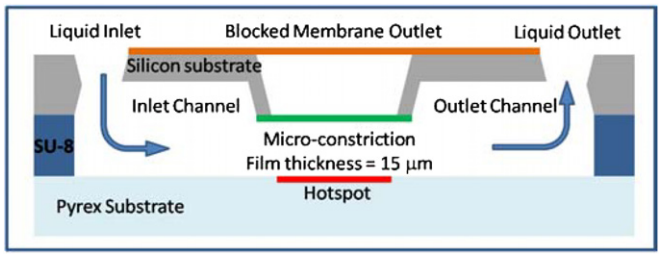


Figure 12. Hotspot thermal management using single-phase liquid flow in the microchannel.

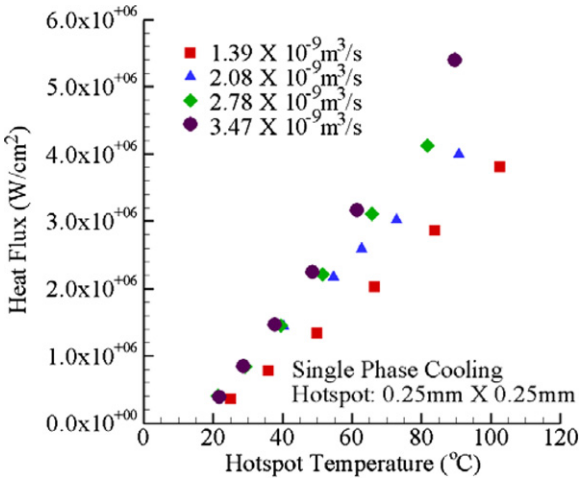


Figure 13. Heat flux dissipated by single-phase liquid flow for different CFRs.

Table 2. The HTC (kW m^{-2} K^{-1}) demonstrated by air jet impingement corresponding to different operating conditions.

AFR/ Separation	3.33×10^{-5} m^3 s^{-1}	5.0×10^{-5} m^3 s^{-1}	6.67×10^{-5} m^3 s^{-1}
5 mm	4.6 ± 0.1	5.1 ± 0.2	5.5 ± 0.2
10 mm	3.8 ± 0.1	4.2 ± 0.1	4.5 ± 0.3
15 mm	3.3 ± 0.2	3.6 ± 0.1	3.8 ± 0.3

4.2. Single-phase microchannel liquid cooling (baseline test 2)

A simple modification is made to the fabricated cooling device to carry out single-phase microchannel liquid cooling. The membrane outlet is blocked to avoid any evaporation to take place through the membrane as schematically shown in figure 12. With a blocked membrane and without air jet impingement, the cooling is only due to single-phase flow of liquid coolant in the micro-constriction. The CFR is varied between 1.39×10^{-9} m^3 s^{-1} and 3.47×10^{-9} m^3 s^{-1}. The heat flux dissipated as a function of hotspot temperature is shown in figure 13, and the HTCs (given by equation (5)) under these conditions are listed in table 3. An increase in power dissipation with an increase in the CFR is due to a reduction in the bulk fluid temperature associated with lower sensible heating of the fluid, which in combination with an approximately constant HTC for fully developed laminar flow in the micro-constriction results yields an improvement in observed heat fluxes.

Table 3. The HTC (kW m^{-2} K^{-1}) demonstrated by single-phase liquid cooling in microchannels corresponding to different flow rates at a hotspot temperature of 85 °C.

CFR (m^3 s^{-1})	1.39×10^{-9}	2.08×10^{-9}	2.78×10^{-9}	3.47×10^{-9}
HTC (kW m^{-2} K^{-1})	39 ± 0.4	56 ± 0.6	65 ± 0.7	76 ± 0.8

Table 4. HTCs achieved by thin-film evaporation at hotspot temperatures approaching 85 °C and constant liquid CFR.

AFR (m^3 s^{-1})	2.50×10^{-5}	3.33×10^{-5}	4.17×10^{-5}	5.00×10^{-5}
CFR (m^3 s^{-1})	2.78×10^{-9}	2.78×10^{-9}	2.78×10^{-9}	2.78×10^{-9}
HTC (kW m^{-2} K^{-1})	89 ± 0.9	94 ± 0.9	92 ± 0.9	88 ± 0.9

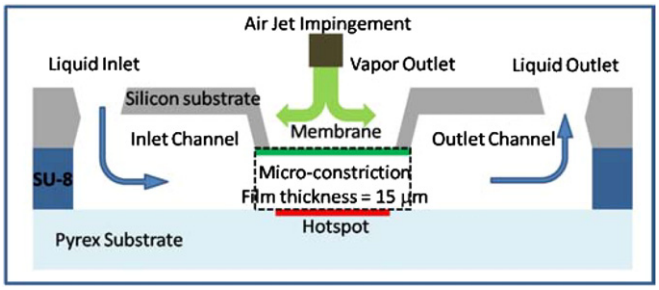


Figure 14. Hotspot thermal management using thin film evaporative cooling: air and CFRs are varied to determine their effect on the average HTC.

4.3. Gas-assisted thin-film evaporative cooling

The coolant and AFRs are varied to determine the change in the overall HTC for gas-assisted liquid evaporation from membrane-confined thin films (as shown in figure 14). Figures 15 and 16 show the net heat flux dissipated by the cooling mechanism as a function of the hotspot temperature for different combinations of air and CFRs for a nozzle to a substrate separation of 1 mm. These results clearly demonstrate the ability to dissipate heat fluxes in excess of 6 MW m^{-2} while maintaining junction temperatures below 95 °C, which correspond to average HTCs approaching 0.1 MW m^{-2} K^{-1}. The average HTCs evaluated at junction temperatures close to 85 °C under different operating conditions are listed in tables 4 and 5.

Evaporative cooling clearly yields an improvement in performance compared to the baseline tests with purely air jet impingement and single-phase microchannel liquid cooling. By comparing the highest HTCs demonstrated by different modes of heat dissipation, evaporative cooling yields a 17 times improvement over jet impingement and about 25% increase over single-phase microchannel cooling.

For a particular hotspot temperature, the dissipated heat flux can be enhanced either by increasing the air or the CFR. In order to further enhance performance, the dominant resistance limiting the performance of the nanopatch can be identified from these experimental results. Figure 15 and table 4 present heat fluxes dissipated for different AFRs (2.5 – 5 × 10^{-5} m^3 s^{-1}), while maintaining a constant CFR of 2.78 × 10^{-9} m^3 s^{-1}. The corresponding HTCs are large, but vary relatively little 0.088–0.094 MW m^{-2} K^{-1} with change in AFRs. On the other hand, a relatively large change in a HTC

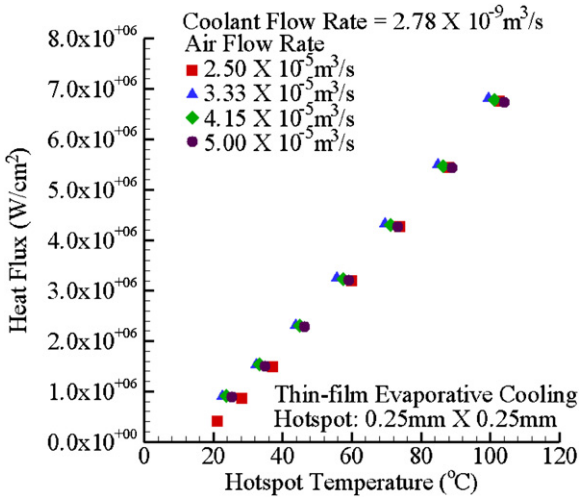


Figure 15. Heat flux dissipated corresponding to a constant CFR but a varying AFR.

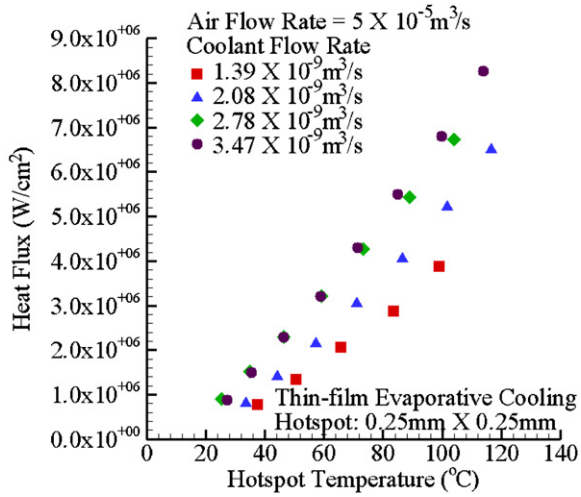


Figure 16. Heat flux dissipated corresponding to a constant AFR but a varying CFR.

is demonstrated varying the CFRs (1.39–3.47 × 10^{-9} m^3 s^{-1}) with AFR maintained at 5 × 10^{-5} m^3 s^{-1}, as shown in figure 16 and table 5. In this case, the HTC is almost doubled from 0.045 to 0.085 MW m^{-2} K^{-1} for an increase in the CFR from 1.39 × 10^{-9} to 3.47 × 10^{-9} m^3 s^{-1}. This indicates that the dominant resistance limiting the cooling performance of the device is either convection in the thin film or vapor transport within the membrane. The former can be decreased by further

Table 5. HTCs achieved by thin-film evaporation at hotspot temperatures approaching 85 °C and constant AFR.

AFR ($m^3\ s^{-1}$)	5.0×10^{-5}	5.0×10^{-5}	5.0×10^{-5}	5.0×10^{-5}
CFR ($m^3\ s^{-1}$)	1.39×10^{-9}	2.08×10^{-9}	2.78×10^{-9}	3.47×10^{-9}
HTC ($kW\ m^{-2}\ K^{-1}$)	45 ± 0.5	61 ± 0.6	79 ± 0.8	85 ± 0.9

thinning the film or increasing the CFR (thus, lowering the mean fluid temperature), whereas the membrane thickness and porosity control the latter. Hence, based on these observations, further optimization of the nanopatch design should result in improvement in cooling performance.

5. Summary and conclusions

A novel cooling approach and its device realization for applications that require dissipation of large heat loads from low form-factor areas, such as hotspot thermal management, is discussed. A chip-mountable MEMS device (termed 'perspiration nanopatch') takes advantage of highly efficient evaporation from a thin liquid film exposed to an impinging gas flow for dissipation of high heat fluxes while maintaining low junction temperatures. Design and fabrication of the device integrate various heterogeneous processes to create the micro-fluidic and nano-scale heat transfer enhancing features on different substrates. The resulting device allows for integrated measurement/sensing of cooling performance under different heating conditions and for different cooling modes. Importantly, the compact design of the nanopatch allows integration with a suitable background cooling system, such as microchannels or pin-fin arrays etc.

Performance characterization of the device focused on assessing the effect of two key operating parameters, the liquid coolant and AFRs, which directly affect thermal and mass transfer resistances. Comprehensive experiments conducted on a 250 μm sized square hotspot allows us to estimate the extent of improvement achievable over a purely air jet and a single-phase microchannel liquid cooling. The baseline experiments of air impingement cooling show the maximum HTC of only 5.5 $kW\ m^{-2}\ K^{-1}$, corresponding to a jet velocity of 75 $m\ s^{-1}$ (AFR of $6.67 \times 10^{-5}\ m^3\ s^{-1}$) and a nozzle-to-hotspot separation of 5 mm. Through evaporative cooling, it is possible to enhance the HTC almost 16-fold to reach 85 $kW\ m^{-2}\ K^{-1}$ with the liquid CFR of $3.47 \times 10^{-9}\ m^3\ s^{-1}$ and the AFR of $5.0 \times 10^{-5}\ m^3\ s^{-1}$. Also, by comparing the highest HTCs, evaporative cooling demonstrates a 25% increase over single-phase microchannel liquid cooling.

Heat fluxes in excess of 600 $W\ cm^{-2}$ are consistently demonstrated with hotspot temperatures approaching 95 °C. Clearly, a much higher heat flux can be dissipated by evaporation compared to the CHF demonstrated by pool boiling, at surface temperatures well below saturation conditions. The results indicate a possibility of further enhancement of heat dissipation through reduction of rate limiting resistances. Experimental observations suggest that to enhance overall performance the thermal resistance of liquid film and the mass transfer resistance of vapor transport through the membrane need to be further reduced by maintaining even thinner film and using a smaller thickness membrane, respectively.

Acknowledgments

The authors acknowledge the support of the Interconnect Focus Center, one of five research centers funded under the Focus Center Research Program, a DARPA and Semiconductor Research Corporation program. They would also like to thank the contributions of National Nanotechnology Infrastructure Network's (NNIN) summer intern, Julia Sukol and NNIN for collaborating with our efforts in micro-fabrication.

References

[1] ITRS 2007 Executive summary, 2007 edition. International technology roadmap for semiconductors, online at www.itrs.net

[2] Hamann H F, Weger A, Lacey J A, Hu Z, Bose P, Cohen E and Wakil J 2007 Hotspot-limited microprocessors: direct temperature and power distribution measurements *IEEE J. Solid-State Circuits* **42** 56–65

[3] Mudawar I 2001 Assessment of high-heat-flux thermal management schemes *IEEE Trans. Compon. Packag. Technol.* **24** 122–41

[4] Bar-Cohen A, Arik M and Ohadi M 2006 Direct liquid cooling of high flux micro and nano electronic components *Proc. IEEE* **94** 1549–70

[5] Agostini B, Fabbri M, Park J E, Wojtan L, Thome J R and Michel B 2007 State of the art of high heat flux cooling technologies *Heat Transfer Eng.* **28** 258–81

[6] Pijnenburg R H W, Dekker R, Nicole C C S, Aubry A and Eummelen E H E C 2004 Integrated micro-channel cooling in silicon *Proc. 34th ESSDERC: Solid-State Device Research Conf. (2004)* pp 129–32

[7] Hetsroni G, Gurevich M and Rozenblit R 2006 Sintered porous medium heat sink for cooling of high-power mini-devices *Int. J. Heat Fluid Flow* **27** 259–66

[8] Overholt M R, McCandless A, Kelly K W, Becnel C J and Motakef S 2005 Micro-jet arrays for cooling of electronic equipment *Proc. 3rd Int. Conf. Microchannels and Minichannels* (Toronto, ON: American Society of Mechanical Engineers) Part B, pp 249–52

[9] Faulkner D, Khotan M and Shekarriz R 2003 *Practical Design of a 1000 W/cm^2 Cooling System* (San Jose, CA: Institute of Electrical and Electronics Engineers) pp 223–30

[10] Kosar A, Kuo C J and Peles Y 2005 Boiling heat transfer in rectangular microchannels with reentrant cavities *Int. J. Heat Mass Transfer* **48** 4867–86

[11] Chen Z Q, Cheng P and Zhao T S 2000 An experimental study of two phase flow and boiling heat transfer in bi-dispersed porous channels *Int. Commun. Heat Mass Transfer* **27** 293–302

[12] Bar-Cohen A, Sherwood G and Hodes M 1994 Gas-assisted evaporative cooling of high density electronic modules *InterSociety Conference on Thermal Phenomena in Electronic Systems, 1994. I-THERM IV. 'Concurrent Engineering and Thermal Phenomena'* pp 32–40

[13] Fedorov A G Nano-patch thermal management devices, methods, and systems *US Patent No* 7545644

[14] Narayanan S, Fedorov A G and Joshi Y K 2009 Gas-assisted thin-film evaporation from confined spaces for dissipation of high heat fluxes *Nanoscale Microscale Thermophys. Eng.* **13** 30–53
[15] Williams K R and Muller R S 1996 Etch rates for micromachining processing *J. Microelectromech. Syst.* **5** 256–69
[16] Williams K R, Gupta K and Wasilik M 2003 Etch rates for micromachining processing: part II *J. Microelectromech. Syst.* **12** 761–78
[17] Crouse D, Lo Y, Miller A and Crouse M 2000 Self-ordered pore structure of anodized aluminum on silicon and pattern transfer *Appl. Phys. Lett.* **76** 49
[18] Jessensky O, Müller F and Gösele U 1998 Self-organized formation of hexagonal pore arrays in anodic alumina *Appl. Phys. Lett.* **72** 1173
[19] Lee W, Ji R, Gösele U and Nielsch K 2006 Fast fabrication of long-range ordered porous alumina membranes by hard anodization *Nat. Mater.* **5** 741–7
[20] Li A, Müller F, Birner A, Nielsch K and Gösele U 1998 Hexagonal pore arrays with a 50–420 nm interpore distance formed by self-organization in anodic alumina *J. Appl. Phys.* **84** 6023
[21] Masuda H and Fukuda K 1995 Ordered metal nanohole arrays made by a two-step replication of honeycomb structures of anodic alumina *Science* **268** 1466
[22] Masuda H, Yamada H, Satoh M, Asoh H, Nakao M and Tamamura T 1997 Highly ordered nanochannel-array architecture in anodic alumina *Appl. Phys. Lett.* **71** 2770
[23] Rabin O, Herz P, Lin Y, Akinwande A, Cronin S and Dresselhaus M 2003 Formation of thick porous anodic alumina films and nanowire arrays on silicon wafers and glass *Adv. Funct. Mater.* **13** 631–8
[24] Wu Z, Richter C and Menon L 2007 A study of anodization process during pore formation in nanoporous alumina templates *J. Electrochem. Soc.* **154** E8
[25] Li Y, Meng G W, Zhang L D and Phillipp F 2000 Ordered semiconductor ZnO nanowire arrays and their photoluminescence properties *Appl. Phys. Lett.* **76** 2011
[26] Brevnov D, Rama Rao G, López G and Atanassov P 2004 Dynamics and temperature dependence of etching processes of porous and barrier aluminum oxide layers *Electrochim. Acta* **49** 2487–94
[27] Han C, Willing G, Xiao Z and Wang H 2007 Control of the anodic aluminum oxide barrier layer opening process by wet chemical etching *Langmuir* **23** 1564–8
[28] Lillo M and Losic D 2009 Pore opening detection for controlled dissolution of barrier oxide layer and fabrication of nanoporous alumina with through-hole morphology *J. Membr. Sci.* **327** 11–7
[29] Agirregabiria M, Blanco F, Berganzo J, Arroyo M, Fullaondo A, Mayora K and Ruano-Lopez J 2005 Fabrication of SU-8 multilayer microstructures based on successive CMOS compatible adhesive bonding and releasing steps *Lab Chip* **5** 545–52
[30] Blanco F, Agirregabiria M, Garcia J, Berganzo J, Tijero M, Arroyo M, Ruano J, Aramburu I and Mayora K 2004 Novel three-dimensional embedded SU-8 microchannels fabricated using a low temperature full wafer adhesive bonding *J. Micromech. Microeng.* **14** 1047–56
[31] Francisco J B, Maria A, Maria T, Javier B, Jorge G, Maria A, Jesus M R, Inigo A and Kepa M 2004 Novel low-temperature CMOS-compatible full-wafer-bonding process for the fabrication of 3D embedded microchannels using SU-8 *Proc. SPIE* **5276** 131–42
[32] Carlier J, Arscott S, Thomy V, Fourrier J, Caron F, Camart J, Druon C and Tabourier P 2004 Integrated microfluidics based on multi-layered SU-8 for mass spectrometry analysis *J. Micromech. Microeng.* **14** 619–24
[33] Chen Y and Lee D 2007 A bonding technique using hydrophilic SU-8 *J. Micromech. Microeng.* **17** 1978–84
[34] Li S, Freidhoff C, Young R and Ghodssi R 2003 Fabrication of micronozzles using low-temperature wafer-level bonding with SU-8 *J. Micromech. Microeng.* **13** 732–8
[35] Svasek P, Svasek E, Lendl B and Vellekoop M 2004 Fabrication of miniaturized fluidic devices using SU-8 based lithography and low temperature wafer bonding *Sensors Actuators* A **115** 591–9
[36] Tuomikoski S and Franssila S 2004 Wafer-level bonding of MEMS structures with SU-8 epoxy photoresist *Phys. Scr.* **114** 223–6
[37] Tuomikoski S and Franssila S 2005 Free-standing SU-8 microfluidic chips by adhesive bonding and release etching *Sensors Actuators* A **120** 408–15
[38] Yovanovich M, Culham J and Teertstra P 1998 Analytical modeling of spreading resistance in flux tubes, half spaces, and compound disks *IEEE Trans. Compon. Packag. Manuf. Technol.* A **21** 168–76
[39] Yovanovich M, Muzychka Y and Culham J 1999 Spreading resistance of Iso ux rectangles and strips on compound flux channels *J. Thermophys. Heat Transfer* **13** 495–500
[40] Narayanan S, Fedorov A G and Joshi Y K 2010 Experimental characterization of a micro-scale thin-film evaporative cooling device *ITHERM (Las Vegas)* accepted