Superconducting FET circuits for analogue VLSI signal processing

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Superconducting FET circuits for analogue VLSI signal processing

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Abstract. CMOSuFET (complementary metal–oxide–superconductor field-effect transistor) discrete-time current-mode (DM) and continuous-time current-mode (CM) circuits for an analogue VLSI (very-large-scale-integrated) signal processing system are described. A family of modules—a simple sampled-data current memory circuit, a current delay circuit, a current integrator, a continuous-time current mirror, and an amplifier—are presented. Their main advantage lies in the very high frequency response, and very low power dissipation. The circuits have extensive development potential for high-performance analogue VLSI signal processing systems.

1. Introduction

Because of the continual enlargement of analogue and digital electron signal processing systems, the design of micro-power-dissipation, super-high-frequency-response analogue VLSI (very-large-scale-integrated) processing becomes more and more important. The most important part of the design process is finding a device and circuit to meet the above performance requirements. Since a MOSuFET (metal–oxide–superconductor field-effect transistor) has a very large transconductance g_{ms} and very low conductance g_{DS} for a drain–source voltage V_{DS} that is very low (but that cannot be equal to zero)—which lead to it having very low power dissipation and a very high frequency response—it is an ideal basic VLSI device [1]. As it penetrates into the development of information science and technology, analogue signal processing equipment will be largely in the form of complex systems. However, its basic functions are very simple: (1) signal inversion, (2) summation, (3) scaling, (4) memory, (5) delay, etc. It can be realized by using either a discrete-time current-mode (DM) CMOSuFET (complementary metal–oxide–superconductor field-effect transistor) circuit or a continuous-time current-mode (CM) CMOSuFET circuit. If CMOSuFETs can be used in future analogue and digital systems, an application in filters, analogue/digital converters, digital/analogue converters, and phase-code-modulation VLSI designs can be found.

2. Basic DM CMOSuFET circuits

2.1. DM memory circuits

Figure 1 shows a DM CMOSuFET memory circuit. When the switch M_s is closed by the clock pulse $\bar{\phi}$, the gate electrodes of M_1 and M_2 are connected through transformer T_{12}, the transformer ratio of T_{12} is 1:1, and the gate voltages of M_1 and M_2 change as a function of time:

$$v_{gs1}(t) = v_{gs2}(t) = v_{gs}(t). \tag{1}$$

The output current correspondingly changes as a function of time:

$$i_{out}(t) = i_{in}(t). \tag{2}$$

Therefore, the output current tracks the input current as shown in figure 1(b), where the circuit is in the tracking state.

When $t = T$, there is an inversion of the clock pulse from $\bar{\phi}$ to ϕ and the switch M_s will be opened. At that time, charges stored in the gate capacitance C_{gs2} of M_2 will change with respect to the product of C_{gs2} and the changes in gate voltage $v_{gs}(T)$, i.e. $q_{gs2}(T) = C_{gs2}v_{gs}(T)$. Correspondingly, the change of current is $i_{in}(T)$. Thus, the output signal current $i_{out}(t)$ will stay at the value $i_{in}(T)$ as shown in figure 1(c) when the switch is opened and the circuit is in the holding state, i.e.

$$i_{out}(t) = i_{in}(T). \tag{3}$$

The best possible memory functioning is thus achieved, because the MOSuFET switch has the ideal high frequency response and high speed.

2.2. DM delay circuits

Figure 2 shows a DM CMOSuFET delay circuit where the output current $i_{out}(t)$ is a non-inverted replica of the input current $i_{in}(t)$ except that it is delayed by one clock pulse period T_s.

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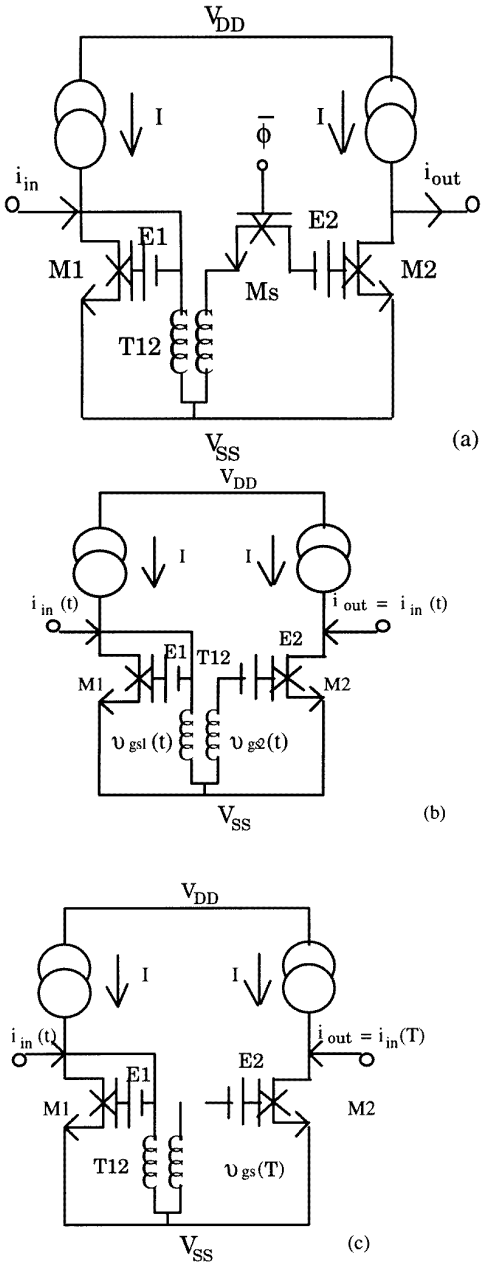

Figure 1. A DM CMOSuFET memory. (a) A DM inverting tracking and holding circuit. (b) Tracking operation. (c) Holding operation.

2.3. DM integrators

If a part of output current shown in figure 2 is fed back to the non-inverting input terminal, and an inverting input terminal is added in, an ideal DM CMOSuFET integrator can be obtained, as shown in figure 3. The integrator is composed of two cascade-connected current memory (tracking/holding) circuits. The switches are controlled by two-phase non-overlapping clock pulses, $\bar{\phi}$ and ϕ (all current-mirror–transistor pairs are assumed to be matched). As it passes through each tracking/holding circuit, the signal will invert once.

To employ the DM CMOSuFET integrator as a basic

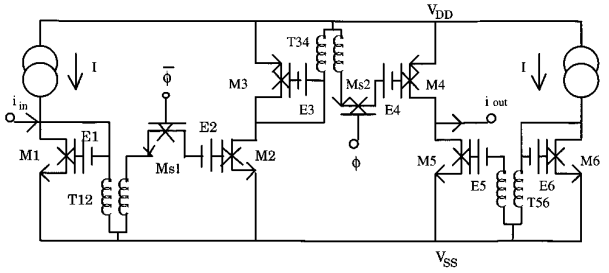

Figure 2. A DM CMOSuFET delay circuit.

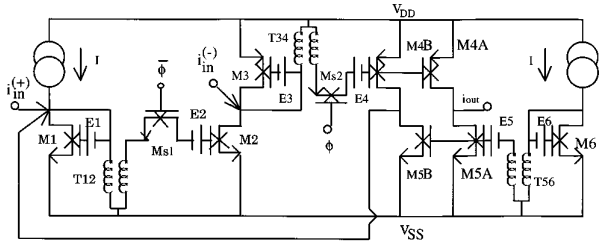

Figure 3. A DM CMOSuFET integrator.

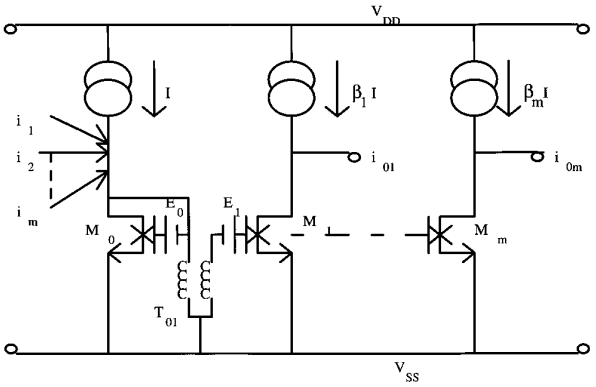

Figure 4. A CM CMOSuFET current mirror and current amplifier.

building block in active filter design, the output current must be scaled. The integrator output is weighted by the scaling aspect ratio of M_{4A} to M_{4B} and the output bias through a factor of K (figure 3). The output signal current is

$$i_{out}(z) = Ki_f(z) = K(i_{in}^{(+)}z^{-1} - i_{in}^{(-)}z^{-1/2})/(1 - z^{-1}). \tag{4}$$

The $(1 - z^{-1})$-term in the denominator represents an integration over discrete time. In the numerator, the input current at the non-inverting terminal $i_{in}^{(+)}$ is delayed by one period compared to the output current, and the input current at the inverting terminal $i_{in}^{(-)}$ is delayed by a half-period as compared to the output current. Also

$$K = [(W/L)_{4A}V_{CDS\ 4A}]/[(W/L)_{4B}V_{CDS\ 4B}] \tag{5}$$

$$V_{CDSi} = [V_{Ci}^2 + V_{DS}^2]^{1/2} \tag{6}$$

$$V_{Ci} = V_{CT}(L/\xi_N)\ \cosh^{-2}(L/2\xi_N) \tag{7}$$

$$V_{CT} = 4\Delta^2(T)/(\pi e K_B T) \tag{8}$$

where L is the channel length, and ξ_N is the coherence length of the semiconductor or semiconductor-like component

The current gain and phase errors of the DM CMOSuFET integrator can be analysed. First, we obtain an expression for the ideal DM CMOSuFET integrator wherein there is an open-loop current gain β_I equal to 1. Substituting $z = e^{i\omega T}$ and $\theta = \omega T_S/2$ into equation (4) with $T_S = 1/f_s$, $i_{out}(\omega)$, using equation (5), is

$$i_{out}(\omega) = [K/(i\omega T_S)](\theta/\sin\theta)(i_{in}^{(+)}e^{-i\theta} - i_{in}^{(-)}) \tag{9}$$

where $K/(i\omega T_S)$ represents continuous-time Miller integration, $\theta/\sin\theta$ represents the DM CMOSuFET current gain error due to the finite sampling frequency, and $e^{-i\theta}$ represents the phase error associated with the full-delay input. Re-evaluating the DM CMOSuFET integrator with $\beta_I < 1$ open-loop current gain, we obtain

$$i_{out}(z) = K(\beta_I i_{in}^{(+)} z^{-1} - \beta_2 i_{in}^{(-)} z^{-1/2})/(1 - \beta_I z^{-1}) \tag{10}$$

where we assume that the current gain of the first tracking/holding circuit is β_1 and that of the second tracking/holding circuit is β_2, indicated in figure 3, with $\beta_I = \beta_1\beta_2$.

Performing a similar analysis with equation (9), we find

$$i_{out}(\omega) = [K/(i\omega T_S)](\theta/\sin\theta)(\beta_I i_{in}^{(+)}e^{-i\theta} - \beta_2 i_{in}^{(-)}) \times[(e^{i\theta} - e^{-i\theta})/(e^{i\theta} - \beta_I e^{-i\theta})]. \tag{11}$$

The current gain error is

$$\Delta\beta_I^{(\omega)} = 2\sin\theta/[(1-\beta_I)^2\cos^2\theta + (1+\beta)^2\sin\theta]^{1/2} \tag{12}$$

and the phase error is

$$\Delta\phi_I^{(\omega)} = \tan^{-1}[(\cot an\,\theta)(1-\beta_I)/(1+\beta_I)]. \tag{13}$$

Present DM CMOSuFET currents typically achieve $\beta_I < 0.99$. Hence, for high-accuracy applications, the dynamic current mirror technique which eliminates mismatch-related gain errors should be used.

3. Basic CM CMOSuFET circuits

3.1. CM current mirrors and current amplifiers

Figure 4 shows CM CMOSFET current mirror and current amplifier circuits, which have many functions, such as summation, inversion, scaling, amplification and fan-out—in fact, all of the required computation repertoire except for memory can be realized.

The input-diode-connected MOSuFET M_o is biased by a current source I and a DC gate voltage E_1; as long as it remains forward biased, it provides a low-input-impedance summing node for the AC signal currents $i_1, i_2, \ldots, i_m$. The M_1 DC gate bias voltage, $E_1 = E_o$, is applied to an array of output MOSuFETs $M_1, M_2, \ldots, M_m$. Through a transformer T_{o1} the sum of the input signal currents $i_1, i_2, \ldots, i_m$ is converted to the gate electrodes of $M_1, M_2, \ldots, M_m$, while the output signal currents $i_{o1}, i_{o2}, \ldots, i_{om}$ can be gained from the drain electrodes of $M_1, M_2, \ldots, M_m$:

$$i_{oi} = -\beta_i(i_1 + i_2 + \ldots + i_m) \tag{14}$$

$$\beta_i = (N_1/N_o)[(W/L)_i/(W/L)_o](V_{ci}/V_{co}) \quad (i = 1, 2, \ldots, m) \tag{15}$$

where N_1/N_o is transformer ratio of T_{o1}, and $(W/L)_o$, $(W/L)_i$ are channel width–length ratios of M_o and M_i, respectively. V_{ci}/V_{co} is the ratio of characteristic voltages of M_i and M_o [2]. When $N_1/N_o = 1$, the drain–source current I_{dso} of M_o is the sum of the DC bias current I and signal current $i_1 + i_2 + \ldots + i_m$; that is

$$I_{dso} = I + \sum_{i=1}^{m} i_i. \tag{16}$$

The total peak signal current

$$\sum_{i=1}^{m} i_i$$

does not exceed the DC bias current I. The above facts show that the functions of summation, inversion, amplification, etc of an input signal current can be completed in the circuit shown as figure 4.

3.2. CM current integrators

Figure 5(a) shows a simplified schematic circuit diagram for a CM CMOSuFET differential integrator, while figure 5(b) shows an intrinsic small-signal model of the integrator, and figure 5(c) shows an ideal small-signal model of the integrator.

In figure 5, $C_1 = C_{GC1}, C_2 = C_p + C_{GC3}, C_{GC1}$ and C_{GC3} are the gate-channel capacitances of M_1 and M_3, respectively, C_p is an additional capacitance, the non-dominant frequency is defined by C_1, and the dominant frequency is defined by C_2. When $g_{ds1}, C_1, g_{ds2}, g_{ds3}$ and g_{ds4} are neglected in the intrinsic small-signal model, an ideal small-signal model can be obtained.

According to Kirchhoff's law (KCL), at the nodes A, B and C in figure 5(c), we have

$$i_{in}^{(+)} + i_f = g_{ms1}V_{GS1} \tag{17}$$

$$i_{in}^{(-)} = g_{ms2}V_{GS1} + (g_{ms3} + SC_2)V_{GS2} \tag{18}$$

and

$$i_f = -g_{ms4}V_{GS2}. \tag{19}$$

If matching needs to be accurate, the CM CMOSuFET current integrator is designed with $g_{ms1} = g_{ms2}$ and $g_{ms3} = g_{ms4}$. Substituting (17) and (19) into (18),

$$i_{in}^{(-)} = i_{in}^{(+)} + i_f + (g_{ms3} + SC_2)(-i_f/g_{ms3}) \tag{20}$$

and hence

$$i_f = (g_{ms3}/SC_2)(i_{in}^{(+)} - i_{in}^{(-)}). \tag{21}$$

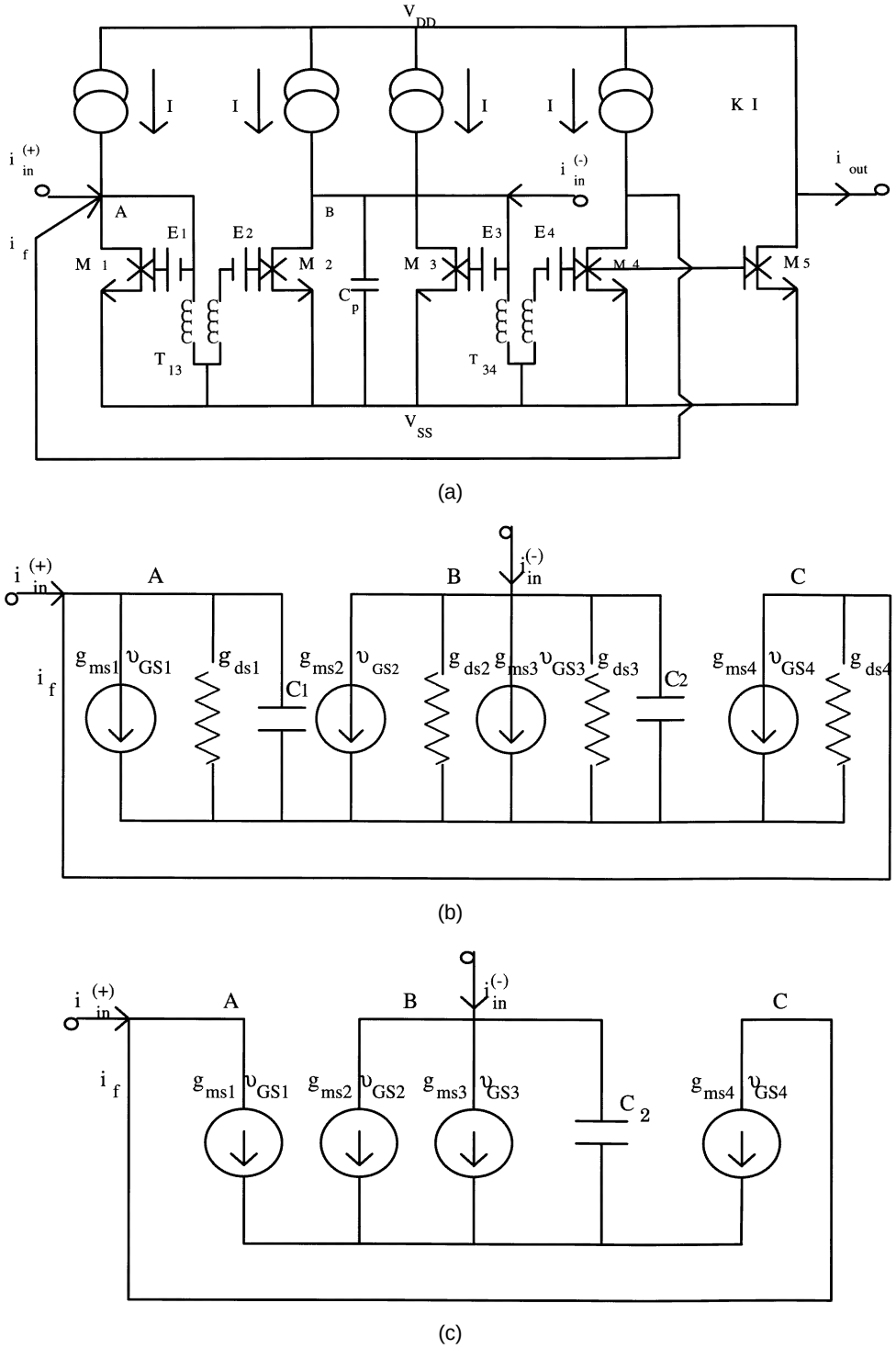

Figure 5. A CM CMOSuFET differential integrator. (a) A simplified schematic circuit diagram. (b) An intrinsic small-signal model. (c) An ideal small-signal model.

Thus, the gain constant of the CM CMOSuFET current integrator can be established using a capacitance C_2 and a scaled output branch; therefore

$$i_{out} = Ki_f = K(g_{ms3}/SC_2)(i_{in}^{(+)} - i_{in}^{(-)}). \qquad (22)$$

Since the dynamic range is typically maximized when $K \approx 1$, the unity-gain crossover frequency of the integrator is given by

$$\omega_0 \approx g_{ms3}/C_2. \qquad (23)$$

When the second-order effects on the accuracy and stability of the CM CMOSuFET integrator are taken into consideration—i.e., using an intrinsic small-signal model including $g_{ds1}, C_1, g_{ds2}, g_{ds3}$ and g_{ds4} as shown

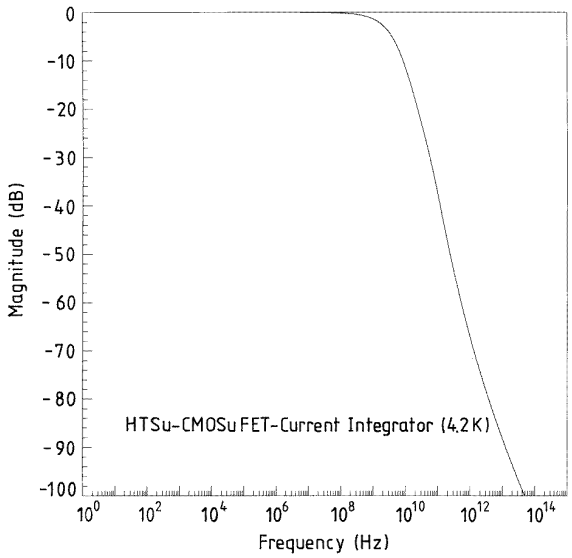

Figure 6. The frequency response of a CM CMOSuFET current integrator.

in figure 5(b), and assuming equal DC bias currents I, characteristic voltages V_{CT}, N_i/N_o ratios, and W/L ratio—we have $g_{msi} = g_{ms}$, $g_{dsi} = g_{ds}$, and the KCL method applied at the nodes A, B, and C now yields

$$i_{in}^{(+)} + i_f = (g_{ms} + g_{ds} + SC_1)V_{GS1} \tag{24}$$

$$i_{in}^{(-)} = g_{ms}V_{GS1} + (g_{ms} + 2g_{ds} + SC_2)V_{GS2} \tag{25}$$

and

$$i_f = -g_{ms}V_{GS2} - g_{ds}V_{GS1}. \tag{26}$$

Solving (24)–(26), we obtain

$$i_f = [K_0 - K_1(S - Z_1)]i_{in}^{(+)}/[(S - P_1)(S - P_2) - K_0] - K_2(S - Z_2)i_{in}^{(-)}/[(S - P_1)(S - P_2) - K_0] \tag{27}$$

$$i_{out} = Ki_f \tag{28}$$

where

$$K_0 = g_{ms}^2/C_1C_2 \tag{29}$$

$$K_1 = g_{ds}/C_1 \tag{30}$$

$$Z_1 = -(g_{ms} + 2g_{ds})/C_2 \tag{31}$$

$$K_2 = g_{ms}/C_2 \tag{32}$$

$$Z_2 = -(g_{ms} + g_{ds})/C_1 \tag{33}$$

$$P_1 = -(g_{ms} + 2g_{ds})/C_2 \tag{34}$$

$$P_2 = -(g_{ms} + 2g_{ds})/C_1. \tag{35}$$

The current gain of the CM CMOSuFET integrator is

$$\beta(\mathrm{i}\omega) = (K/2)(1 + N)[K_0 - K_1(S - Z_1)] \times [(S - P_1)(S - P_2) - K_0]^{-1} \tag{36}$$

where

$$N = K_2(S - Z_2)/[K_0 - K_1(S - Z_1)]. \tag{37}$$

An approximate expression for the CM CMOSuFET integrator quality factor Q is derived by assuming that effects of all non-dominant poles (and zeros) can be approximated to that of a single non-dominant pole located above the unity-gain frequency of the CM CMOSuFET integrator. Therefore, the two-pole approximate frequency response of the CM CMOSuFET current integrator is

$$b(\mathrm{i}\omega) = K/[(1 + \mathrm{i}\omega/P_1)(1 + \mathrm{i}\omega/P_2)] \tag{38}$$

$$|b(\mathrm{i}\omega)| = 20\log K - 20\log[1 + (\omega/P_1)^2]^{1/2} - 20\log[1 + (\omega/P_2)^2]^{1/2}. \tag{39}$$

Figure 6 shows the frequency response of a CM CMOSuFET differential integrator. In the computation, assuming that the channel length L is equal to 10^{-7} m, W/L is equal to 100, $V_{DS} = 10^{-9}$ V, $\mu_n = 1.42 \times 10^{-2}$ m^2 V^{-1} s^{-1}, $V_T = 0.1$ V, $E_i = 0.2$ V, and $N_D = 5 \times 10^{26}$ m^{-3} from m_1 to m_4. Evaluating $\beta(\mathrm{i}\omega)$ at the unity-gain crossover frequency of the CM CMOSuFET integrator yields, when $\omega = \omega_0$, equation (38) in the form

$$\beta(\mathrm{i}\omega_0) = K/[(1 + \mathrm{i}\omega_0/P_1)(1 + \mathrm{i}\omega_0/P_2)] = K/\{[1 - \omega_0^2/(P_1P_2)] + \mathrm{i}\omega_0(1/P_1 + 1/P_2)\}. \tag{40}$$

Since the Q-factor of the CM CMOSuFET integrator is defined as the ratio of the imaginary to the real part of the denominator polynomial, we have

$$\begin{aligned} Q &= \omega_0(1/P_1 + 1/P_2)/[1 - \omega_0^2/(P_1P_2)] \\ &\approx (\omega_0/P_1)/[1 - \omega_0^2/(P_1P_2)] \\ &\approx -(\omega_0/P_1)/[\omega_0^2/(P_1P_2)] \\ &= -P_2/\omega_0 \\ &= (g_{ms} + 2g_{ds})C_2/g_{ms}C_1. \end{aligned} \tag{41}$$

4. Conclusions

The structures and principles of CMOSuFET circuits for the basic functions in analogue discrete-time current-mode (DM) and continuous-time current-mode (CM) VLSI signal processing systems have been described. The study of DM and CM CMOSuFET analogue circuits shows that analogue VLSI systems can be developed using CMOSuFETs, to have better performance than semiconducting analogue VLSI systems [2]. It is possible that they will provide the basis of a new technology for future microelectronics systems with a large development potential.

Acknowledgment

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