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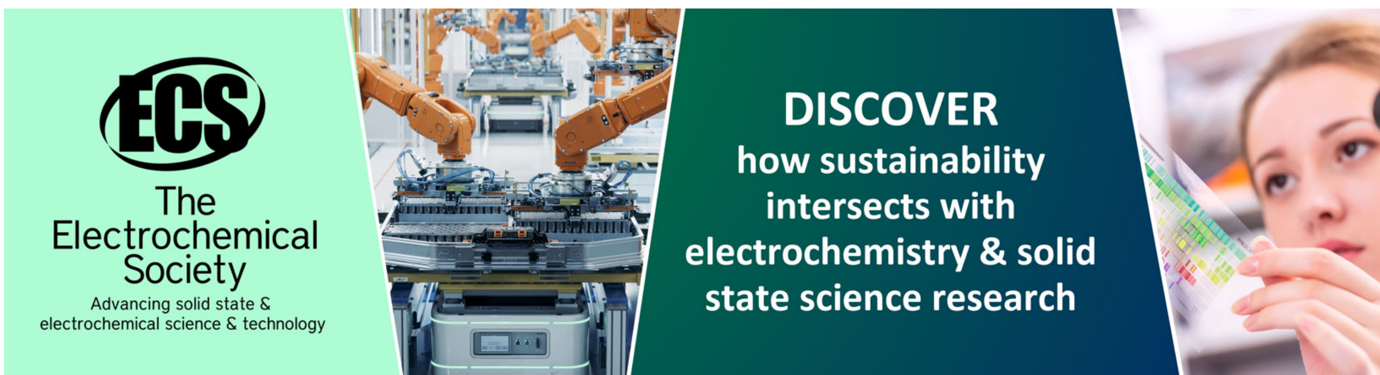

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Constant voltage stress induced current in Ta_2O_5 stacks and its dependence on a gate electrode

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Abstract
Response of 8 nm Ta_2O_5 stacks with different gates (Al, W and Au) to voltage stress at gate injection is studied by probing under various voltage/time conditions at room temperature and at 100 °C. A stress-induced leakage current (SILC) is detected in all samples and reveals gate dependence. It is established that the pre-existing traps actually govern this response, and the impact of gate-induced defects is stronger. The Au-gated devices are the most susceptible to the stress degradation. Two processes—electron trapping at pre-existing traps and positive charge build-up—are suggested to be responsible for generation of SILC. It is concluded that despite some gate effects, the origin of CVS degradation in this particular high-*k* dielectric is different from that in SiO_2.

1. Introduction

Fundamental differences between the bonding of SiO_2 and high-*k* insulators to Si make the direct use of SiO_2 knowledge unfeasible for interpretation of high-*k* properties. High-*k* dielectrics are trap-rich materials which originates from their electronic structure [1–5]. As a consequence they are not good glass formers like SiO_2, and have large concentrations of bulk traps, border traps and interface states. The probability of bias-induced charge trapping is high due to the large densities of these defects, a portion of which could be created during electrical stressing. That is why high-*k* dielectric reliability is still dominated by defect related degradation mechanisms [5–13] and not related to intrinsic properties. Despite the increasing interest in the reliability of high-*k* films (the electrical reliability will be critical for their application in nanoscale technologies) most of the data and models proposed for the degradation mechanisms are available for the family of hafnium-oxide-based materials as the most promising dielectrics for nanoscale MOSFETs [4–18]. Particularly for Ta_2O_5, one of the best high-*k* candidates for the storage capacitors in DRAMs, such data are almost completely missing, and the defects which act as precursors for breakdown are not specified. It emerges that high-voltage breakdown of Ta_2O_5 is determined by the interfacial layer, due to the high electric field across the interfacial layer which in turn leads to bulk Ta_2O_5 breakdown immediately after interface degradation [4, 7]. Since the degradation mechanisms are poorly understood and entirely different from those of SiO_2, the reliability models developed for SiO_2 cannot be easily transferred to high-*k* films. Briefly, the transition from SiO_2-based to high-*k* dielectric does have obstacles when directly applying the knowledge on degradation mechanisms in SiO_2 to high-*k* dielectrics. Recently [19], we have demonstrated that the changes of the electrical characteristics after constant current stress (CCS) of Ta_2O_5 stacks with different gates are addressed to gate-induced defects rather than to poor-oxidation related defects, and the parameters of the pre-existing traps define the stress response. It is also known that the properties of high-*k* films are very sensitive to the fabrication process and consequently to the nature of these pre-existing traps. This fact namely complicates the comparison of films with similar composition fabricated under different methods and makes it difficult to generalize a conclusion from a given set of samples to the whole family of high-*k* materials. All this motivates us

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to extend the investigations of degradation characteristics to different high-k alternatives. To understand the degradation mechanisms, more data on the effect of specific electrical stress (constant current stress or constant voltage stress) on the parameters of high-k-based devices are also needed. This work is focused on the effect of constant voltage stressing on the reliability of capacitors with thin Ta_2O_5. In a number of papers [20–27] we have reported that amorphous and stoichiometric Ta_2O_5 layers can be successfully obtained by thermal oxidation of a Ta film deposited on Si. Fabrication conditions providing films with high dielectric constant (of about 35) corresponding to a thick (~30 nm) film and leakage current density below 10^{-9} A cm^{-2} have been optimized. A special emphasis here will be put on the effect of the metal gate electrode (both the type of gate and the deposition technique) on the degradation of the capacitors after constant voltage stress (CVS).

2. Experimental procedure

Chemically cleaned p-type (1 0 0) 15 Ω cm p-Si wafers were used as substrates (the native SiO_2 was removed by etching the substrates in a 1% HF solution). A Ta film (~4 nm) was deposited on Si by rf sputtering of the Ta target in Ar atmosphere. Subsequently the Ta film was oxidized in dry O_2 at 550 °C to Ta_2O_5. More details on the sample preparation can be found in [20–23]. The oxidation temperature was chosen to be low enough to minimize the substrate oxidation and to prevent Ta silicide formation. The thickness d and the refractive index n of Ta_2O_5 layers were 8 nm and 2, respectively, as determined ellipsometrically ($\lambda = 632.8$ nm). Electrical measurements were performed on a set of MIS structures with three top electrodes (Al, W and Au). Al and Au electrodes were evaporated and W ones were deposited by rf sputtering of W in Ar atmosphere (gas pressure 3 Pa, rf power density of 3 W cm^{-2}). The capacitors with four gate areas, A, of 1, 2.25, 6.25 and 25 × 10^{-4} cm^2, were defined by photolithography. In order to examine the effect of CVS on the reliability of as-fabricated films, the samples experienced no post-deposition annealing and no post-metal annealing in forming gas. To analyze the stress-induced leakage current (SILC) the current–voltage J–V curves before and after CVS were measured. Negative CVS was performed with a voltage V_g, in the range of −1 to −6 V, stressing time t_s from 50 to 2000 s and at two temperatures, 20 and 100° C. We focused on negative V_g (gate injection) in these p-type MIS devices, as this is the most limiting condition in real working situations. The J–V measurements were performed within seconds and at the same temperature as the stressing, to minimize slow trapping/detrapping effects. The curves were recorded at both polarities before as well as after the stressing to get an insight into the spatial location of the stress-induced defects. All the measurements were performed with the Keithley 236 source measurement unit.

3. Results and discussions

Despite the insufficient physical understanding of the high-k reliability, in the following study we will refer to SILC as the stress-induced-steady-state leakage current and will use only general similarities and analogies with the case of SiO_2. By applying a CVS for a definite period of time and determining the change in the leakage current, SILC as well as such phenomena as soft and hard breakdown can be observed. The SILC at a given voltage can be expressed as a relative change in the leakage current $\Delta J/J_0 = (J_g - J_0)/J_0$, where J_0 and J_g are the currents corresponding to pre- and post-stress curves. $\Delta J/J_0$ is usually used as a measure of defect density created by the stress.

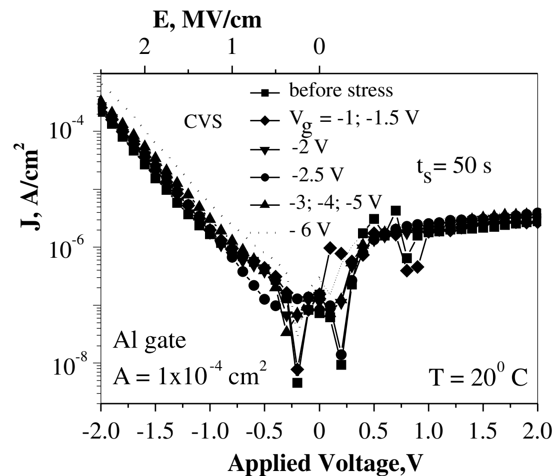

Figure 1. Pre- and post-stress leakage current characteristics of Al-gated capacitors. The stress conditions producing the corresponding curves are indicated. The upper x-axis shows J–E dependence.

3.1. CVC at 20 °C

3.1.1. Dependence on V_g, t_s = 50 s. Figure 1 shows the current density versus gate bias characteristics of fresh and stressed Al-gated capacitors; the stress voltage V_g varies from −1 to −6 V, at a fixed stress time of 50 s. The curves are reproducible and do not change when measured repeatedly several times. Here and further, the terms 'forward' and 'reverse' bias will be referred to the negative and positive voltages on the top electrode (p-type substrate), respectively, by analogy with the curves of diodes, and because of their common use in the high-k literature. The voltage range for measurement of the curves is chosen to be substantially below the largest stress voltages to ensure that the J–V measurement only samples the traps and does not generate any new ones. Note that the curves do not exhibit well-pronounced dependence on the gate area for all samples studied. At a first approximation this suggests that the films are homogeneous within the area range of 0.1–2.5 × 10^{-3} cm^2. The observed current fluctuations in the low-voltage range (~−0.3, +0.5 V) are attributed to a transient conduction which is known to have weak field dependence [27, 28]. The behavior of the transient current is not of interest here and we will focus on the change of the steady state current under CVS. The stressing with V_g from −1 to −5 V slightly affects the current in Al-gated capacitors: the current increase at forward bias is less than

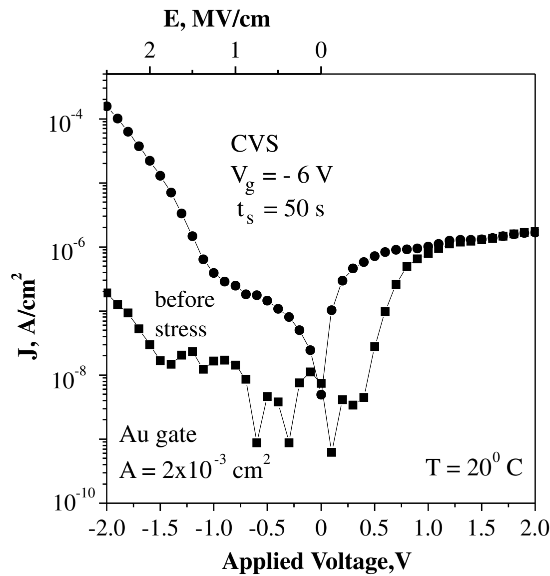

Figure 2. *J–V* curves before and after voltage stress of −6 V at 20 °C in Au-gated stack; $t_s = 50$ s.

∼30–50% for lower V_g and ∼50–100% for $V_g \sim -3$ to −5 V. At $V_g = -2.5$ V the transient current decays with ∼70% at around the −0.5 V applied voltage indicating electron trapping. The leakage current after −6 V stress under forward and reverse biases showed different features; the curve at forward bias is parallel shifted after stress toward higher current. The current increase is relatively small, ∼2 times. When a fresh device for stressing with −6 V is used (in order to minimize the effect of previous measurements), the same change of current is obtained. Similar dependence of the curves on V_g is found for W-gated capacitors (not shown). The independence of the gate means that SILC in these two types of stacks is attributed to bulk traps intrinsic to Ta_2O_5 rather than defects close to the gate/Ta_2O_5 interface. Generally, this is consistent with the results of others [18], that during stressing of high-*k*-based devices at the accumulation mode, the oxide-trapped charge is mainly responsible for the SILC. At reverse bias the current after $V_g = -6$ V is almost the same as that corresponding to lower V_g, and the curves are virtually unchanged on stress (figure 1), i.e. the results indicate no stress effect on the interface with Si. The saturation level of the current corresponds to the generation rate of minority carriers in the substrate and as expected is independent of the stress conditions and the gate material.

Comparing the SILC corresponding to a given gate it is seen that the current increase for Au-gate stacks is much higher than the other two gates (figure 2): the current increases with more than one order of magnitude at low forward biases (up to −1 V) and by a factor of 100–1000 for higher voltages. The difference in the current increase for different gates is a result of the complex effect of the electrode work function, the gate-deposition technology and the possible interaction between the top electrode and Ta_2O_5. These factors constitute the initial curves of the unstressed capacitors; devices with Al and W top electrodes exhibit higher currents compared to Au ones. As we have recently reported [24, 25, 27] this higher current is attributed either to gate-deposition-induced defects (this is the case for the W electrode) or to reaction between the gate and Ta_2O_5 (the case for the Al gate). W does not reduce Ta_2O_5 but radiation defects generated during W sputtering are present in the capacitors with the W gate. Additionally the larger work function of Au results in a lower leakage current compared to Al and W electrodes. We will not focus on the exact reasons for the differences in the curves of the unstressed samples, and will consider these curves only as the initial ones of the fresh capacitors. These differences, however, due to some gate effect have to be acknowledged because they reflect on the post-stress curve behavior. Briefly, the initial stacks have in-fabrication traps that may play a role in dielectric degradation due to the stress. So the low initial current of the unstressed Au-electroded capacitors accounts for their apparent higher susceptibilities to CVS. Since J_g levels are nearly the same for the three types of stacks, the SILC actually depends on this initial current level—the higher the initial current (Al and W gates), the lower ΔJ. The post-stress current magnitude at forward bias is virtually independent of the gate (figures 1 and 2) which means that the effect of the gate manifests in a relative change of the SILC rather than in the absolute value of the post-stress current corresponding to various gates.

Let us analyze the left part of the curves in figures 1 and 2. (During a voltage sweep, the forward curve is the main characteristic of the stack.) The relatively low conductivity at low fields (bias from ∼ −0.4 to ∼−0.8 V; applied field E ∼0.3–1 MV cm^{-1}, figure 1) of both initial and stressed stacks with Al and W gates is attributed to trap-assisted tunneling (TAT) ($J \exp E$) [36]. (The thick physical thickness of Ta_2O_5 ∼8 nm reduces the direct tunneling probability through the Ta_2O_5.) TAT also limits the current in Au-gated devices, in the field region of ∼0.9–1.6 MV cm^{-1} before and after stressing with −1 to −5 V, and at E ∼0.2–1.3 MV cm^{-1} after −6 V stressing. Now we will consider the mechanisms of conductivity at higher fields (above the region of both the transient currents and TAT currents). The dominating conduction mechanisms will be considered only generally. The precise analysis requires modeling of the current by using exact values of stack parameters (e.g., the effective mass of electrons in Ta_2O_5; trap density and location; formation of dipole layers at the interfaces; the metal work function which could be different from that used in the literature, etc). Independent measurements of these parameters for these particular stacks have not been performed. Since their values are strongly influenced by a number of technological factors, the data from the literature deliberately are not used to illustrate the conduction mechanisms by a proper energy-band diagram. However, the observed gate dependent current (i.e. the visible effect of metal work function on the *J–V* curves) gives a reason to assume that it is dominated by the electron injection from the gate rather than by hole injection from the accumulation layer. In addition, the rough estimation of the band diagram of Ta_2O_5-based stacks shows that the barrier height for hole injection is substantially higher than that for electron injection supporting the assumption of lower probability for hole injection. With all this in mind, we will

check the validity of Poole–Frenkel (PF) effect and Schottky emission as the most frequently observed mechanisms of leakage in Ta_2O_5. In order to verify whether either of these two mechanisms is present in the films, the curves at forward bias have been drawn (not shown here) in the PF and Schottky plot (the value of dynamic dielectric constant, k_r ($k_r = n^2$), can be derived from the slope of the straight line). In the case of modified PF conduction, the effect of compensating traps is presented by the factor of compensation, r ($1 \leqslant r \leqslant 2$). Considering the measured value of refractive index ($n = 2$), the obtained values of $k_r = 4$ and $r \sim 1.7$ are in agreement with n for stacks with Al and W gates before and after stressing with $V_g = -1$ to -5 V. The same phenomenon is observed in the case of the Au gate ($k_r = 4$ and $r \sim 1.5$, before and after the stress). Therefore, the modified PF conduction governs the current in the three types of capacitors at high applied fields ($E \sim 1$–2.5 MV cm^{-1} when the gates are Al and W, and $E \sim 2$–2.5 MV cm^{-1} when the gate is Au), and the stress at $V_g = -1$ to -5 V does not affect the mechanism of conductivity at all. The results suggest a threshold for generation of a measurable SILC at about -6 V. This is apparently typical of Ta_2O_5-based capacitors since the three types of stacks show the mentioned behavior. The curve of Au-electroded devices after -6 V stress (figure 2) exhibits two distinct regions with a clearly visible change of the trend at ~ -1 V, corresponding to TAT in the low field region and to PF effect domination at higher fields, with $k_r = 4$ and $r = 1.4$. The mechanism of conductivity is preserved, only the compensation factor slightly lowers after -6 V stress. This SILC behavior is little different from that of Al- and W-gated stacks where a parallel shift of the curves toward higher currents is observed after stronger stressing accompanied by no change of either the dominant conduction mechanism or its parameters, k_r and r. In a wider meaning, the difference is attributed to the origin of stress-generated traps as well as to the density of pre-existing traps. Both are a function of the technological history of the samples including the type of gate and the gate deposition technology. The latter can define different physical and chemical nature of the interface region at the gate and/or of the bulk Ta_2O_5, and all this creates specific SILC behavior. The parallel shift of the curves to higher current is indicative of the charge build-up in the layers which modifies the field, and hence the current. It seems that the SILC is due more likely to a charge build-up in the dielectric than to a generation of traps acting as transport sites as in the case of SiO_2 [29]. Therefore, the data imply that the SILC in Ta_2O_5 stacks (regardless of some gate effects) seems generally different from that known for SiO_2. On the other hand, among the possible reasons for SILC widely accepted for SiO_2 (interface trap generation, bulk neutral trap generation, weak spot formation in the dielectric [29–33]), the stress-induced-oxide traps generation is the most possible one for the used gate-injection regimes. We will check this hypothesis for each stack type later. A scenario with the presence of two sets of pre-existing traps with different response to CVS (traps in the virgin stacks which are insensitive to the stress and others which are activated by CVS) is possible as well.

Summarizing this section, gate injection at the stressing voltage from ~ -1 to -5 V slightly affects the current, whereas -6 V stress causes SILC indicating a voltage threshold for SILC generation. CVS at -6 V ($t_s = 50$ s) generates small SILC in Al- and W-gated devices and a significant one in accumulation mode of Au-gated capacitors. Since the current reflects mainly the changes in the cathode electric field, it seems that the traps responsible for SILC are located near the gate/Ta_2O_5 interface. It is evident that unlike the case of SiO_2, SILC in Ta_2O_5-based capacitors is related to defects at the cathode. An explanation may be searched in the different conduction mechanisms in SiO_2 and Ta_2O_5, as a high-k material. The high energy of electrons at anode, defined by Fowler–Nordheim or direct tunneling processes in SiO_2, initiates degradation processes and bulk trap generation in SiO_2 [29–35]. Trap-assisted tunneling or PF conduction via bulk traps currently observed in high-k dielectrics do not ensure high enough energy of electrons at the anode to start degradation processes typical of SiO_2.

3.1.2. Dependence on the stressing time Figures 3(*a*)–(*c*) exhibit J–V curves recorded after various stressing times, at a constant stress voltage of -5 V. All the SILCs over the applied voltage are very small in Al- and W-electroded stacks and saturate at $t_s \sim 100$–500 s (shown for the Al gate in figure 4). As a result of the small stress-induced current variations the shape of the curve remains generally the same as the pre-stress one. In all stressed stacks a transient current component presents in a low bias region (~ -0.7 to +0.5 V). In fact, the stressing time is an indicator whether it is sufficient or not to completely change the charge state of the traps. Figure 3(*a*) shows that as stressing progresses from 50 to 500 s, the magnitude of the current weakly increases at accumulation. The subsequent increase of t_s up to 2000 s does not affect the current any more. The opposite trend of the current variation is detected in the case of the W electrode (figure 3(*b*)); current initially lowers with t_s, and further the general behavior of the SILC with t_s is the same as for the Al gate. This implies that in the former case detrapping and in the later case trapping of electrons occurs as a result of CVS. The current decrease could be a consequence of the partial occupation of pre-existing traps (or newly stress-induced generated traps) and the higher the number of traps, the higher the trapping and less the current through the stack should be. The electron trapping reduces the local field with corresponding current decay. It should be mentioned, however, that the initial stacks with the W gate are quite leaky and subsequently every conclusion on the net effect of the stress has to be considered as speculative. The detrapping is stronger in Au-gated devices resulting in larger $\Delta J/J_0$ compared to Al ones (the current increase is 100–200% at $E > 2$ MV cm^{-1} for Al, and 1–2 orders of magnitude, $E > 1$ MV cm^{-1}, for the Au gate, respectively). Progressive increase of SILC in Au-gated devices with increasing t_s up to 1000 s is visible in figures 3(*c*) and 4; after this t_s, ΔJ is negligible. A scenario different from the detrapping process is also possible when the stress-induced current increase is observed (figures 3(*a*) and (*c*)), namely with increasing t_s the voltage stress generates traps in Ta_2O_5. For 50 s, $< t_s <$ 500 s more traps are created and more electrons tunnel from the cathode to these traps. The essential result of figures 3(*a*)–(*c*)

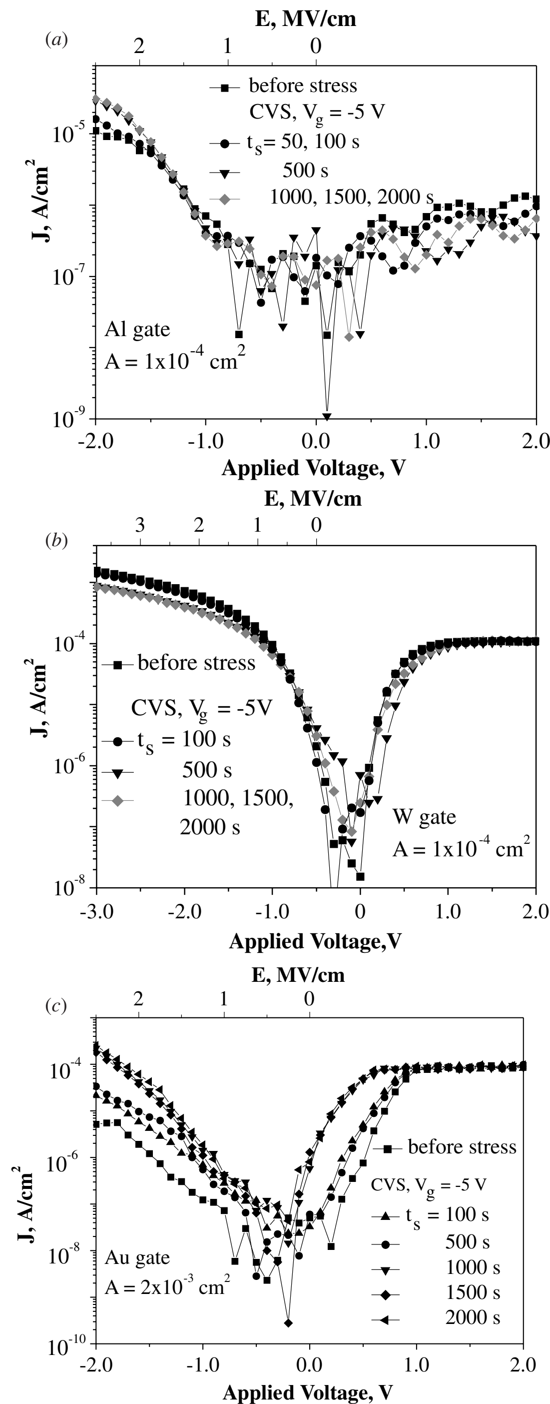

Figure 3. *J–V* characteristics of virgin and stressed capacitors with (*a*) Al, (*b*) W and (*c*) Au gates. $V_g = -5$ V, t_s is a parameter; CVS at 20 °C.

is, however, that CVS over the used t_s does not change the dominant conduction mechanism in the three types of devices. The conduction at fields above ∼1 MV cm^{-1} in Al- and Au-gated stacks before and after stress is through modified PF effect with $k_r = 4$. The stressing time influences only the compensation factor causing it to decrease when t_s is higher than 500 s. This implies that

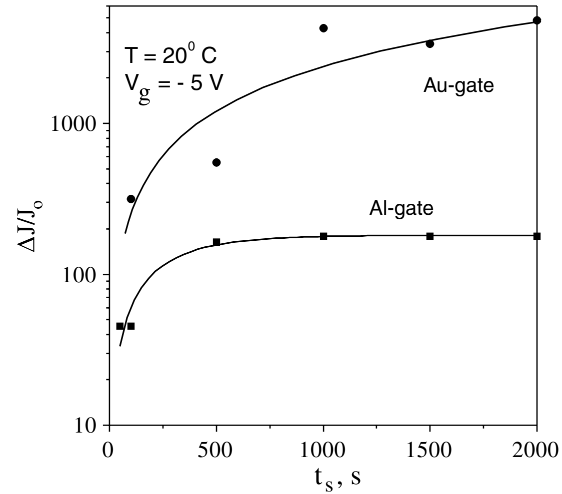

Figure 4. $\Delta J/J_0$ versus stress time for capacitors with Au and Al gates. CVS at 20 °C.

a variation of the relative concentration of both PF centers and compensating traps takes place during the stress with $t_s > 500$ s. For example, the density of compensating centers is higher in both pre-stress and stressed with $50 < t_s < 500$ s Al-gated samples, resulting in a value of $r \sim 2$. Stressing longer than 500 s lowers r through a prevailing of donor traps over the compensating ones, i.e. it seems that the longer t_s stimulate processes in Ta_2O_5 leading to domination of donor traps generation. CVS with t_s of 1000–2000 s does not modify the character of high-field conduction mechanism in Au-gated stacks. Although the characteristics of both unstressed and stressed W-gated stacks seem similar, the curves after stress with $t_s > 50$ s cannot be explained either by PF effect or by Schottky emission for $E > 1.2$ MV cm^{-1}. The curves tend to agree best with the SCLC mechanism (as $J \sim E^2$). An accumulation of trapped electrons at deep states presumably take place resulting in the space charge and then contributes to the leakage current. J in the low-field region (∼0.4–1.2 MV cm^{-1}) obeys an exponential growth dependence consistent with the TAT model. The transient component is more likely due to the process of filling of a portion of traps which do not participate in the above considered conducting processes, i.e. it is a result of specific parameters of a part of the traps (for example, trap localization). Similar to SiO_2 [29, 33], SILC in high-k is often related to trap-assisted tunneling processes [13, 18, 36]. Our results with CCS at accumulation of Ta_2O_5 stacks (Al, W and Au gates) [19] have shown, however, that SILC corresponds to a modified PF effect with a contribution of another conduction mechanism(s), and TAT governs the SILC only at low applied fields. The data here are generally in accordance with those of CCS. Combining the data of both CCS and CVS experiments, it can be said that the mechanism of conductivity in the Ta_2O_5 stack after stressing is a function of its initial parameters rather than of the stressing conditions; most frequently observed mechanisms are TAT, PF emission and SCLC. The variation of the current after stressing is different at low and high fields and depends on the gate as well. The measurable SILC for

Al- and W-gates stacks is detected only in the accumulation regime, i.e. at high fields (figures 3(*a*) and (*b*)). In the case of the Au gate, the leakage current increases with t_s up to ~500–700 s over the applied voltage region (−2 V, 1 V) and the increase tends to saturate for longer t_s (figures 3(*c*) and 4). At low applied fields (up to ~1 MV cm^{-1}) this increase is due to the TAT process and at higher fields the predominant mechanism is the PF one via bulk traps in accordance also with the results for CCS of similar Ta_2O_5 stacks [19]. The current of capacitors with the W gate lowers with t_s (again $t_s \sim 500$ s is a feature time for the current variation) in the high field region due to electron trapping in bulk traps. The origin of these defects is radiation defects generated during the sputtering of W, i.e. they are pre-existing gate-deposition-induced traps [24, 25, 27].

The variation of the curves at reverse bias with stressing time shows the following: SILC in inversion mode is gate dependent; the saturation region of the curves is unaffected by the stress. The current density is reduced under the stress by a factor of 10 in Al-electroded stacks which could be assigned to the charge trapping in interface states; the shape of the curves is generally preserved after the stress. The current variations when the gate is W are almost negligible. CVS causes a significant increase of SILC (up to two orders of magnitude) in Au-gated devices. This effect cannot be attributed to process assisted by the stress-induced traps, since the excess current exhibits the same slope as in the unstressed samples.

Next, the parallel shift at both polarities in the whole voltage range of capacitors with the Au gate (figure 3(*c*)) (which indicates that the leakage conduction maintains the same field dependence as the film undergoes the stress) will be analyzed. The observed large shift reveals positive oxide charge build-up during the stress rather than detrapping as suggested above. The density and the centroid of this charge can be determined by using the following equations [37]:

$$Q_{ot} = (\varepsilon/d)\left[\Delta V_g^- - \Delta V_g^+\right]$$
$$\bar{x} = d\left[1 - \Delta V_g^-/\Delta V_g^+\right]^{-1}.$$

Q_{ot} is the total charge density, $\bar{x}$ is the charge centroid, ΔV_g^- and ΔV_g^+ are the voltage shifts at negative and positive biases, respectively. The Q_{ot} and $\bar{x}$ values for $V_g = -5$ V and different t_s are presented in table 1. The charge density increases with t_s with a clear tendency of saturation at a level of $Q_{ot} = 6 \times 10^{12}$ cm^{-2}. The centroid is at 2.2 nm for $t_s = 50$ s, i.e. it is closer to the Au/dielectric interface. It moves farther from this interface with increasing t_s, reaching a value of 3.8 nm at $t_s > 1000$ s, i.e. the centroid is nearly in the middle of the film implying a homogeneous distribution of the positive charge throughout the whole thickness. These results indicate that the positive charge build-up in Au-gated stacks is a more plausible process than a detrapping one, in good accordance with our results of CCS experiments [19]. Q_{ot} is substantially larger when $V_g = -6$ V than that created at $V_g = -5$ V and $t_s = 50$ s (table 1). The centroid of the charge, however, for the two cases is nearly the same, i.e. it seems that $\bar{x}$ does not depend on the stress voltage. The question why the positive charge build-up happens in devices with the Au gate is at present open. Factors such as gate-deposition-induced defects which become active during the stress could be the starting point for future extensive research on this kind of stack.

Table 1. The density Q_{ot} and the centroid of the stress-induced positive charge build-up as a function of stressing conditions.

Stressing time (s)	$Q_{ot} \times 10^{12}$ (cm^{-2})	Centroid (nm)
	$V_g = -5$ V	
50	3	2.2
100	3.6	2.5
1000	6.1	3.6
1500	6.3	3.8
2000	5.8	3.8
	$V_g = -6$ V	
50	9.7	2.3

3.2. CVS at 100 °C

The simultaneous effect of thermal and voltage stress is studied by performing *J–V* measurements after negative voltage stressing at 100 °C. The pre-stress curves at 100 °C show the following features (figures 5(*a*)–(*c*)) as compared with the corresponding curves at 20 °C: (i) the current increases as the temperature changes from 20 to 100 °C for all samples indicating thermally activated processes of conductivity; (ii) the extent of this increase and the curve shape modification depend on both the gate and the applied voltage—the parallel shift of the curves, over the applied voltages, toward higher current (current increases by ~10×) for the case of the W electrode is observed; the shape of the curves corresponding to Al and Au gates changes with increasing temperature, and the current increase is different for low- and high-voltage regions: for example, $\sim 10^2\times$ at lower (up to −1 V) and $\sim 10^3\times$ at higher biases, in Au-gated devices; (iii) the curves become more symmetrical, indicating a domination of the bulk-limited-conduction mechanism at elevated temperatures. The temperature dependence of the mechanisms of conductivity is not of interest here. We note only that with increasing temperature the dominant conduction mechanism in the pre-stressed samples changes from the PF effect with compensation to either electron-hopping conductivity (Al-gated devices) or the SCLC mechanism (Au- and W-gated ones). The higher temperature activates not only the bulk traps and traps near the gate interface (left part of the figures) but also the interface traps as well, giving rise to the current at reverse bias (figures 5(*a*)–(*c*)). The weak field dependence of the current at 100 °C for Al- and W-gated devices at fields exceeding ~0.5 MV cm^{-1} suggests that the trapping process governs the current [38]. The CVS at 100 °C does not change that for the case of the Al electrode—the curves before and after stress (t_s up to 500 s) are almost parallel. The SCLC mechanism controls the current at longer t_s (500–1000 s) (figure 5(*b*)). The stress also does not affect the shape of the curve of Au-gated capacitors. The conduction in both pre- and post-stressed samples is consistent with the SCLC mechanism, i.e. at $E > 1.5$ MV cm^{-1}, an accumulation of trapped electrons

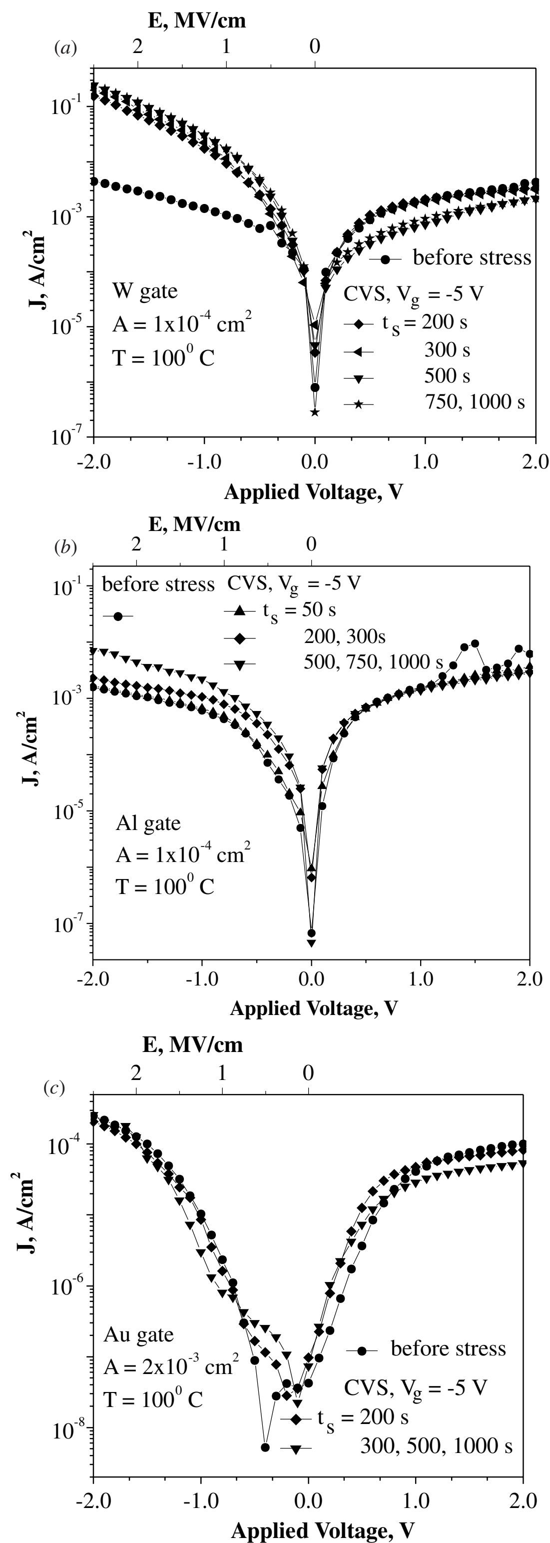

Figure 5. J–V curves before and after CVS at 100 °C, $V_g = -5$ V for capacitors with different gates: (*a*) W, (*b*) Al and (*c*) Au gates; t_s is a parameter.

at deeper traps take place resulting in a space charge. CVS changes the mechanism of conductivity in the case of the W gate resulting to a stronger field dependence of the current

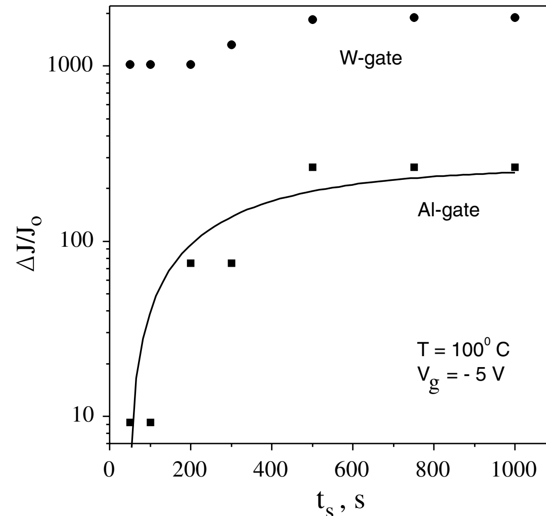

Figure 6. $\Delta J/J_0$ versus stress time for W- and Al-gated capacitors. CVS at 100 °C.

(figure 5(*a*)). The current behavior cannot be explained with a single conduction mechanism and implies the simultaneous effect of several mechanisms. The observed different behavior of the stacks with various top electrodes is attributed to the nature and density of traps located predominantly at the electrode interface and their response to the stress. The probability of one or another response, which constitutes the dominant conduction mechanism, depends on the parameters of these traps which are a function of the type of gate and the method of its deposition. The current in Au-electroded devices is not sensitive to gate injection with V_g from -1 to -5 V at stressing time from 50 to 1000 s (the largest used here) (figure 5(*c*))—the capacitors have a stable, relatively low current (it is approximately two orders of magnitude lower than that in Al- and W-gated ones) and this current is intact during the stress. In the low-voltage region at two voltage polarities very small SILC is observed, which is addressed to the slight effects of tunneling processes via both the interface states and the slow states. The SILC at accumulation mode begins to occur at t_s ~200–300 s for each of the three types of capacitors (figures 5(*a*)–(*c*)). The leakage slightly increases with t_s and $\Delta J/J_0$ saturates beyond stressing time of ~500 s (Al and W gates, figure 6). The very small SILC in Au-gated stacks for all t_s, consistently implies again that the mechanism of SILC creation is different from that known for SiO_2, where hydrogen or holes generated at the anode [29–32, 34, 35, 39, 40] account for the generation of bulk neutral traps and therefore for SILC. Note that any effect of H-induced defects, which result from hydrogen particles created by the injected electrons close to the Si interface and further transported into the high-*k* [41], can hardly account for the SILC, because the capacitors were not subjected to post-metallization anneal in N_2/H_2. Therefore, the probability of hydrogen presence in the stacks (which could be potentially released at the Si interface) is small. It is not negligible, however, having in mind that hydrogen could be everywhere in the stack and is predominantly located at the Si interface of the high-*k* capacitors.

Generally, the SILC could be a result of the combined effect of neutral trap generation, electron trapping in pre-existing traps and positive charge generation. The positive charge is usually related to oxygen vacancies in Ta_2O_5, and as mentioned above it is unlikely to come from hydrogen diffusion in the stack. Among these possible processes the second one appears to be to the greatest extent an explanation of many of our results: (i) the observed saturation region in the SILC and the weak dependence on t_s (figures 3 and 5) is consistent with the assumption that SILCs are related to pre-existing traps rather than generation of new traps by the stress. The saturation region can be caused by the limited number of available traps which can capture electrons; (ii) electron trapping is likely responsible for the slight SILC also observed at CVS at 100 °C—trapping is known to be weakly temperature dependent. Considering all this, a more thorough explanation of the results for Al-gated capacitors is the following. Figure 1 reveals that a voltage higher than $|-3|$ V is required for a measurable SILC generation; further the current does not depend on V_g in the range $|-3| \leqslant V_g \leqslant |-5|$ V. At $V_g = -6$ V an increase of SILC is observed. It suggests that two different mechanisms are responsible for SILC. The first one is dominant in the V_g range, -3 to -5 V, and most likely is related to trapping in pre-existing sites. This hypothesis is confirmed by figures 4 and 6. The $\Delta J/J_0$ versus t_s dependences measured at room temperature and 100 °C fit well with a first-order trapping kinetics which means no generation of additional traps. However, the electron trapping itself could not create SILC. Another condition to fulfill is a threshold for SILC creation that in this case is about -3 V. Therefore, the possible scenario is the trapping of electrons in pre-existing sites that leads to weakening of some bonds which break at voltages higher than this threshold and create defects giving rise to SILC [42]. Further, at $V > |-5|$ V (second threshold) another mechanism is also involved which creates significant SILC. Regarding microstructural aspects of the defects, weak Ta–O, Si–O bonds, off-stoichiometry defects all these represent precursors of the degradation. The data strongly imply that the pre-existing traps in the stacks are addressed to poor-oxidation related defects (to a smaller extent) and to gate-induced defects (to a larger extent).

3.3. Breakdown events

Destructive breakdown (BD) does not occur for all the samples. More precisely, the current behavior (i.e. very large SILC) which can be assigned to both soft and hard breakdown is not observed. BD events do not occur even after $t_s = 2000$ s (figures 3 and 5). It does not mean that BD is completely absent in the samples during CVS. The relatively big gate area of the devices studied obviously hampers the direct observation of BD events. The intrinsic BD is more representative of the intrinsic dielectric quality at least by analogy with SiO_2 devices, and has to be studied with gate areas of $\sim 10^{-6}$ cm^2. Although the BD mechanism(s) in high-k insulators is ultimately different from that of SiO_2, we speculate that the used gate areas are sufficiently large to reveal some kind of intrinsic breakdown in Ta_2O_5 devices, if it exists at all. At the same time, the lack of well-pronounced BD events is indirect support of the conclusion that the extrinsic gate-induced defects are mainly responsible for the stress degradation in our samples. Soft BD can be observed during CVS and is manifested as a sudden increase in the current. It is considered to result from a weak localized percolation path between the gate and the substrate formed when the electron traps in the dielectric reach a critical number. Considering the large gate area for revealing BD, the current fluctuations around the zero bias (figures 1–3) can be due indeed to trapping–detrapping of electrons in traps located near the Si interface (as already discussed) and not to analog processes in the percolation clusters [18]. The breakdown characteristics and the device behavior after BD events are beyond the scope of this study, but their importance and possible manifestation should be acknowledged. In this sense, the very slow growth of the leakage at relatively low voltages can be addressed to 'progressive' breakdown, i.e. gradual hard BD [43, 44].

4. Conclusion

The most important features of the data presented are the following.

The pre-existing traps are a key parameter to evaluate CVS degradation under gate injection in Ta_2O_5 stacks. There is a stress-voltage threshold for generation of a significant leakage current in the accumulation mode of capacitors, and the SILC is gate dependent. We speculate that this is a result of a complex effect of the electrode work function and the gate-induced traps, and the impact of the latter is stronger. The effect of the gate manifests in a relative change of the SILC rather than in the magnitude of the post-stress current corresponding to various gates. Among the top electrodes investigated the stack with the Au gate is the most susceptible to the stress degradation. Despite some gate effects, the mechanism of the stress-induced current seems different from that known for SiO_2: the processes of electron trapping at pre-existing traps and positive charge build-up are responsible for SILC in this particular high-k stack; there is no evidence for stress-induced generation of new traps. In addition, unlike the case of SiO_2, SILC in the three types of capacitors is mainly related to defects at the gate (cathode in our experiments). We assume that the same fundamental difference in the conduction mechanisms governing the current in Ta_2O_5 and SiO_2 is responsible for the different origin of SILC in the two cases. A number of the results obtained (small SILC, the saturation level of SILC, stress-voltage and stress-time threshold(s) to detect measurable SILC, weak temperature effect on the SILC) are indicative of the presence of a trapping process. Considering, however, that the electron trapping itself could not create the stress-induced current, the degradation can be presented as a three-stage process: (i) electron trapping at pre-existing traps at the beginning of the low-voltage stress; the trapping weakens some bonds; (ii) breaking of these bonds at higher voltage stress, which manifests as the appearance of a stress-voltage threshold; (iii) further, when the stress voltage increases another mechanism (giving a significant rise in SILC) is involved, and a second stress-voltage threshold

is detected. If this mechanism corresponds to positive charge species trapping at pre-existing defects, the build-up of positive charges is observed, as in the Au-gated capacitors. Whatever the dominant process is, the data imply that the origin of CVS-created degradation in Ta_2O_5-based capacitors is not the same as that in SiO_2.

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